

# FDP027N08B\_F102

## N-Channel PowerTrench® MOSFET

80 V, 223 A, 2.7 mΩ

### Features

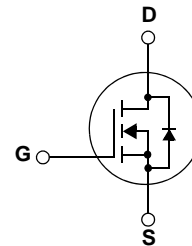
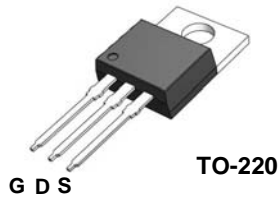
- $R_{DS(on)} = 2.21 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 100 \text{ A}$
- Low FOM  $R_{DS(on)} * Q_G$
- Low Reverse Recovery Charge,  $Q_{rr} = 112 \text{ nC}$
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP027N08B_F102	Unit
$V_{DSS}$	Drain to Source Voltage	80	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	223*
		-Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	158*
		-Continuous ( $T_C = 25^\circ\text{C}$ , Package Limited)	120
$I_{DM}$	Drain Current	- Pulsed (Note 1)	892
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	917
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	246
		- Derate above $25^\circ\text{C}$	1.64
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A

### Thermal Characteristics

Symbol	Parameter	FDP027N08B_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.61	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Description	Quantity
FDP027N08B	FDP027N08B_F102	TO-220	F102: Trimmed Leads	50

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.05	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 64\text{V}, T_C = 150^\circ\text{C}$	-	-	1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 100\text{A}$	-	2.21	2.7	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 100\text{A}$	-	227	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	10170	13530	pF
$C_{oss}$	Output Capacitance		-	1670	2220	pF
$C_{riss}$	Reverse Transfer Capacitance		-	35	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	3025	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40\text{V}, V_{GS} = 10\text{V}$ $I_D = 100\text{A}$	-	137	178	nC
$Q_{gs}$	Gate to Source Gate Charge		-	56	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	25	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	28	-
ESR	Equivalent Series Resistance (G-S)	$f = 1\text{MHz}$	-	2.4	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{V}, I_D = 100\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.7\Omega$	-	47	104	ns
$t_r$	Turn-On Rise Time		-	66	142	ns
$t_{d(off)}$	Turn-Off Delay Time		-	87	184	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	41	92

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	223*	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	892	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 100\text{A}$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, V_{DD} = 40\text{V}, I_{SD} = 100\text{A}$	-	80	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt = 100\text{A}/\mu\text{s}$	-	112	-	nC

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 3\text{mH}, I_{AS} = 24.72\text{A}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 100\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

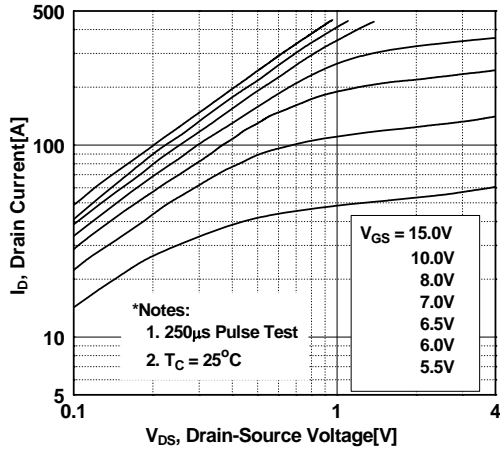


Figure 2. Transfer Characteristics

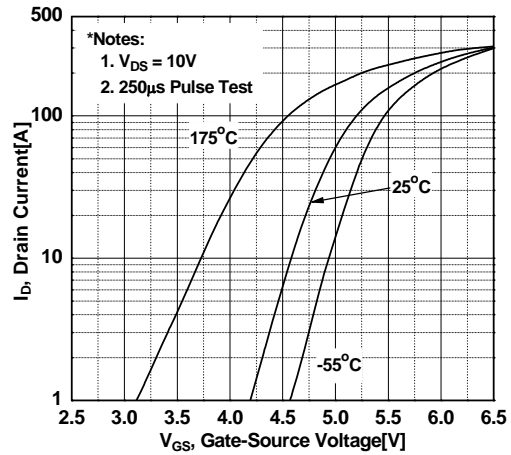


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

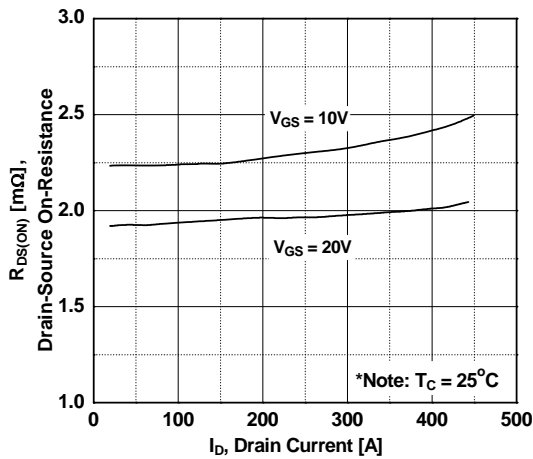


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

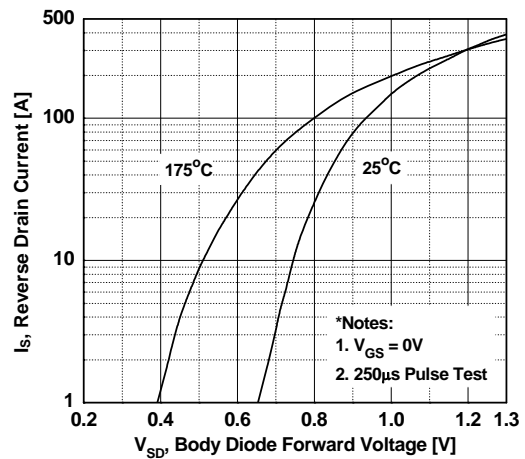


Figure 5. Capacitance Characteristics

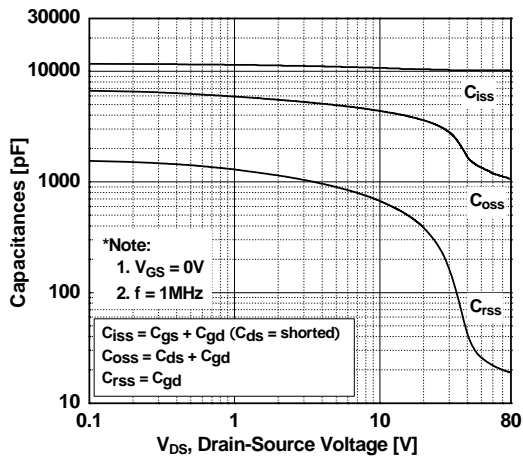
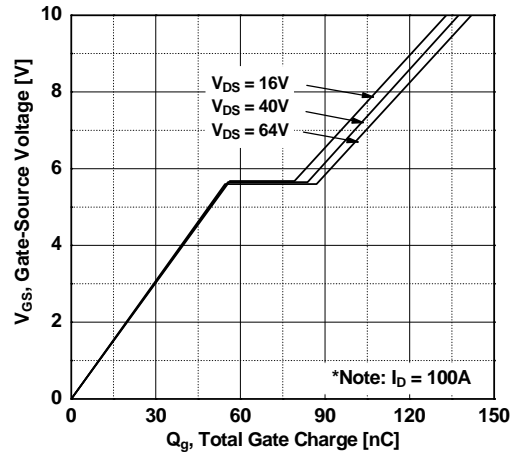
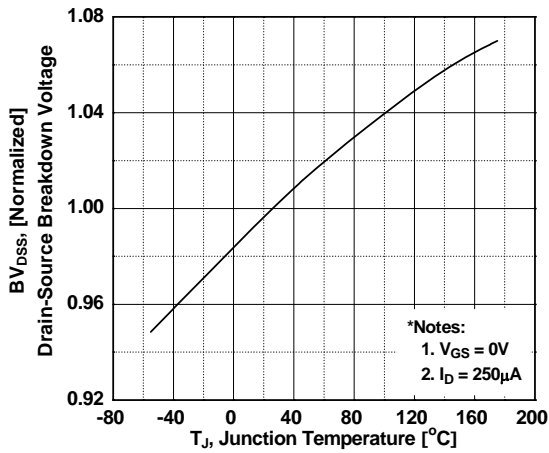


Figure 6. Gate Charge Characteristics

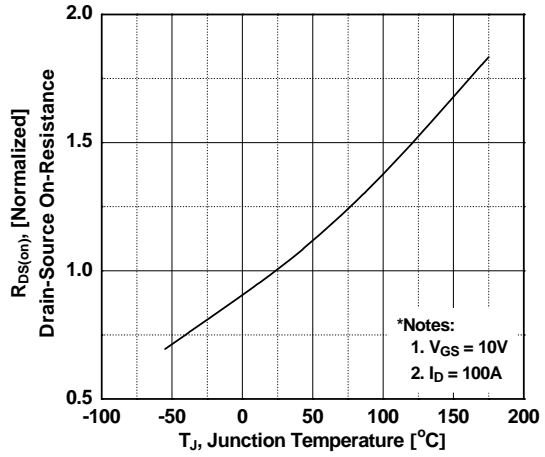


## Typical Performance Characteristics (Continued)

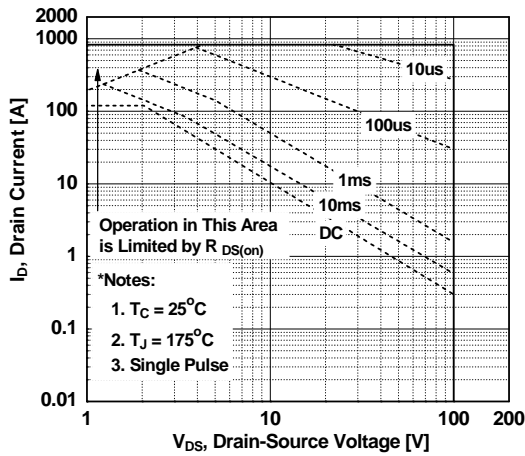
**Figure 7. Breakdown Voltage Variation vs. Temperature**



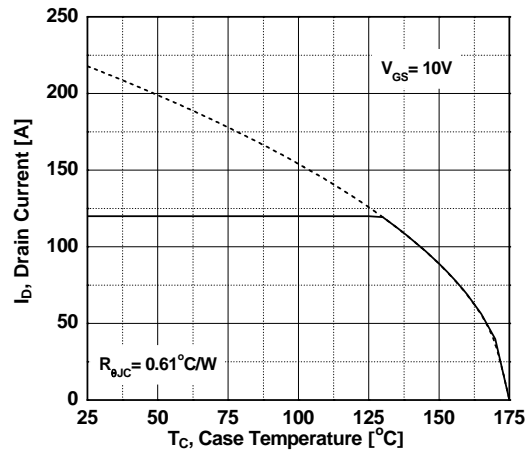
**Figure 8. On-Resistance Variation vs. Temperature**



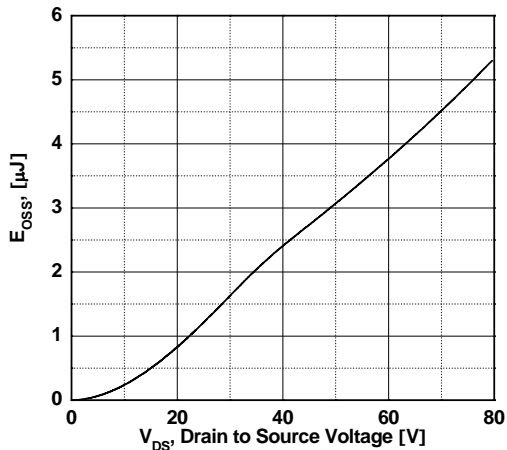
**Figure 9. Maximum Safe Operating Area vs. Case Temperature**



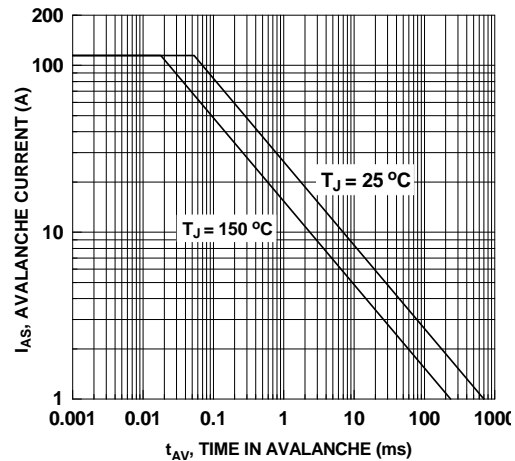
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E\_oss vs. Drain to Source Voltage Switching Capability**

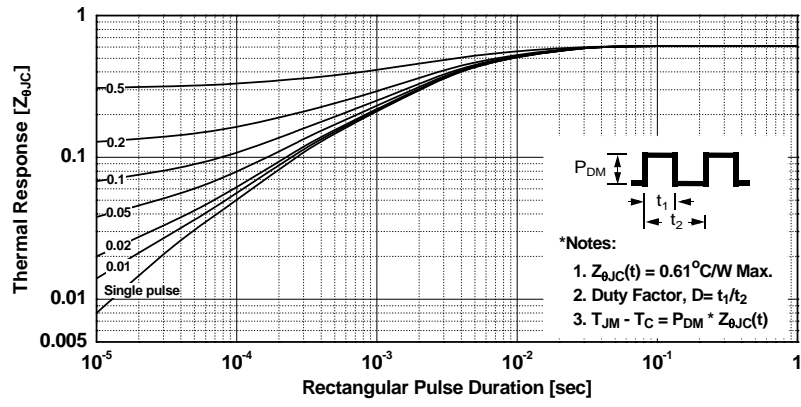


**Figure 12. Unclamped Inductive**

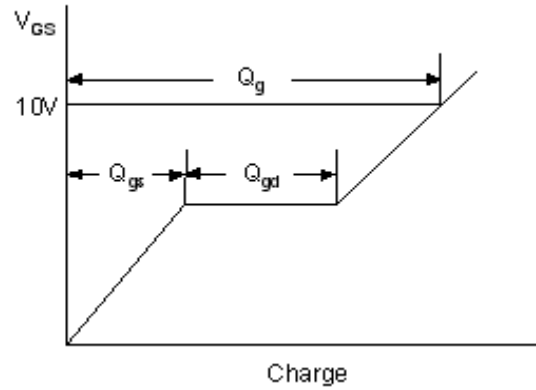
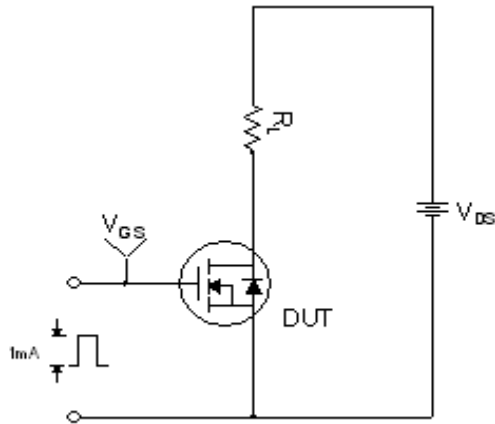


Typical Performance Characteristics (Continued)

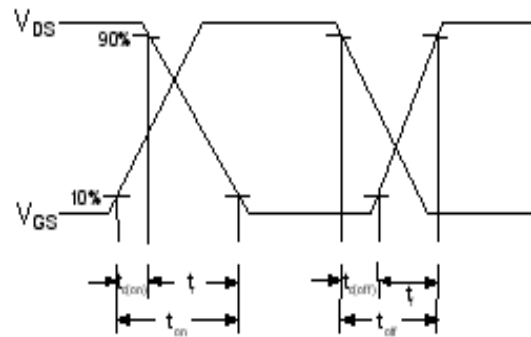
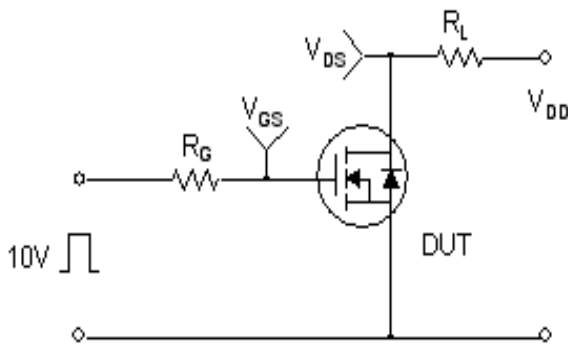
Figure 13. Transient Thermal Response Curve



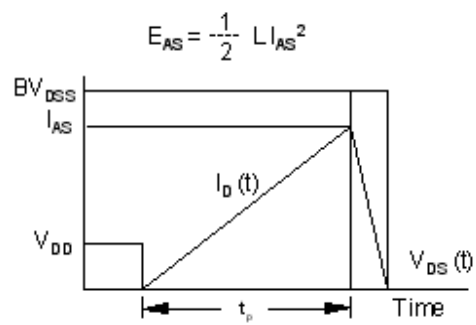
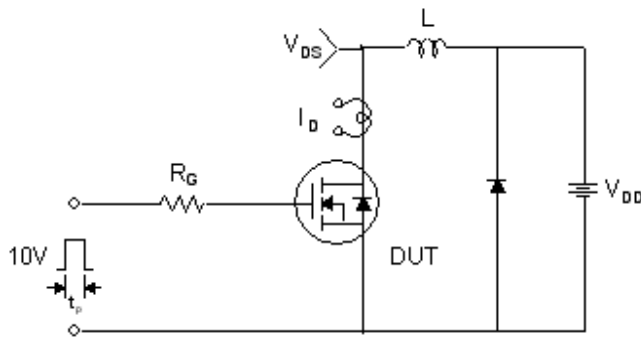
**Gate Charge Test Circuit & Waveform**



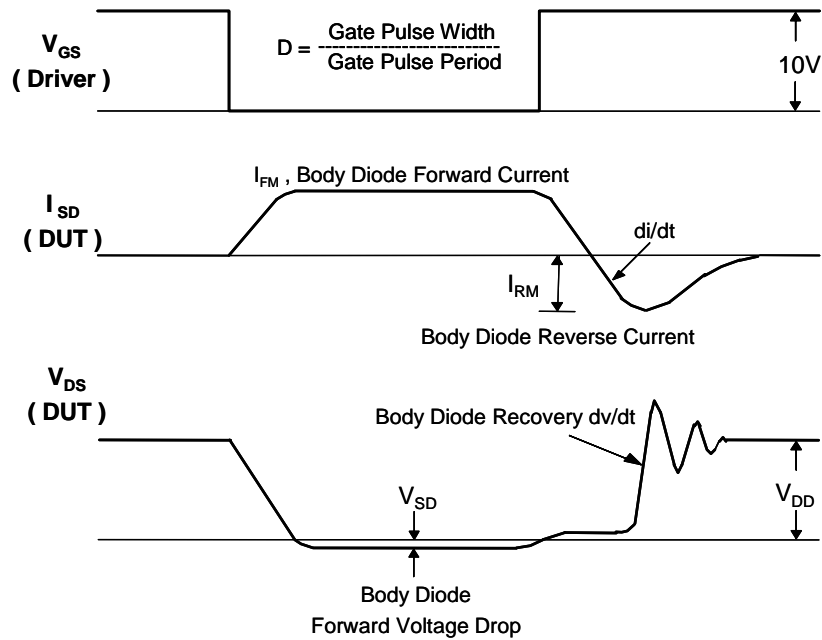
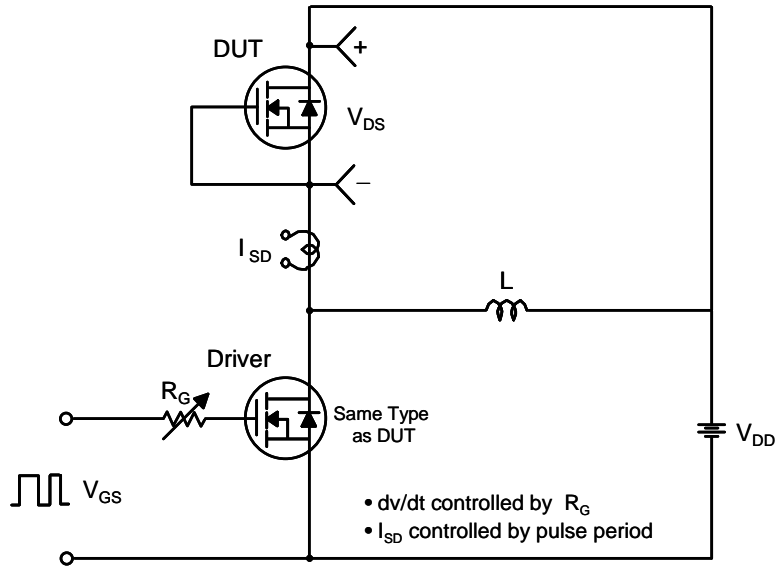
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



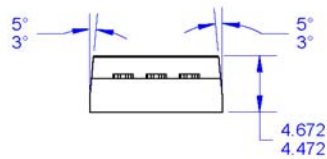
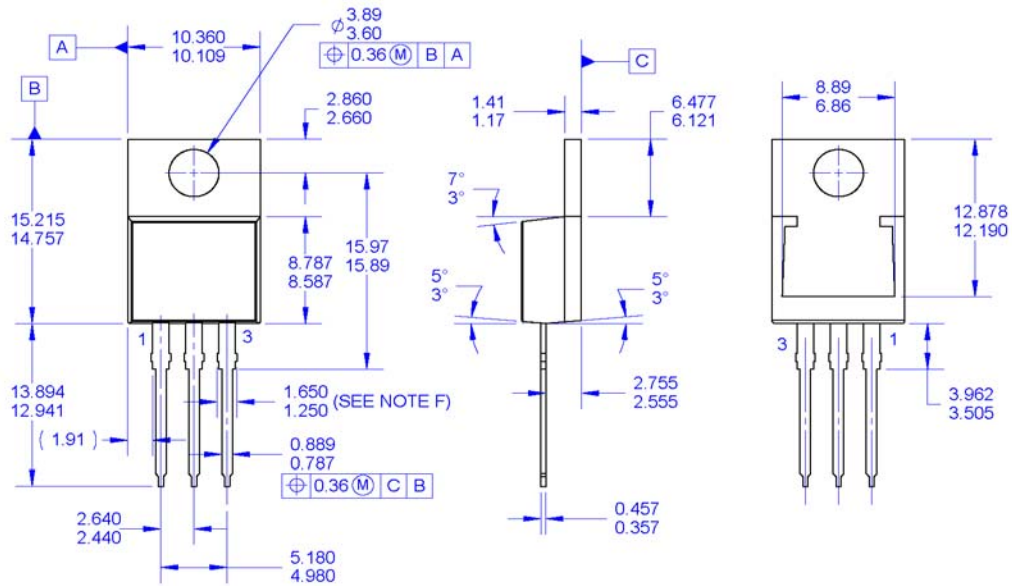
Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

# TO-220

(F102: Trimmed Leads)



### NOTES:


- PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- THIS PACKAGE IS FSZZ INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.
- MAX WIDTH FOR F102 DEVICE = 1.35mm.
- DRAWING FILE NAME: TO220T03REV3





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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