# CY62137FV18 MoBL®

# 2-Mbit (128 K × 16) Static RAM

## Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V to 2.25 V
- Pin compatible with CY62137CV18
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 5 µA
- Ultra low active power
  - Typical active current: 1.6 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Byte power-down feature
- Available in a Pb-free 48-ball Very fine-pitch ball grid package (VFBGA) package

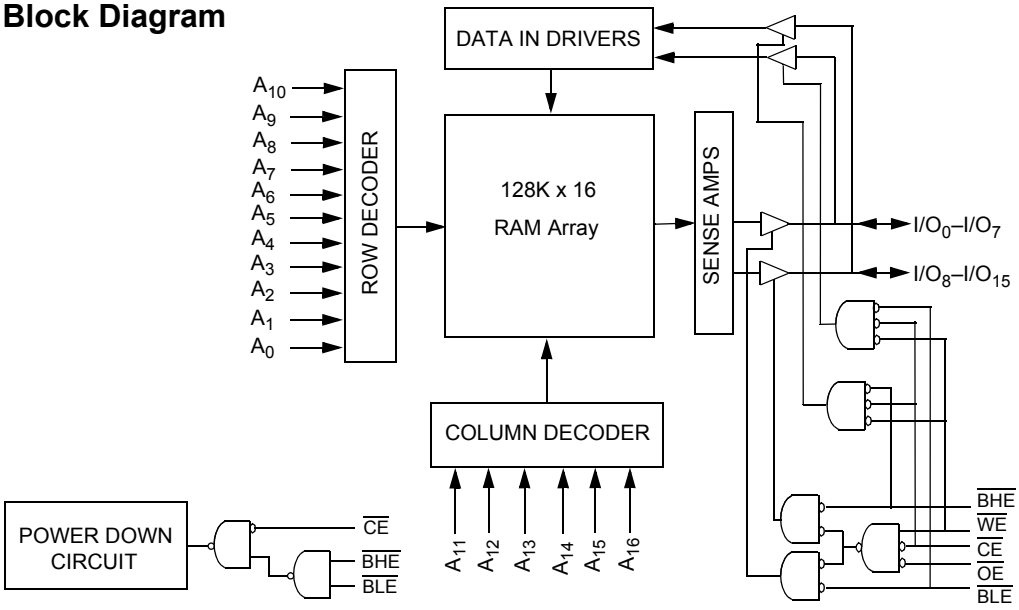
## Functional Description

The CY62137FV18 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins ($I/O_0$ through $I/O_{15}$) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both the Byte High Enable and the Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during an active write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$) is written into the location specified on the address pins ($A_0$ through $A_{16}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{16}$).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from the memory appears on $I/O_8$ to $I/O_{15}$. See the Truth Table on page 11 for a complete description of read and write modes.

## Logic Block Diagram



## Contents

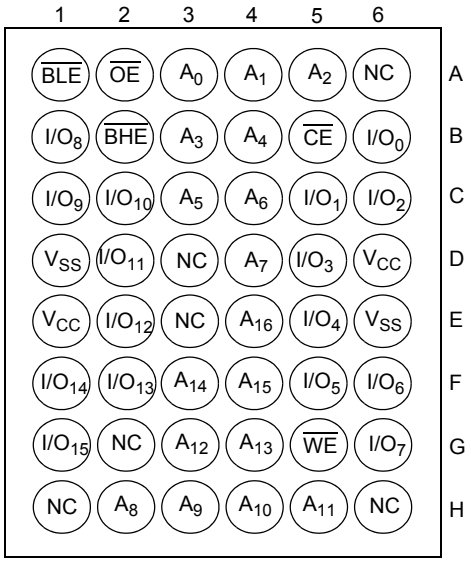
## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | Min | Typ [1] | Max | | Typ [1] | Max | Typ [1] | Max | Typ [1] | Max |
| CY62137FV18LL | 1.65 | 1.8 | 2.25 | 55 | 1.6 | 2.5 | 13 | 18 | 1 | 5 |

## Pin Configuration

**Figure 1. 48-ball VFBGA pinout [2, 3]**

**Top View**




**Notes**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.2 V to + 2.45 V

DC voltage applied to outputs in High Z State [4, 5] .....–0.2 V to 2.45 V

DC Input Voltage [4, 5] .....–0.2 V to 2.45 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up Current .....> 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [6] |
|---|---|---|---|
| CY62137FV18 | Industrial | –40 °C to +85 °C | 1.65 V to 2.25 V |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 55 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [7] | Max | |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = –0.1 mA | | 1.4 | – | – | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 0.1 mA | | – | – | 0.2 | V |
| $V_{IH}$ | Input high voltage | $V_{CC}$ = 1.65 V to 2.25 V | | 1.4 | – | $V_{CC}$ + 0.2 | V |
| $V_{IL}$ | Input low voltage | $V_{CC}$ = 1.65 V to 2.25 V | | –0.2 | – | 0.4 | V |
| $I_{IX}$ | Input leakage current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_O$ ≤ $V_{CC}$, output disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | f = $f_{max}$ = 1/$t_{RC}$ | $V_{CC(max)}$ = 2.25 V, $I_{OUT}$ = 0 mA, CMOS levels | – | 13 | 18 | mA |
| | | f = 1 MHz | $V_{CC(max)}$ = 2.25 V | – | 1.6 | 2.5 | mA |
| $I_{SB1}$ [8] | Automatic power-down current – CMOS inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2 V, or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≤ 0.2 V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$) | $V_{CC(max)}$ = 2.25 V | – | 1 | 5 | µA |
| $I_{SB2}$ [8] | Automatic power-down current – CMOS inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2 V, or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V, or $V_{IN}$ ≤ 0.2 V, f = 0 | $V_{CC(max)}$ = 2.25 V | – | 1 | 5 | µA |

**Notes**

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$=$V_{CC}$ + 0.5 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC}$(min) and 200 µs wait time after $V_{CC}$ stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.

## Capacitance

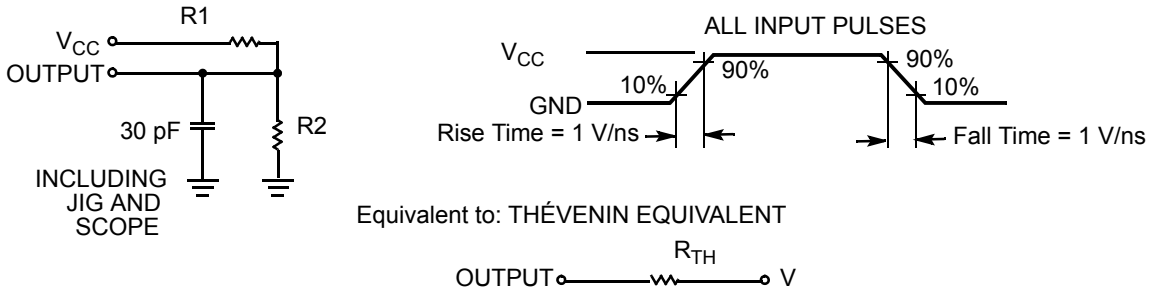
| Parameter [9] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [9] | Description | Test Conditions | 48-ball VFBGA | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 75 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 10 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**




| Parameters | 1.80 V | Unit |
|---|---|---|
| R1 | 13500 | Ω |
| R2 | 10800 | Ω |
| $R_{TH}$ | 6000 | Ω |
| $V_{TH}$ | 0.80 | V |

**Note**
9. Tested initially and after any design or process changes that may affect these parameters.

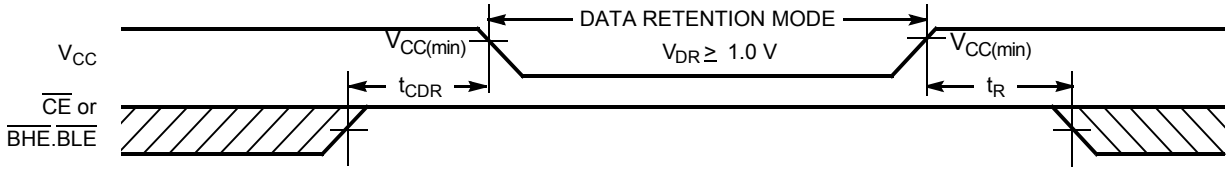
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ [10] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | 1.0 | – | – | V |
| $I_{CCDR}$ [11] | Data retention current | $V_{CC}$ = 1.0 V, $\overline{CE} \geq V_{CC} - 0.2$ V, or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 1 | 4 | µA |
| $t_{CDR}$ [12] | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R$ [13] | Operation recovery time | | 55 | – | – | ns |

## Data Retention Waveform

**Figure 3. Data Retention Waveform** [14]




**Notes**

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range

| Parameter [15, 16] | Description | 55 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 55 | – | ns |
| $t_{AA}$ | Address to data valid | – | 55 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z [17] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z [17, 18] | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z [17] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z [17, 18] | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power down | – | 55 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to data valid | – | 55 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to low Z [17] | 10 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to high Z [17, 18] | – | 18 | ns |
| **Write Cycle** [19] | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 35 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 35 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z [17, 18] | – | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z [17] | 10 | – | ns |

**Notes**

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the Figure 2 on page 5.
16. In an earlier revision of this device, under a specific application condition, READ operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
18. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Figure 4. Read Cycle No.1 (Address Transition Controlled)** [20, 21]

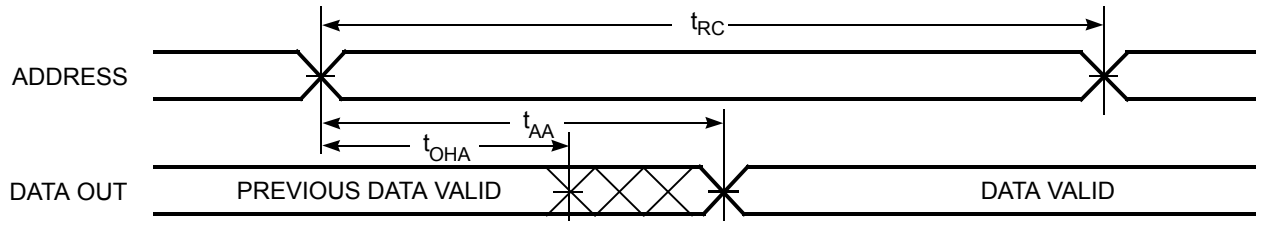
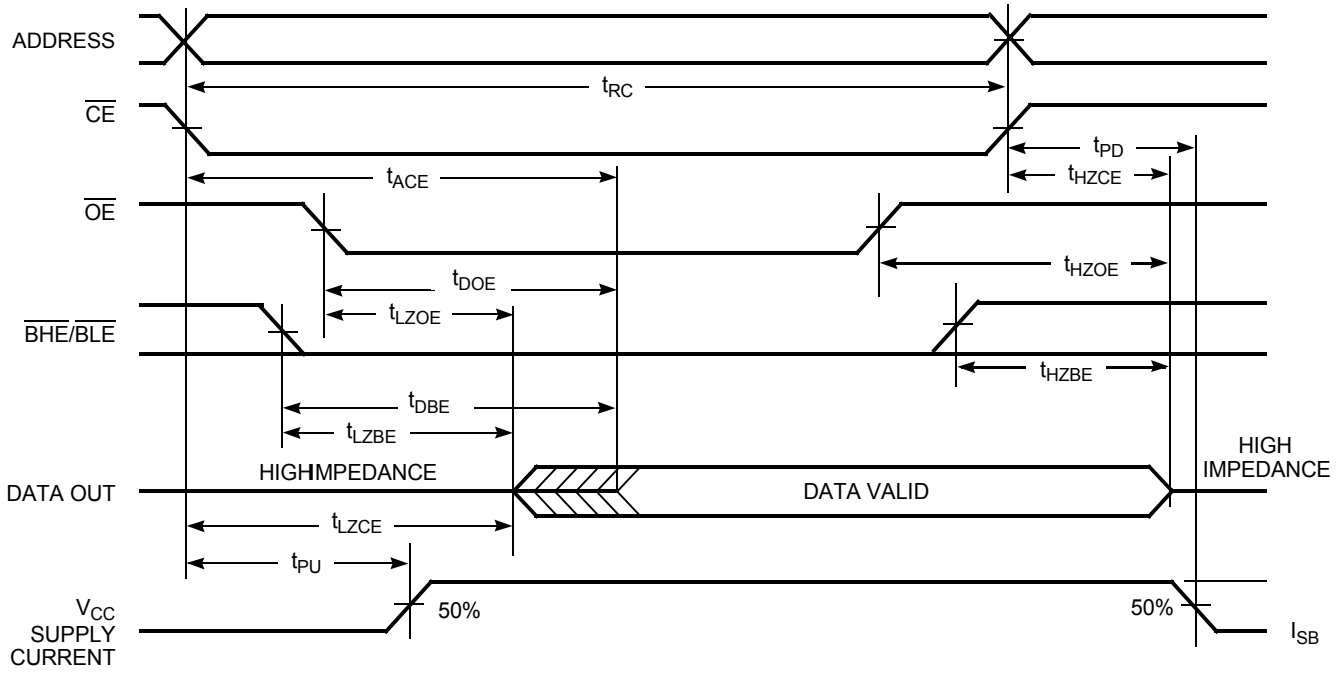



**Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [21, 22]




**Notes**
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 (WE Controlled) [23, 24]**

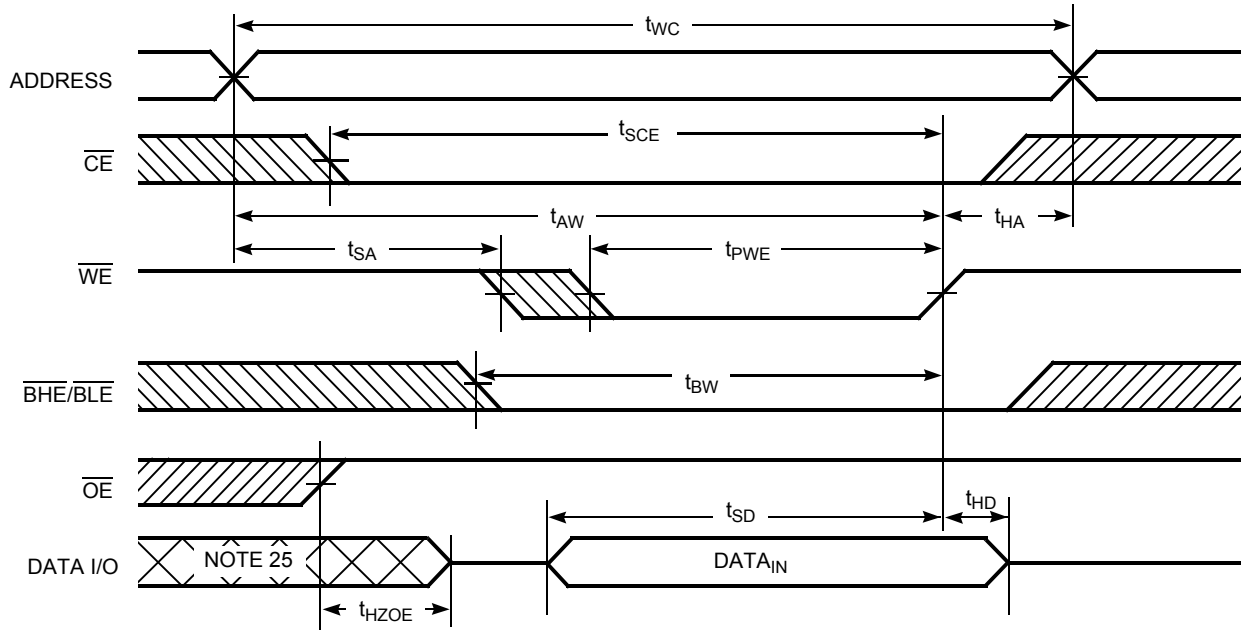
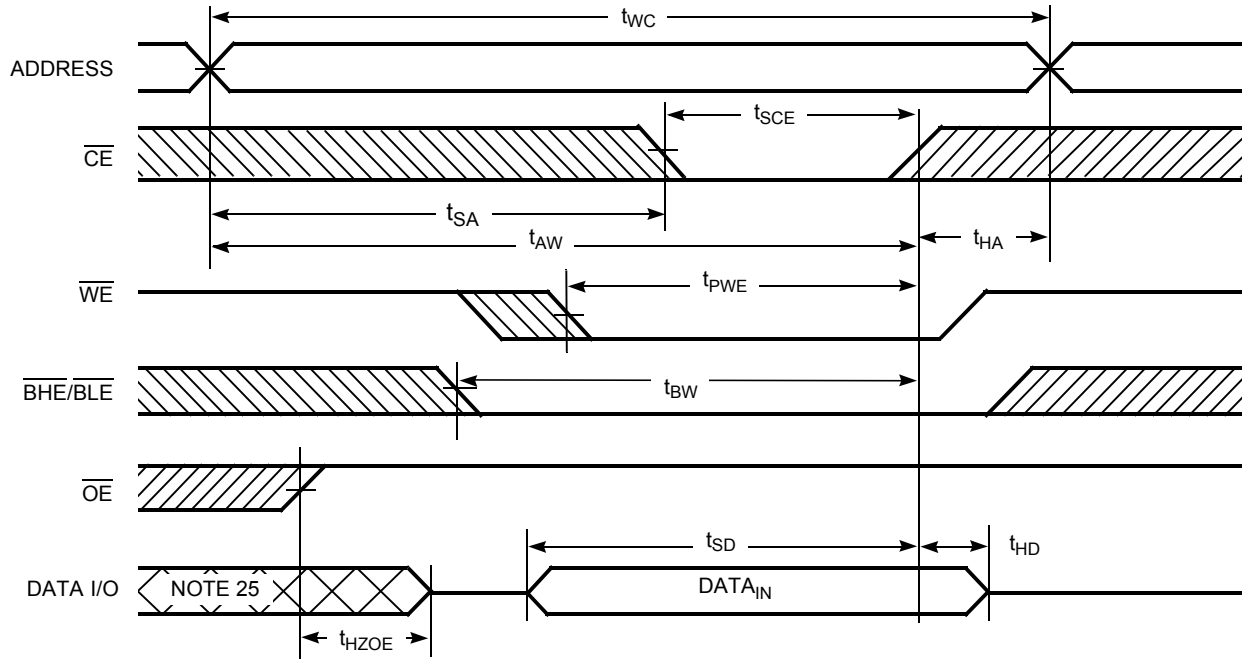



**Figure 7. Write Cycle No. 2 (CE Controlled) [23, 24]**




**Notes**
23. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 (WE Controlled) [26]**

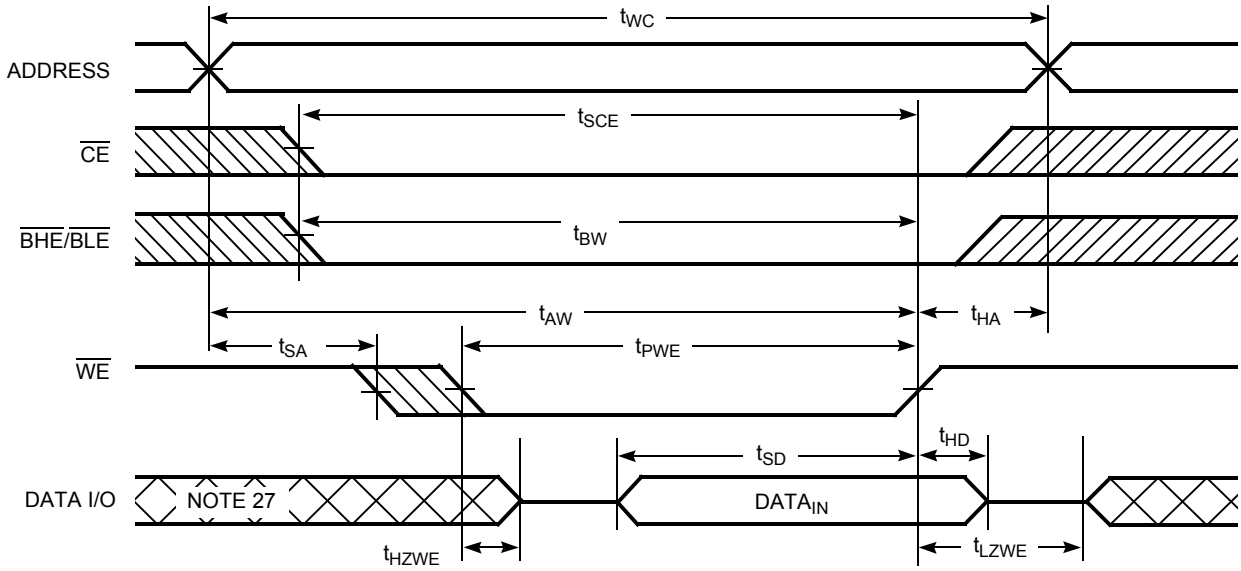
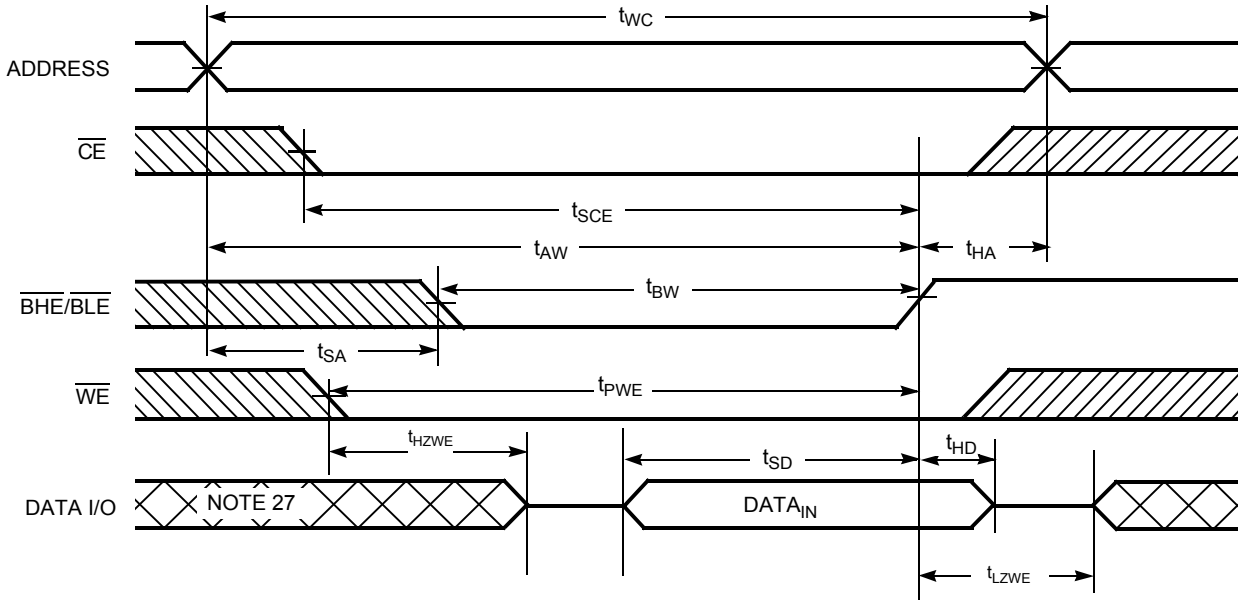



**Figure 9. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [26]**




**Notes**
26. If CE goes HIGH simultaneously with WE = $V_{IH}$, the output remains in a high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs or Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X[28] | X[28] | High Z | Deselect or power down | Standby ($I_{SB}$) |
| X[28] | X | X | H | H | High Z | Deselect or power down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data out ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data in ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data in ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data in ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Write | Active ($I_{CC}$) |

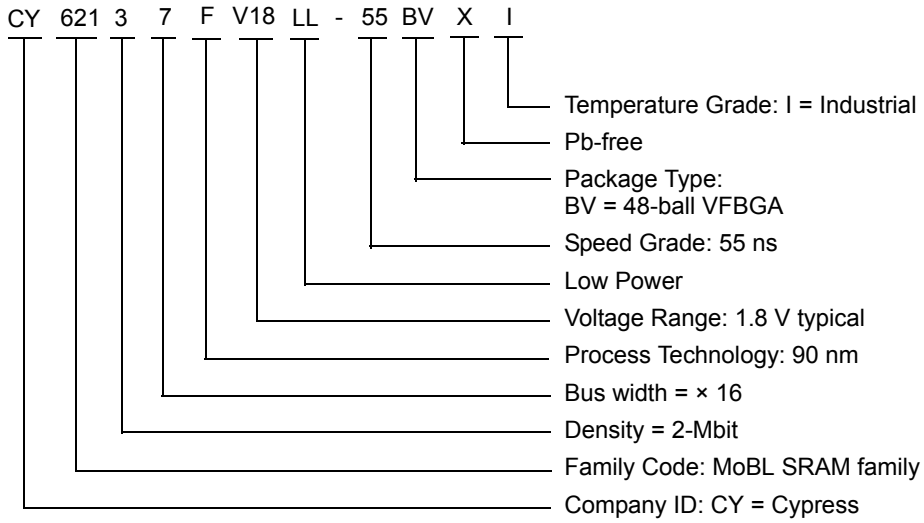
**Note**
28. The 'X' (Don't care) state for the Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ and $\overline{BLE}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62137FV18LL-55BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | Industrial |

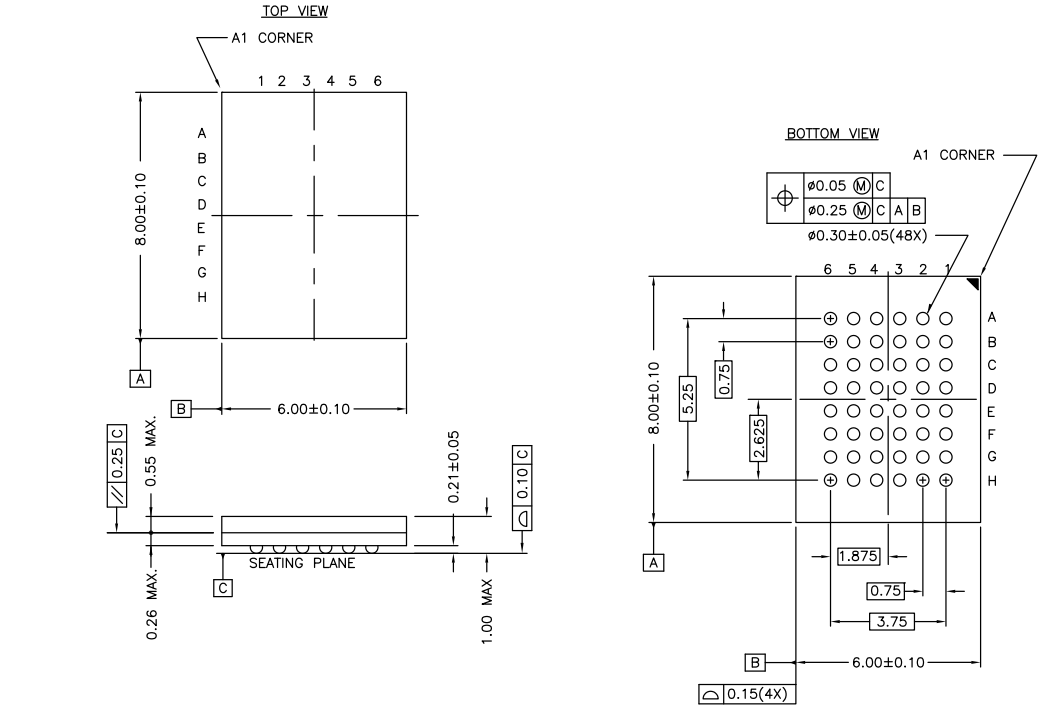
Contact your local Cypress sales representative for availability of other parts.

### Ordering Code Definitions



## Package Diagram

**Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150**




NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{BHE}$ | Byte High Enable |
| $\overline{BLE}$ | Byte Low Enable |
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62137FV18 MoBL®, 2-Mbit (128 K × 16) Static RAM<br>Document Number: 001-08030 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 463660 | See ECN | NXR | New data sheet. |
| *A | 469180 | See ECN | NSI | Minor change: moved to external web |
| *B | 569125 | See ECN | NXR | Converted from preliminary to final<br>Replaced 45 ns speed bin with 55 ns speed bin<br>Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition f=1 MHz<br>Changed the $I_{SB2(typ)}$ value from 0.5 μA to 1 μA<br>Changed the $I_{SB2(max)}$ value from 2.5 μA to 5 μA<br>Changed the $I_{CCDR(typ)}$ value from 0.5 μA to 1 μA and $I_{CCDR(max)}$ value from 2.5 μA to 4 μA |
| *C | 869500 | See ECN | VKN | Added footnote #12 related to $t_{ACE}$ |
| *D | 908120 | See ECN | VKN | Added footnote #8 related to $I_{SB2}$ and $I_{CCDR}$<br>Made footnote #13 applicable to AC parameters from $t_{ACE}$<br>Changed $t_{WC}$ specification from 45 ns to 55 ns<br>Changed $t_{SCE}$, $t_{AW}$, $t_{PWE}$, $t_{BW}$ specification from 35 ns to 40 ns<br>Changed $t_{HZWE}$ specification from 18 ns to 20 ns |
| *E | 1274728 | See ECN | VKN/AESA | Changed $t_{WC}$ specification from 55 ns to 45 ns<br>Changed $t_{SCE}$, $t_{AW}$, $t_{PWE}$, $t_{BW}$ specification from 40 ns to 35 ns<br>Changed $t_{HZWE}$ specification from 20 ns to 18 ns |
| *F | 2943752 | 06/03/2010 | VKN | Added Contents<br>Added footnote related to Chip enable and Byte enables in Truth Table<br>Updated Package Diagram<br>Added Sales, Solutions, and Legal Information |
| *G | 3055165 | 10/12/2010 | RAME | Added Contents<br>Added Acronyms and Units of Measure<br>Update Package Diagram from *E to *F<br>Added Ordering Code Definitions details.<br>Changed $I_{SB1}/I_{SB2}/I_{CCDR}$ test conditions to reflect byte power down feature |
| *H | 3061313 | 10/15/2010 | RAME | Minor Changes: Corrected CE to $\overline{CE}$ and WE to $\overline{WE}$ in Figures 7 and 8 |
| *I | 3263825 | 06/17/2011 | RAME | Replaced CE and OE with $\overline{CE}$ and $\overline{OE}$ in all instances in page 1.<br>Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”).<br>Updated in new template. |
| *J | 4102185 | 08/22/2013 | VINI | Updated Switching Characteristics:<br>Updated Note 16.<br><br>Updated Package Diagram:<br>spec 51-85150 – Changed revision from *F to *H.<br><br>Updated in new template. |
| *K | 4208614 | 12/03/2013 | MEMJ | Updated Features:<br>Removed repeated instance of “Ultra low standby power”.<br><br>Completing Sunset Review. |

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