CY62126EV30 MoBL®

1-Mbit (64 K × 16) Static RAM

Features

- High speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
  - Automotive-E: –40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62126DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II packages

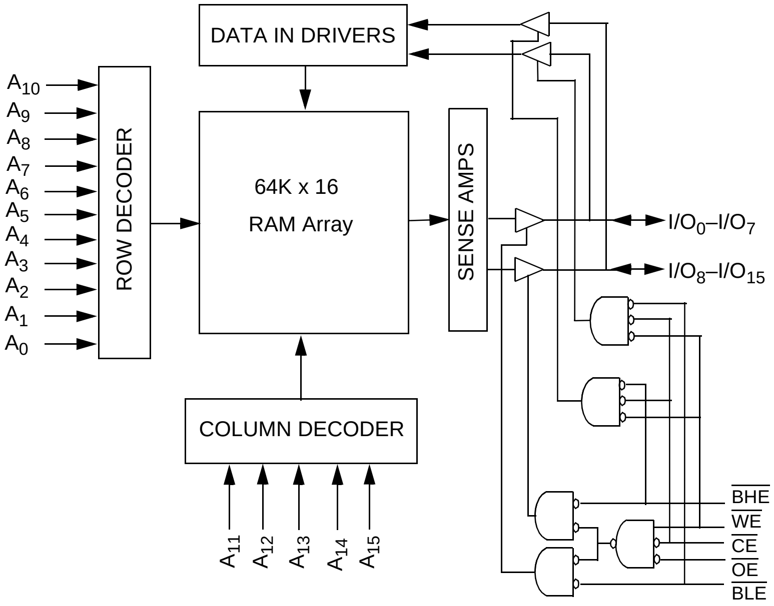
Functional Description

The CY62126EV30 is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{\text{CE}}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH) or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

To write to the device, take Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

To read from the device, take Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

Logic Block Diagram



Contents

Pin Configuration

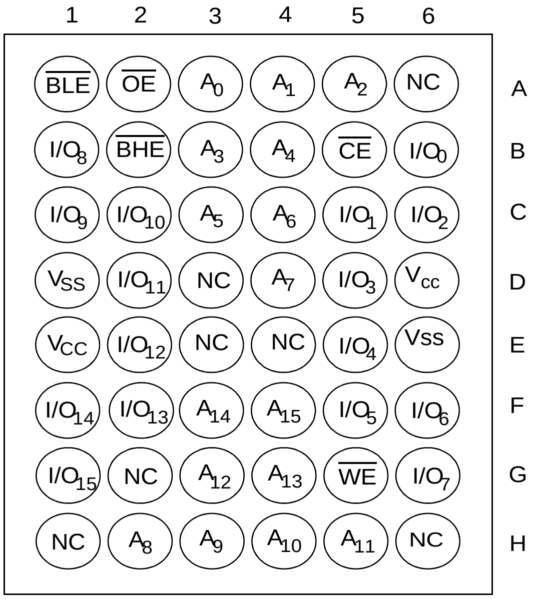


Figure 1. 48-ball VFBGA pinout (Top View)

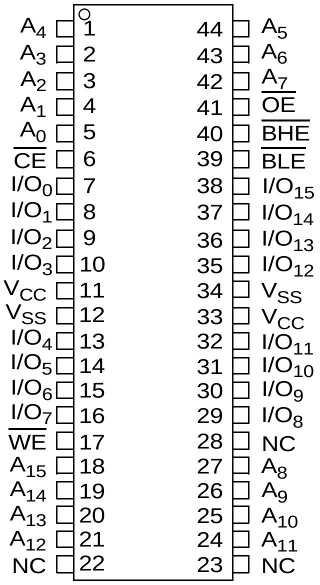


Figure 2. 44-pin TSOP II pinout (Top View) [1]

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating, I_{CC} (mA)				Standby, I_{SB2} (μA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62126EV30LL	Industrial	2.2	3.0	3.6	45	1.3	2	11	16	1	4
CY62126EV30LL	Automotive-A	2.2	3.0	3.6	45	1.3	2	11	16	1	4
CY62126EV30LL	Automotive-E	2.2	3.0	3.6	55	1.3	4	11	35	1	30

Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage to ground potential .... –0.3 V to 3.6 V (V_{CCmax} + 0.3 V)

DC voltage applied to outputs in High Z state [3, 4] .... –0.3 V to 3.6 V (V_{CCmax} + 0.3 V)

DC input voltage [3, 4] .... –0.3 V to 3.6 V (V_{CCmax} + 0.3 V)

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch up current .... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62126EV30LL	Industrial / Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V
	Automotive-E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial / Automotive-A)			55 ns (Automotive-E)			Unit
			Min	Typ[6]	Max	Min	Typ[6]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq 2.70$ V	2.4	–	–	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA	–	–	0.4	–		0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq 2.70$ V	–	–	0.4	–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V	1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V	2.2	–	V_{CC} + 0.3	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage	V_{CC} = 2.2 V to 2.7 V	–0.3	–	0.6	–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V	–0.3	–	0.8	–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$	–1	–	+1	–4	–	+4	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–1	–	+1	–4	–	+4	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CCmax}$ I_{OUT} = 0 mA CMOS levels	–	11	16	–	11	35	mA
		f = 1 MHz	–	1.3	2.0	–	1.3	4.0	
I_{SB1}[7]	Automatic CE power down current —CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V	–	1	4	–	1	35	µA
I_{SB2} [7]	Automatic CE power down current —CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, V_{CC} = 3.60 V	–	1	4	–	1	30	µA

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
7. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball VFBGA Package	44-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 4.25 × 1.125 inch, two-layer printed circuit board	58.85	28.2	°C/W
Θ_{JC}	Thermal resistance (junction to case)		17.01	3.4	°C/W

AC Test Loads and Waveforms

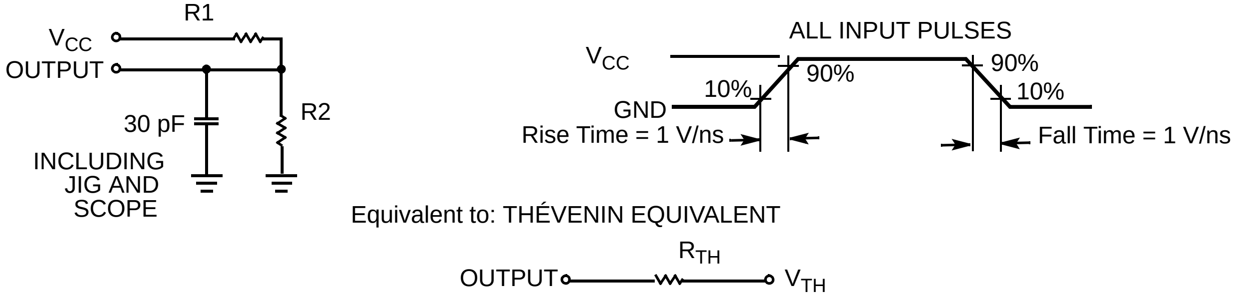


Figure 3. AC Test Loads and Waveforms

Parameters	2.2 V–2.7 V	2.7 V–3.6 V	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Note

8. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}[10]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial / Automotive-A	–	–	3	µA
			Automotive-E	–	–	30	µA
t_{CDR}[11]	Chip deselect to data retention time			0	–	–	ns
t_R[12]	Operation recovery time		CY62126EV30LL-45	45	–	–	ns
			CY62126EV30LL-55	55	–	–	

Data Retention Waveform

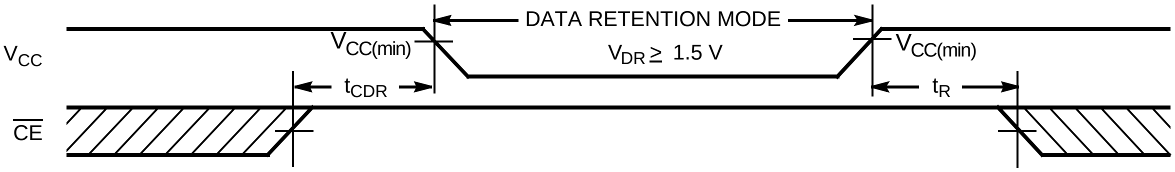


Figure 4. Data Retention Waveform

Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs.

Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45 ns (Industrial / Automotive-A)		55 ns (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [15]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [15, 16]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [15]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [15, 16]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	–	55	ns
t_{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to data valid	–	22	–	25	ns
t_{LZBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z [15]	5	–	5	–	ns
t_{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z [15, 16]	–	18	–	20	ns
Write Cycle [17, 18]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BHE}$ / $\overline{BLE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [15, 16]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [15]	10	–	10	–	ns

Notes

13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
14. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.
18. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

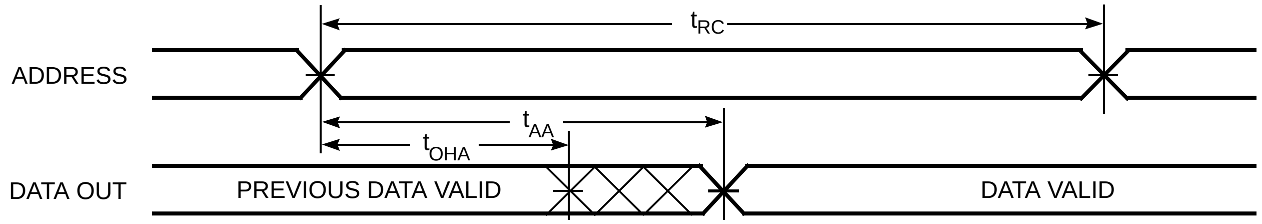


Figure 5. Read Cycle No. 1 (Address transition controlled) [19, 20]

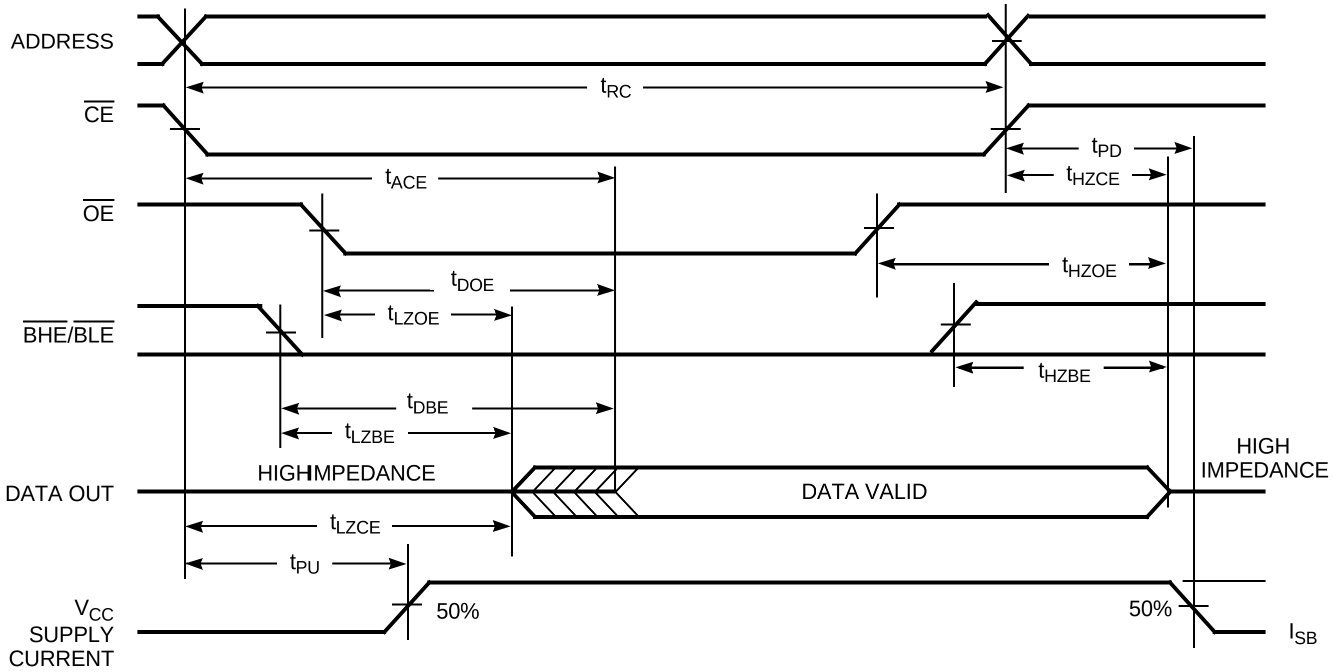


Figure 6. Read Cycle No. 2 (OE controlled) [20, 21]

Notes

[19] The device is continuously selected. OE, CE = V_{IL}, BHE, BLE, or both = V_{IL}.

[20] WE is high for read cycle.

[21] Address valid before or similar to CE and BHE, BLE transition LOW.

Switching Waveforms *(continued)*

Figure 7. Write Cycle No. 1 ($\overline{WE}$ controlled) [22, 23, 24]

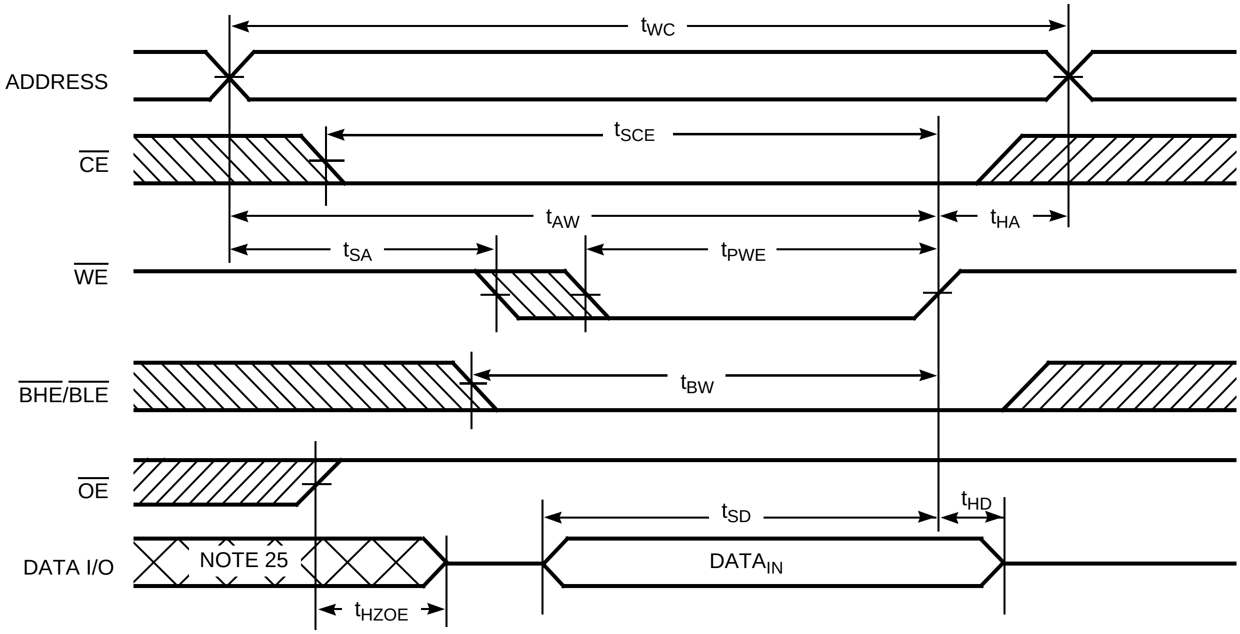
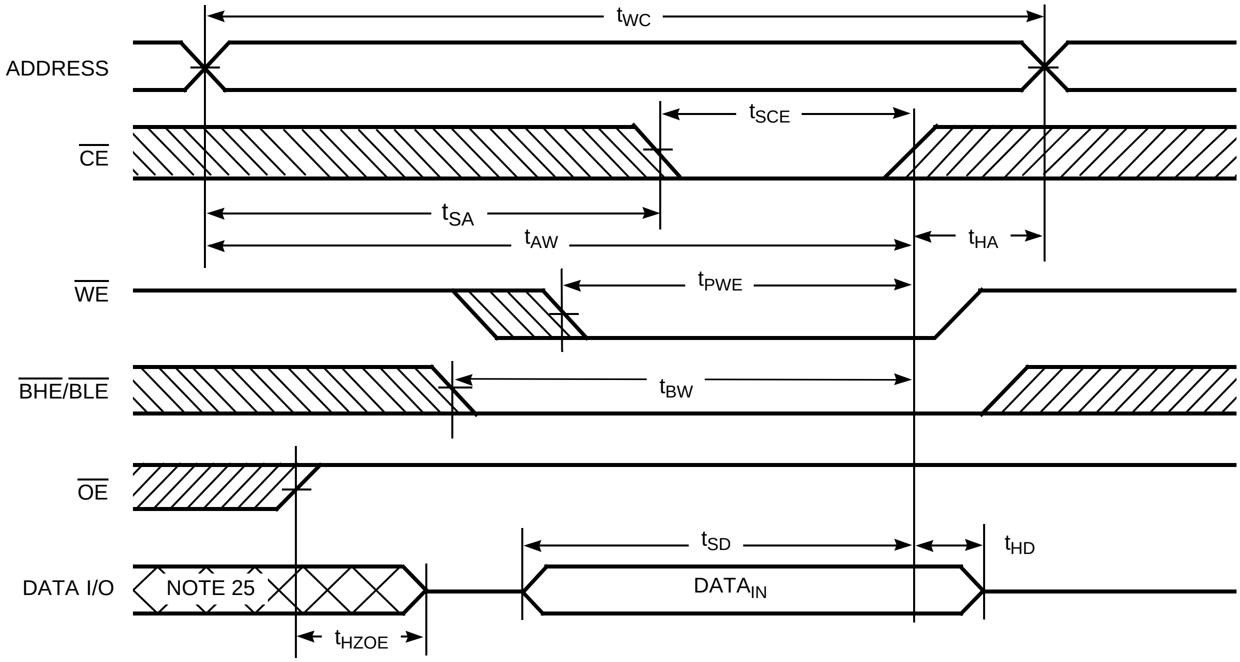


Figure 8. Write Cycle No. 2 ($\overline{CE}$ controlled) [22, 23, 24]



Notes

22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms *(continued)*

Figure 9. Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW [26, 27]

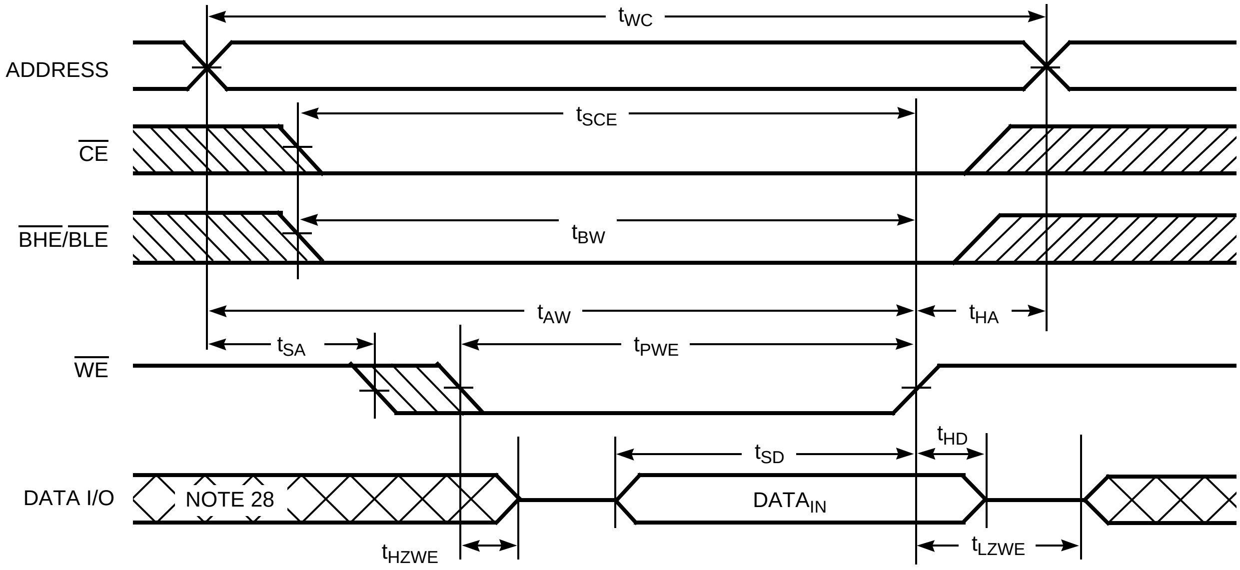
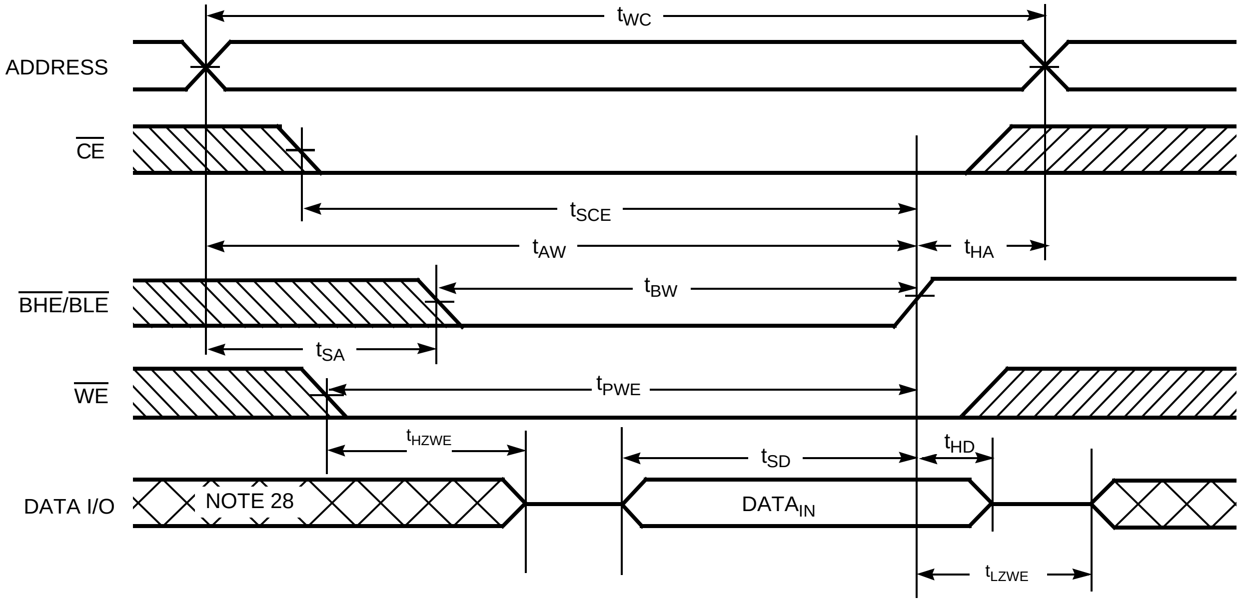


Figure 10. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ controlled, $\overline{OE}$ LOW) [26]



Notes

[26] If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.

[27] The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.

[28] During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}$[29]	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Note

[29] Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62126EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62126EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
	CY62126EV30LL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
55	CY62126EV30LL-55BVXE	51-85150	48-ball VFBGA (Pb-free)	Automotive-E
	CY62126EV30LL-55ZSXE	51-85087	44-pin TSOP II (Pb-free)	Automotive-E

Contact your local Cypress sales representative for availability of other parts.

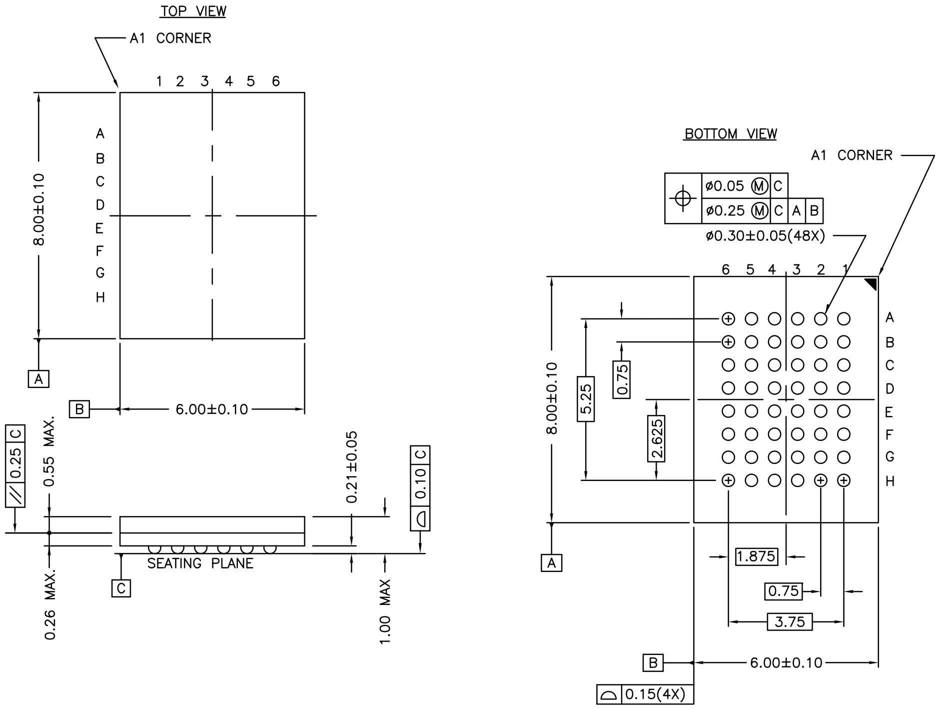
Ordering Code Definitions

CY 621 2 6 E V30 LL - XX XX X X

Temperature Range: X = I or A or E
I = Industrial; A = Automotive-A; E = Automotive-E
Pb-free
Package Type: XX = BV or ZS
BV = 48-ball VFBGA
ZS = 44-pin TSOP II
Speed Grade: XX = 45 ns or 55 ns
LL = Low Power
Voltage: V30 = 3 V Typical
Process Technology: E = 90 nm
Bus Width: 6 = × 16
Density: 2 = 1-Mbit
Family Code: 621= MoBL SRAM family
Company ID: CY = Cypress

Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



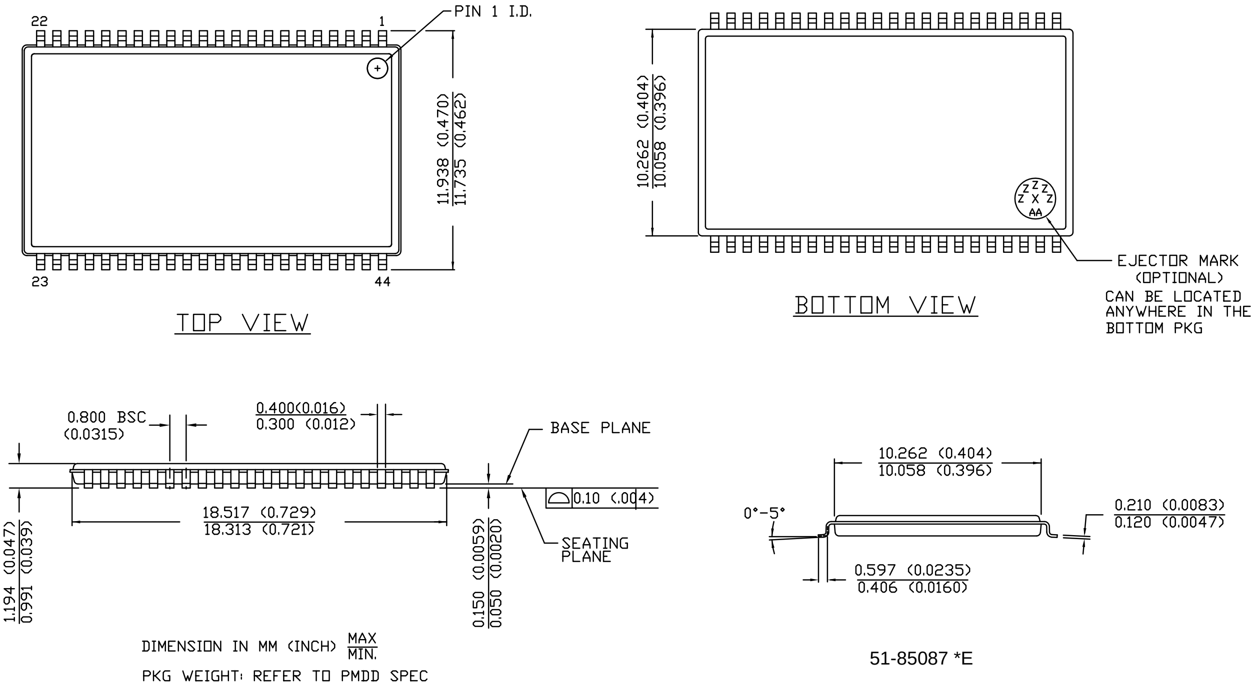
NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams *(continued)*

Figure 12. 44-pin TSOP II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62126EV30 MoBL®, 1-Mbit (64 K × 16) Static RAM **Document Number: 38-05486**				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	202760	See ECN	AJU	New data sheet.
*A	300835	See ECN	SYT	Converted from Advance Information to Preliminary Specified Typical standby power in the Features Section Changed E3 ball from DNU to NC in the Pin Configuration for the FBGA Package and removed the footnote associated with it on page #2 Changed t_{OHA} from 6 ns to 10 ns for both 35- and 45-ns speed bins, respectively Changed t_{DOE}, t_{SD} from 15 to 18 ns for 35-ns speed bin Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 and 15 ns to 15 and 18 ns for the 35 ns and 45 ns speed bins, respectively Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for the 35- and 45-ns speed bins, respectively Changed t_{SCE},t_{BW} from 25 and 40 ns to 30 and 35 ns for the 35- and 45-ns speed bins, respectively Changed t_{AW} from 25 to 30 ns and 40 to 35 ns for 35 and 45-ns speed bins respectively Changed t_{DBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Removed footnote that read “$\overline{\text{BHE}}$.$\overline{\text{BLE}}$ is the AND of both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$” on page # 4 Removed footnote that read “If both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are toggled together, then t_{LZBE} is 10 ns” on page # 5 Added Pb-free package information
*B	461631	See ECN	NXR	Converted from Preliminary to Final Removed 35 ns Speed Bin Removed “L” version of CY62126EV30 Changed $I_{CC\ (Typ)}$ from 8 mA to 11 mA and $I_{CC\ (max)}$ from 12 mA to 16 mA for $f = f_{max}$ Changed $I_{CC\ (max)}$ from 1.5 mA to 2.0 mA for f = 1 MHz, I_{SB1}, $I_{SB2\ (max)}$ from 1 µA to 4 µA, I_{SB1}, $I_{SB2\ (Typ)}$ from 0.5 µA to 1 µA, $I_{CCDR\ (max)}$ from 1.5 µA to 3 µA, AC Test load Capacitance value from 50 pF to 30 pF, t_{LZOE} from 3 to 5 ns, t_{LZCE} from 6 to 10 ns, t_{HZCE} from 22 to 18 ns, t_{LZBE} from 6 to 5 ns, t_{PWE} from 30 to 35 ns, t_{SD} from 22 to 25 ns, t_{LZWE} from 6 to 10 ns, and updated the Ordering Information table.
*C	925501	See ECN	VKN	Added footnote #7 related to I_{SB2} and I_{CCDR} Added footnote #11 related AC timing parameters
*D	1045260	See ECN	VKN	Added Automotive information Updated Ordering Information table
*E	2631771	01/07/09	NXR / PYRS	Changed $\overline{\text{CE}}$ condition from X to L in Truth table for Output Disable mode Updated template
*F	2944332	06/04/2010	VKN	Added Contents Removed byte enable from footnote #2 in Electrical Characteristics Added footnote related to chip enable in Truth Table Updated Package Diagrams Updated links in Sales, Solutions, and Legal Information
*G	2996166	07/29/2010	AJU	Added CY62126EV30LL-45ZSXA part in Ordering Information. Added Ordering Code Definitions. Modified table footnote format.
*H	3113864	12/17/2010	PRAS	Updated Figure 1 and Package Diagram, and fixed Typo in Figure 3.

Document History Page *(continued)*

Document Title: CY62126EV30 MoBL®, 1-Mbit (64 K × 16) Static RAM
Document Number: 38-05486

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*I	3270487	05/31/2011	RAME	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Electrical Characteristics. Updated Data Retention Characteristics. Added Acronyms and Units of Measure. Updated in new template.
*J	4205722	11/29/2013	MEMJ	Updated Features: Added Automotive-A range information. Updated Product Portfolio: Added Automotive-A range information. Updated Operating Range: Segregated Automotive-A and Automotive-E ranges. Updated Electrical Characteristics: Added Automotive-A with Industrial for 45 ns speed bin. Renamed Automotive as Automotive-E for 55 ns speed bin. Updated Data Retention Characteristics: Segregated Automotive-A and Automotive-E in conditions for I_{CCDR} parameter. Updated Switching Characteristics: Added Automotive-A with Industrial for 45 ns speed bin. Renamed Automotive as Automotive-E for 55 ns speed bin. Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E. Updated in new template.
*K	4211675	12/12/2013	MEMJ	No technical updates. Removed the border lines in Package Diagram specs.
*L	4410948	06/17/2014	VINI	Updated Switching Characteristics: Added Note 18 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 27 and referred the same note in Figure 9. Completing Sunset Review.

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