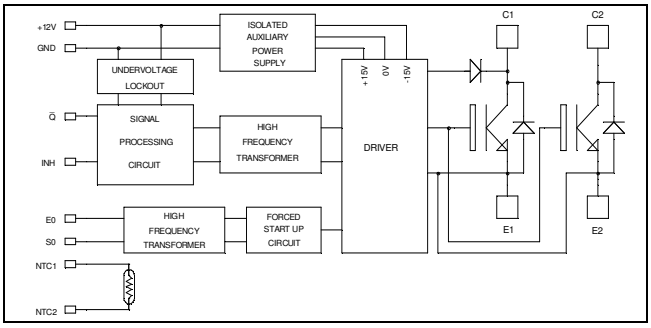
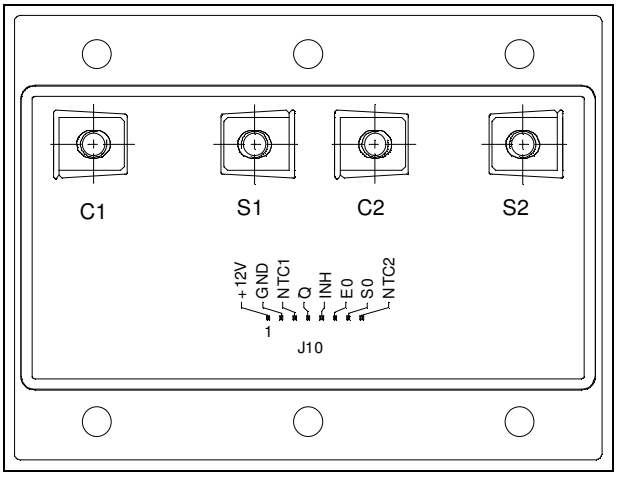
APTLGF280U120T

Zero Voltage switching Single switch NPT IGBT Power Module

V_{CES} = 1200V
I_C = 280A @ Tc = 80°C





Application

- Wide output range converters
- Induction heating
- X-Ray power supplies
- ZVS-PWM Uninterruptible Power Supplies
- High frequency, high density, high efficiency power supplies
- Welder

Features

- Integrated power and driver circuits
- Integrated DC/DC converter
- 80kHz switching frequency without high switching losses using ZVS technique
- low EMI and RFI
- isolated input signals
- Very low stray inductance
- Internal thermistor for temperature monitoring
- High level of integration

Benefits

- Outstanding performance at high frequency operation
- Direct mounting to heatsink (isolated package)
- Low junction to case thermal resistance
- Solderable terminals for signal and M5 for power for easy PCB mounting

For all ratings, C1 & C2 are connected together, same for E1 & E2.

Absolute maximum ratings

Symbol	*Parameter*		*Max ratings*	*Unit*
V_{CE}	Collector - Emitter Breakdown Voltage		1200	V
I_C	Continuous Collector Current	T_C = 25°C	400	A
		T_C = 80°C	280	
I_{CM}	Pulsed Collector Current		800	
P_D	IGBT Total Power Dissipation	T_C = 25°C	1900	W
	Diode Total Power Dissipation	T_C = 25°C	1040	
$F_{S(Max)}$	Maximum Operating Frequency		80	kHz
V_{AUX}	Isolated Auxiliary Power Supply Voltage		13	V
Q, $\overline{Q}$	Input Signal Voltage		13.6	

CAUTION: These Devices are sensitive to Electrostatic Discharge. Proper Handing Procedures Should Be Followed.

Static Electrical Characteristics

Symbol	Characteristic	Test Conditions		Min	Typ	Max	Unit
BV_{CES}	Collector Emitter Breakdown Voltage	Ic=2mA		1200			V
$V_{CE(on)}$	Collector Emitter on Voltage	Q or $\overline{Q}$ High I_C = 400A	T_j = 25°C		2.7	3.2	V
			T_j = 125°C		3.3	3.9	
I_{CES}	Zero Gate Voltage Collector Current	V_{CC} = 800V, V_{GE} = 0V				3000	µA

Dynamic Electrical Characteristics

Symbol	Characteristic	Test Conditions		Min	Typ	Max	Unit
C_{oes}	Output Capacitance	Q or $\overline{Q}$ = 0V V_{CE} = 25V, f = 1MHz			3680		pF
C_{res}	Reverse Transfer Capacitance				1760		
E_0-S_0	Forced Startup Voltage Level	See figures 8, 9 & 11		10		12	V
$P_W(E_0$-$S_0)$	Forced Startup Pulse Width	See figures 8 & 9		1		4	µs
INH	Inhibit Voltage Level (Active Level)	See figures 4 & 10		-0.6		1	V
E_{off}	Turn-off Switching Energy	V_{CC} = 600V I_C = 400A	T_j = 25°C		31		mJ
			T_j = 125°C		34		
		V_{CC} = 600V I_C = 200A	T_j = 25°C		15.5		
			T_j = 125°C		17		

Freewheeling Diode Characteristics

Symbol	Characteristic	Test Conditions		Min	Typ	Max	Unit
V_{RRM}	Max. Peak Repetitive Reverse Voltage			1200			V
V_F	Diode Forward Voltage	I_F = 400A				2.5	
		I_F = 800A			2.7		
		I_F = 400A	T_j = 150°C			2.0	
$I_{F(av)}$	Maximum Average Forward Current	Duty cycle=50%	T_C = 60°C		400		A
t_{rr}	Reverse Recovery Time	I_F = 400A V_R = 650V di/dt=800A/µs	T_j = 25°C		70		ns
			T_j = 100°C		130		
Q_{rr}	Reverse recovery Charge	I_F = 400A V_R = 650V di/dt=800A/µs	T_j = 25°C		5		µC
			T_j = 100°C		14.6		

Driver Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{AUX}	Isolated Auxiliary Power Supply Voltage		11	12	13	V
I_{AUX}	Isolated Auxiliary Power Supply Current				1.5	A
Q, $\overline{Q}$	Blocking Signal Input Voltage	Low level	-0.6		1	V
		High level	10		13.6	
IQ, $I\overline{Q}$	Blocking Signal Input Current				5	mA
$T_{d(on)}$	Turn-on Delay Time	See figure 5		500		ns
$T_{d(off)}$	Turn-off Delay Time	See figure 4		500		ns

Thermal and package characteristics

Symbol	Characteristic			Min	Typ	Max	Unit
R_{thJC}	Junction to Case		IGBT			0.065	°C/W
			Diode			0.12	
V_{ISOL}	RMS Isolation Voltage, any terminal to case t =1 min, I isol<1mA, 50/60Hz			2500			V
T_J	Operating junction temperature range			-40		150	°C
T_{STG}	Storage Temperature Range			-40		125	
T_C	Operating Case Temperature			-40		100	
Torque	Mounting torque	To heatsink	M5	2		3.5	N.m
		For terminals	M5	2		3.5	
Wt	Package Weight					470	g

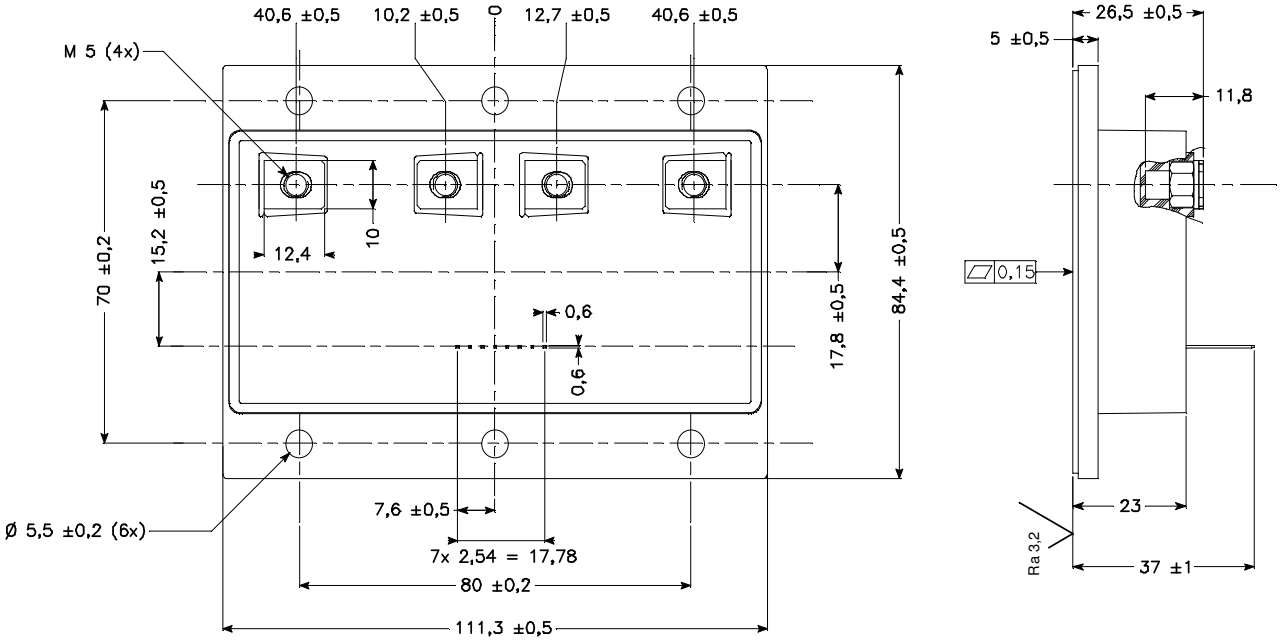
Temperature sensor NTC

Symbol	Characteristic	Min	Typ	Max	Unit
R_{25}	Resistance @ 25°C		68		kΩ
$B_{25/85}$	T_{25} = 298.16 K		4080		K

$$R_T = \frac{R_{25}}{\exp\left[B_{25/85}\left(\frac{1}{T_{25}} - \frac{1}{T}\right)\right]}$$

T: Thermistor temperature
R_T: Thermistor value at T

Package outline



NTC Characteristics

R@25°C = 68kΩ ±5%

Temperature (°C)	R(T)/R@25°C	Tolerance (%)
-30	19,33	10,9
-25	14,12	9,1
-20	10,41	7,5
-15	7,758	6,1
-10	5,834	4,9
-5	4,426	3,8
0	3,387	2,9
5	2,614	2,1
10	2,033	1,4
15	1,593	0,9
20	1,258	0,4
25	1	0
30	0,8004	0,4
35	0,6448	0,8
40	0,5228	1,3
45	0,4264	1,8
50	0,3497	2,3
55	0,2885	2,9
60	0,2392	3,5
65	0,1994	4,1
70	0,1671	4,8
75	0,1406	5,5
80	0,1189	6,2
85	0,101	6,9
90	0,08617	7,6
95	0,07381	8,3
100	0,06347	9,1
105	0,0548	9,8
110	0,04748	10,6
115	0,04129	11,3
120	0,03603	12,1
125	0,03155	12,9

Table 1, NTC Characteristics

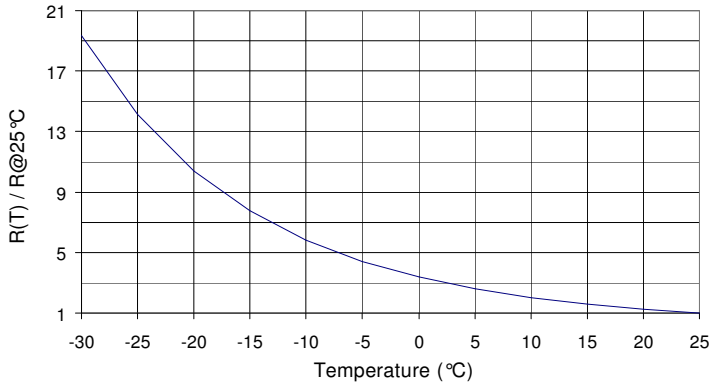


Figure 1, Normalized NTC Characteristics -30°C to 25°C

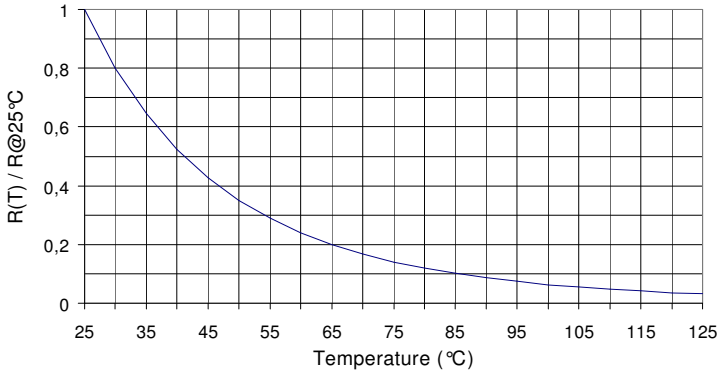


Figure 2, Normalized NTC Characteristics 25°C to 125°C

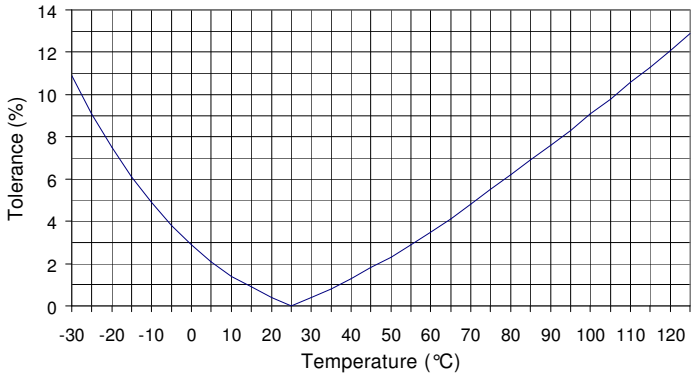
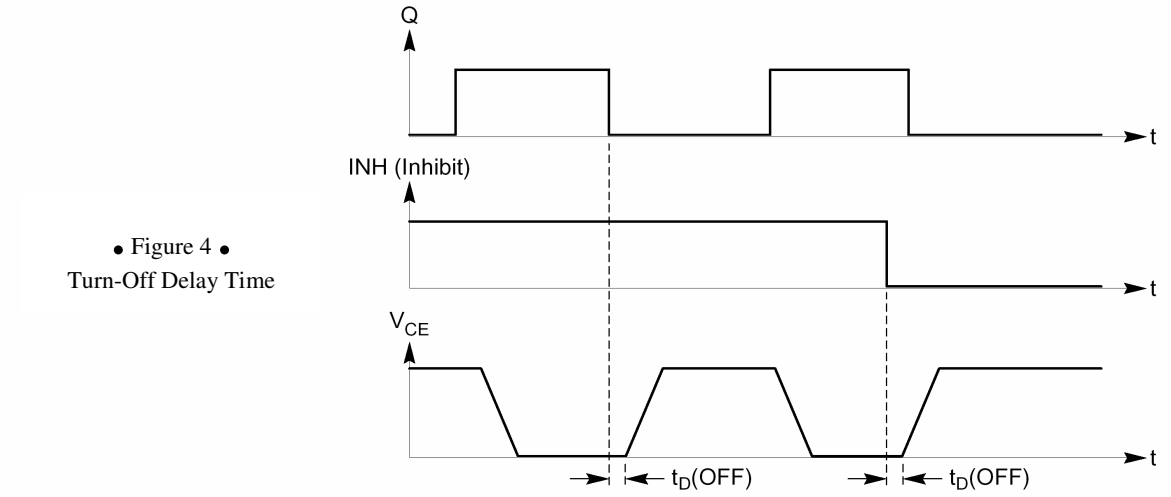
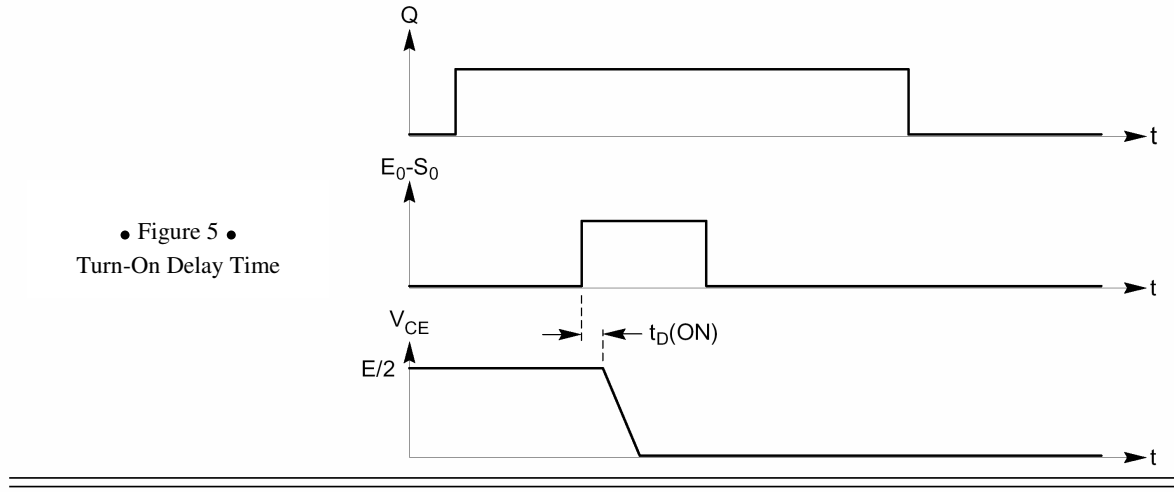


Figure 3, NTC Tolerance vs Temperature



• Figure 4 •
Turn-Off Delay Time



• Figure 5 •
Turn-On Delay Time

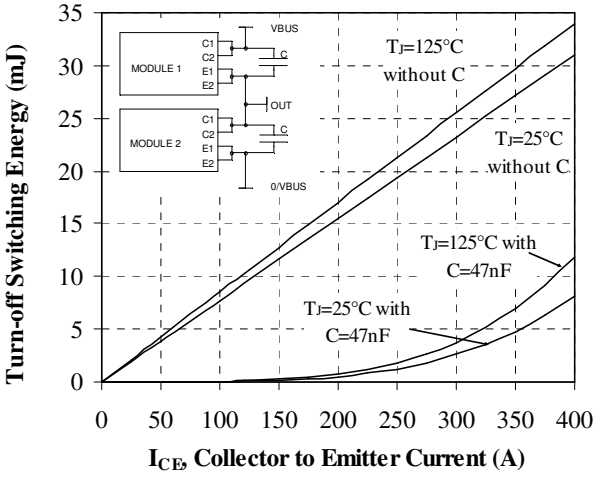


Figure 6: Turn-Off Energy losses vs Collector Current

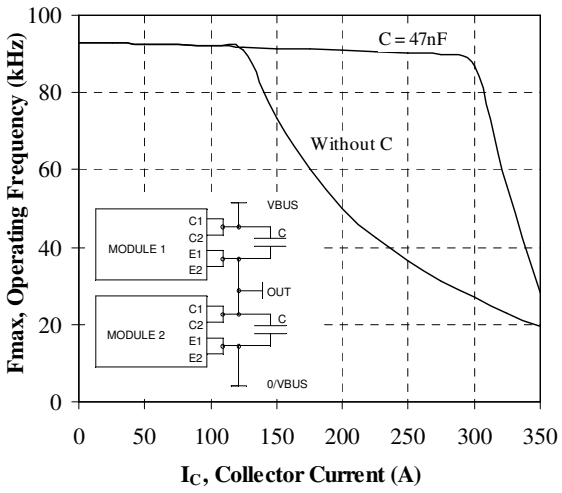
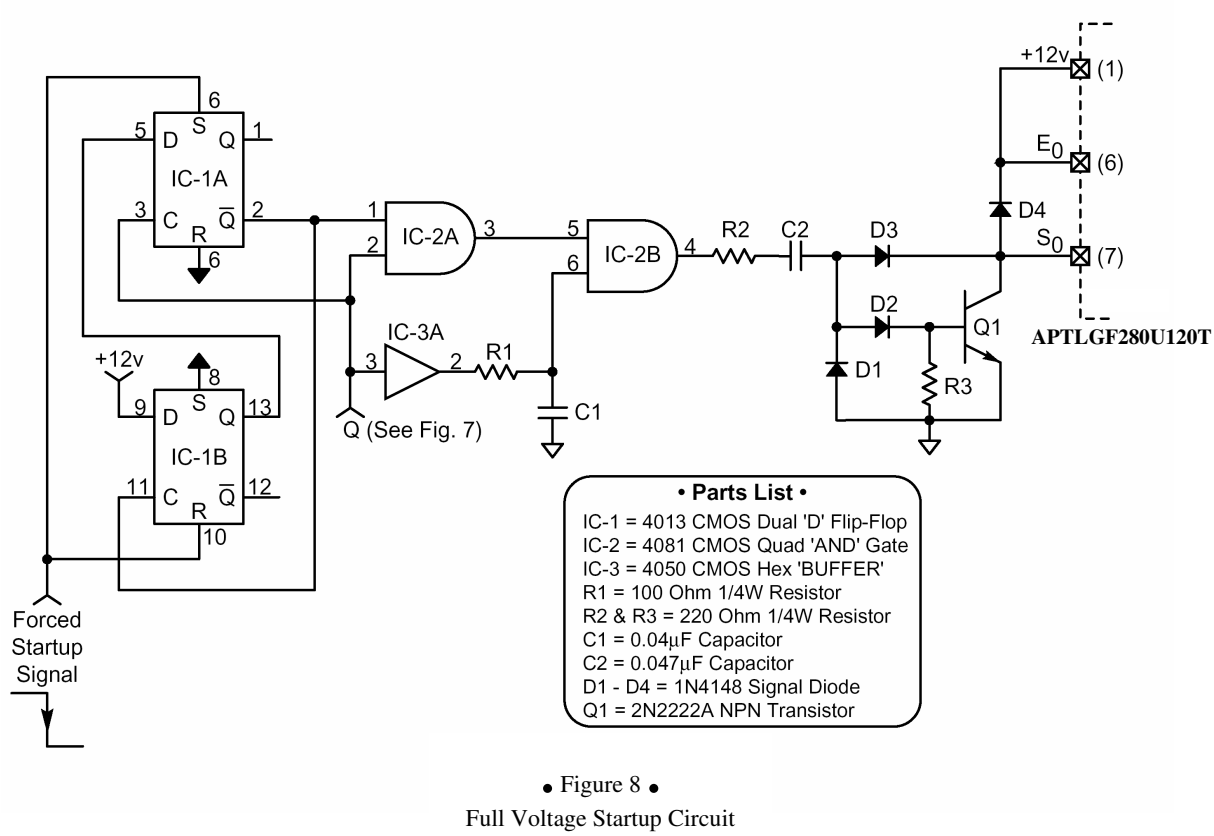


Figure 7: Operating Frequency vs Collector Current

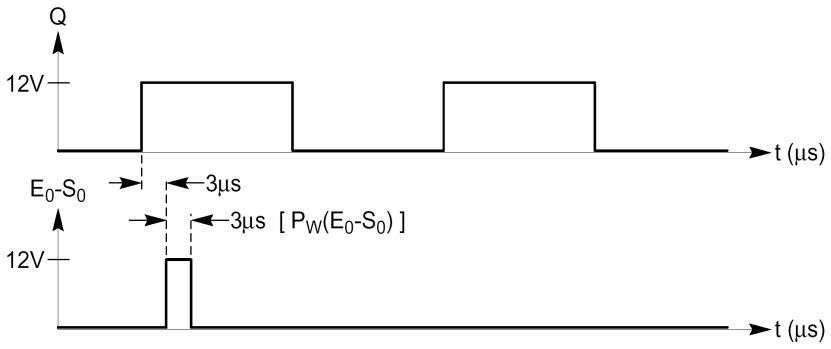


• Figure 8 •
Full Voltage Startup Circuit

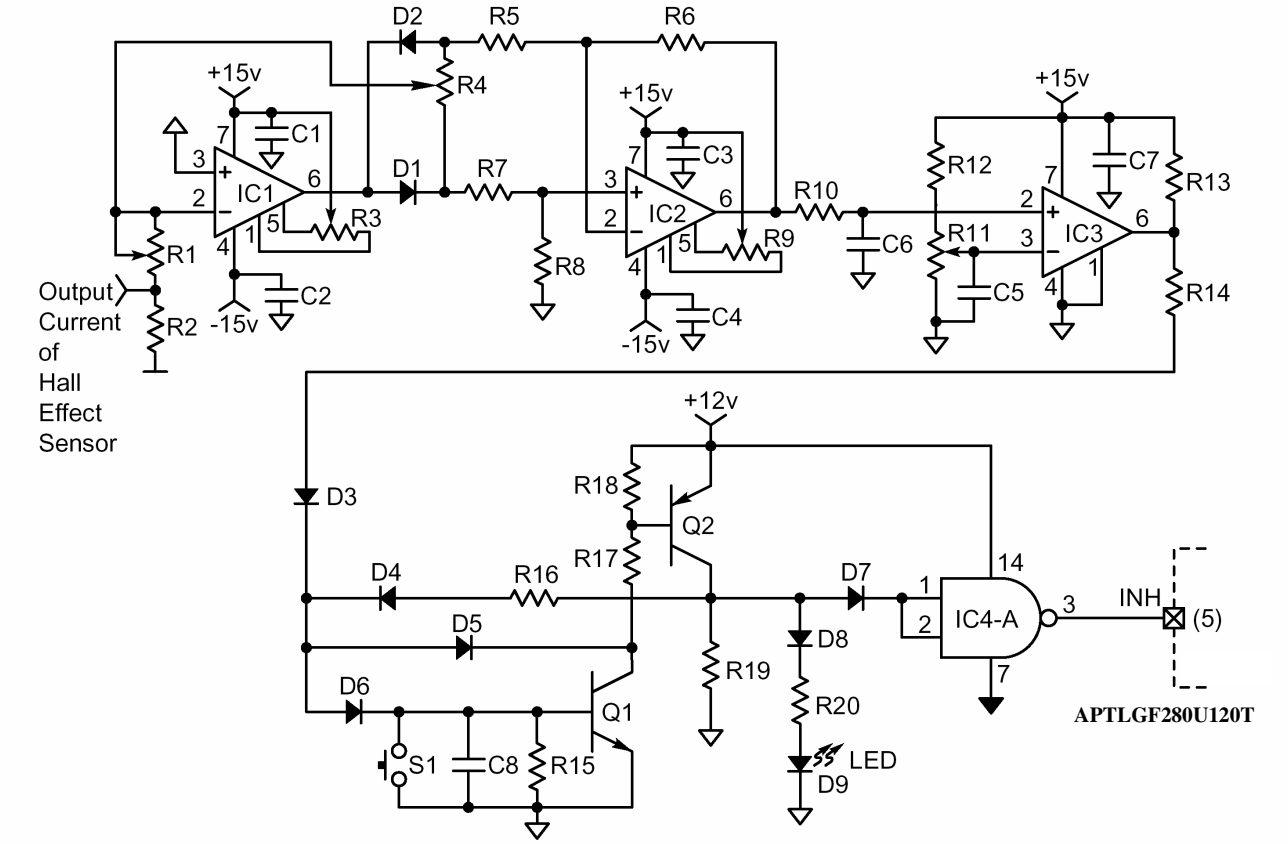
• After power is applied and/or after an inhibit (INH) signal (active low) has been applied and removed, the APTLGF280U120T module requires a forced startup signal between E_0-S_0, forcing startup under full voltage conditions. The forced startup signal must be a single pulse and cannot be repeated with a frequency greater than 1 kHz. The duration of this pulse must be between 1 & 4µsec and must be synchronized with input signal Q being high. The startup timing diagram is shown in figure 9.

• The circuit, shown in figure 8 is proposed as an example for generating the startup pulse for inputs E0 and S0. The signal is initiated by the falling edge of a voltage applied to the forced startup signal input. The circuit will synchronize the forced startup signal with Q and forcing the upper switch to turn ON.

• The startup signal, between E_0-S_0, may also be implemented by a negative pulse synchronized with input signal Q being low and forcing the lower switch to turn ON. Examples of both startup sequences being used in the startup of a full – bridge configuration is shown in figure 11.



• Figure 9 •
Startup Pulse
Timing Diagram



• Parts List •

IC-1 & 2 = LF-355 JFET Op Amp	R3 & R9 = 22K Ohm Trim Pot.	R18 = 330 Ohm 1/4W Resistor
IC-3 = LM-311Voltage Comparator	R2 & R3 = 47K Ohm 1/4W Resistor	R19 = 22K Ohm 1/4W Resistor
IC-4 = 4011 CMOS Quad 'NAND' Gate	R5 - R8 = 220 Ohm 1/4W Resistor	R20 = 820 Ohm 1/4W Resistor
D1 - D8 = 1N4148 Signal Diode	R10 = 2.2K Ohm 1/4W Resistor	C1 - C4; C6 & C7 = 0.1µF Capacitor
Q1 = BC237 NPN Transistor	R12 = 4.7K Ohm 1/4W Resistor	C5 = 10pF Capacitor
Q2 = BC307 PNP Transistor	R13 & R16 = 10K Ohm 1/4W Resistor	C8 = 33pF Capacitor
R1, R4 & R11 = 10K Ohm Trim Pot.	R14 & R17 = 1K Ohm 1/4W Resistor	
R2 = 100 Ohm 1/4W Resistor	R15 = 3.3K Ohm 1/4W Resistor	

Figure 10: Inhibit Circuit for APTLGF280U120T

- The APTLGF280U120T modules can be protected against over currents by the inhibit circuit shown above.
- This circuit can be implemented by one of several functions:
  - Output current measurement with Hall sensor.
  - Rectification of the measured value without offset.
  - Comparison of this value to a reference value (inhibit level fixed by potentiometer).
  - Memorization of the inhibit order.
  - Inhibit signal adaption.
- When the inhibit order is given, the default is latched and the output of the circuit connected to the INH (pin5) input of the APTLGF280U120T module switches to a low level (the active level for INH). Then the LED (D9) illuminates.
- Pushbutton switch (S1) provides a source for the re-initialization of the Inhibit circuit.

For more information see APT9904 and APT9601 application notes.

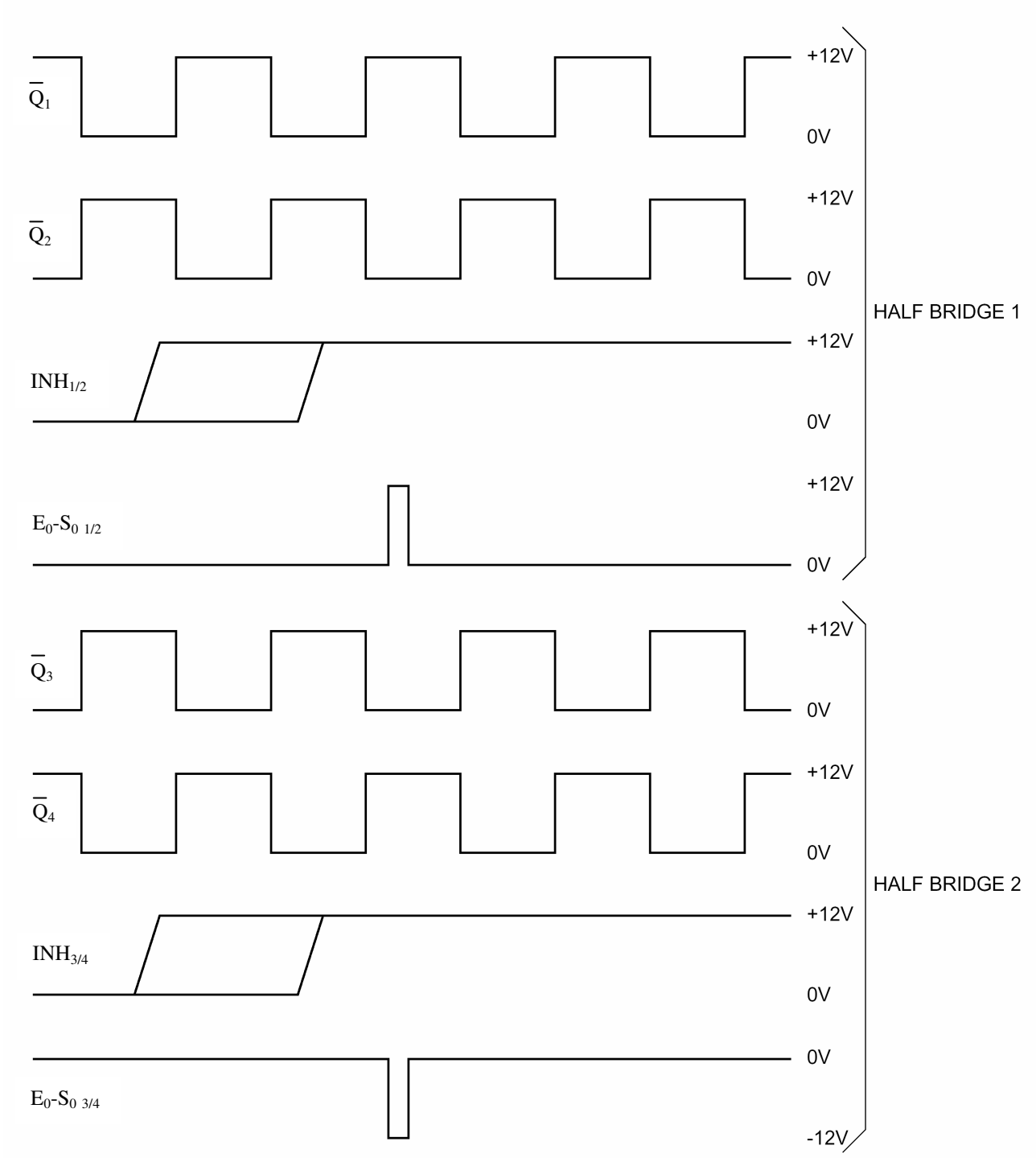


Figure 11: example of input signal for 4 x APTLGF280U120T modules connected in a Full Bridge configuration