

# AN6366NK, AN6366NS

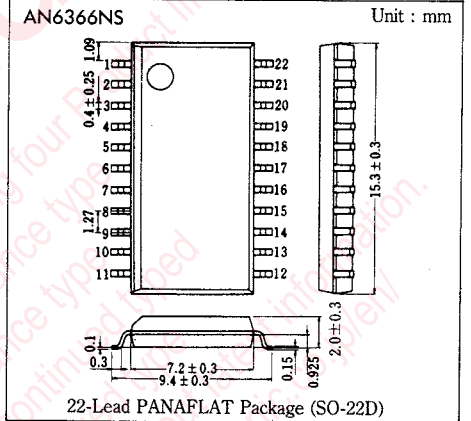
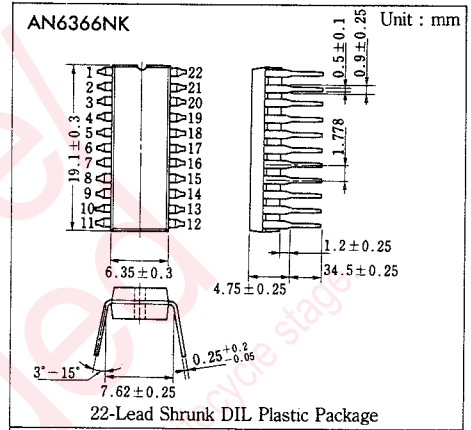
## VTR Color Signal Processing Circuits for NTSC System

### ■ Outline

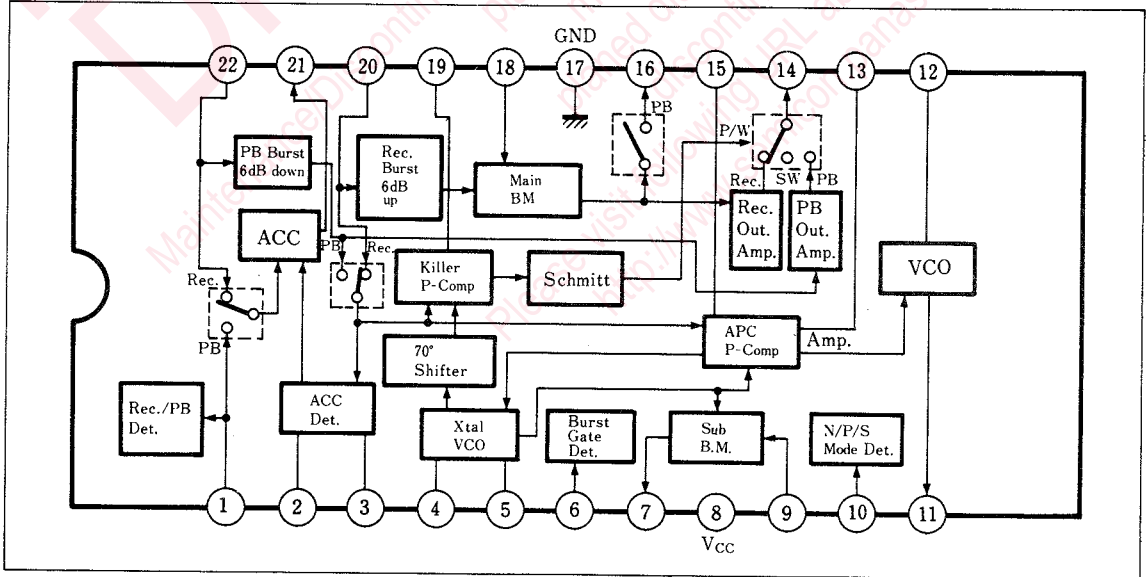
The AN6366NK and The AN6366NS by combining with the MN6163A, are integrated circuits provided with the function which processes VTR color signals matching each mode of 2H/4H/6H in the NTSC system.

### ■ Features

- Operated by low supply voltage :  $V_{cc}=5V$
- Low power consumption(110mW)
- AFC+APC system during recording mode Only APC system during playback mode
- Better S/N ratio by chroma ACC(2H/6Hmode)



### ■ Block Diagram



■ Absolute Maximum Ratings (T<sub>a</sub>=25°C)

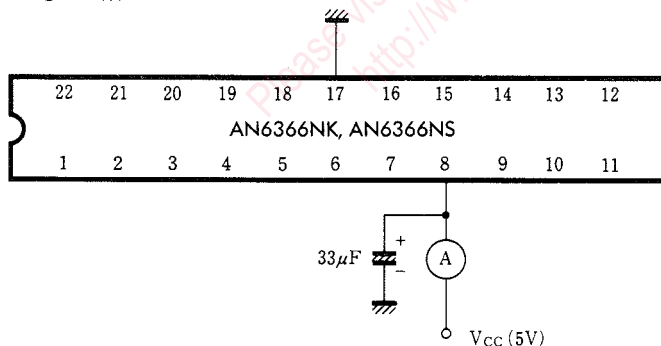
Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	6	V
Power dissipation (T <sub>a</sub> =70°C)	P <sub>D</sub>	250	mW
Operating ambient temperature	T <sub>opr</sub>	-20~+70	°C
Storage temperature	T <sub>stg</sub>	-40~+150	°C

■ Electrical Characteristics (T<sub>a</sub>=25°C)

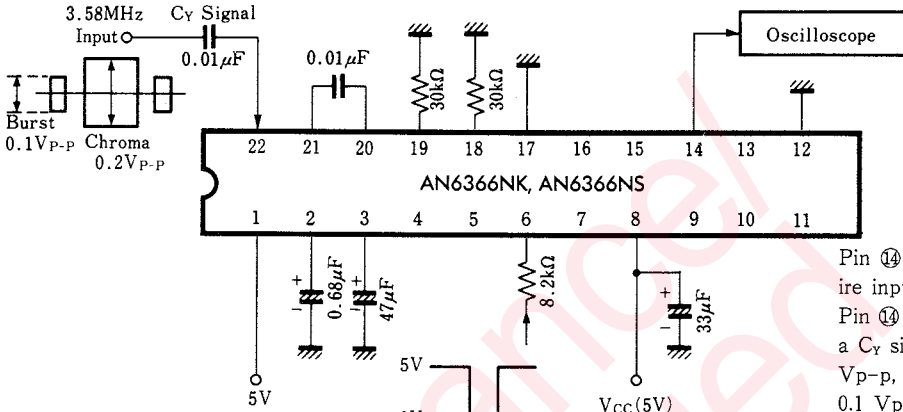
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total circuit current	I <sub>tot</sub>	1	V <sub>CC</sub> =5V	15		32	mA
REC output amplitude (Burst ACC)	v <sub>O14-R</sub>	2	V <sub>CC</sub> =5V, Pin ② Input Burst 0.1V <sub>P-P</sub>	0.5		1.2	V <sub>P-P</sub>
REC ACC control sensitivity (Burst ACC)	β <sub>AGC-B</sub>	2	V <sub>CC</sub> =5V, +6dB~-15dB			3	dB
Chroma ACC	β <sub>AGC-C</sub>	2	V <sub>CC</sub> =5V	0.5		4.5	dB
Main BM amp. gain	G <sub>V-16</sub>	3	V <sub>CC</sub> =5V, Pin ⑩ Input 0.5V <sub>P-P</sub>	4		9	dB
Main BM carrier leak	CL <sub>16</sub>	4	V <sub>CC</sub> =5V			-33	dB
Burst emphasis amount	G <sub>E11</sub>	5	V <sub>CC</sub> =5V, Pin ⑩ Input 0.25V <sub>P-P</sub>	5		7	dB
REC current up rate	G <sub>REC</sub>	5	V <sub>CC</sub> =5V, Pin ⑩ Input 0.25V <sub>P-P</sub>	0.5		2.5	dB
PB output amplitude (2H)	v <sub>O14-P</sub>	6	V <sub>CC</sub> =5V, Pin ① Input 0.2V <sub>P-P</sub>	0.2		0.55	V <sub>P-P</sub>
Burst de-emphasis amount	G <sub>DE</sub>	6	V <sub>CC</sub> =5V, Pin ① Input 0.2V <sub>P-P</sub>	-6.5		-4.5	dB
PB/REC cross talk	CT <sub>14-P</sub>	7	V <sub>CC</sub> =5V			-40	dB
REC control voltage	S <sub>I-REC</sub>	7	V <sub>CC</sub> =5V	4.6			V
Sub BM amp. gain	G <sub>V-7</sub>	8	V <sub>CC</sub> =5V, Pin ⑨ Input 0.65V <sub>P-P</sub>	1		5	dB
Sub BM carrier leak	CL <sub>7</sub>	9	V <sub>CC</sub> =5V			-35	dB
Killer sensitivity (ON)	K <sub>gate1</sub>	10	V <sub>CC</sub> =5V, Pin ② Input 0dB=0.25V <sub>P-P</sub>	-22			dB
Killer sensitivity (OFF)	K <sub>gate2</sub>	10	V <sub>CC</sub> =5V, Pin ② Input 0dB=0.25V <sub>P-P</sub>			-10	dB
Killer output (LOW)	V <sub>14-L</sub>	10	V <sub>CC</sub> =5V			0.5	V
VCO FREE frequency	f <sub>OSC</sub>	11	V <sub>CC</sub> =5V	3		7	MHz
VCO control sensitivity	β <sub>2</sub>	11	V <sub>CC</sub> =5V	1.5		3.5	kHz/mV
VCO output amplitude	v <sub>O11</sub>	11	V <sub>CC</sub> =5V	0.4			V <sub>P-P</sub>
REC Pull in range (H)	f <sub>APC-H</sub>	12	V <sub>CC</sub> =5V	500			Hz
REC Pull-in range (L)	f <sub>APC-L</sub>	12	V <sub>CC</sub> =5V			-500	Hz
2H mode range	S <sub>10-1</sub>	13	V <sub>CC</sub> =5V			0.6	V
4H mode range	S <sub>10-2</sub>	13	V <sub>CC</sub> =5V	1.6		2	V
6H mode range	S <sub>10-3</sub>	13	V <sub>CC</sub> =5V	3.2		3.6	V

Note) Operating supply voltage: V<sub>CC(oper)</sub> = 4.5~5.5V

Test Circuit 1 (I<sub>tot</sub>)

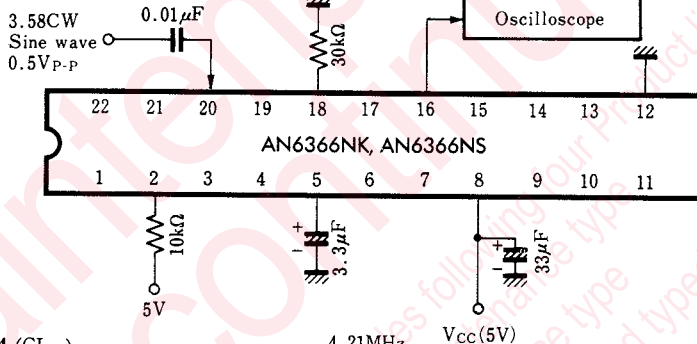


**Test Circuit 2** ( $v_{O14-R}$ ,  $\beta_{AGC-B}$ ,  $\beta_{AGC-C}$ )

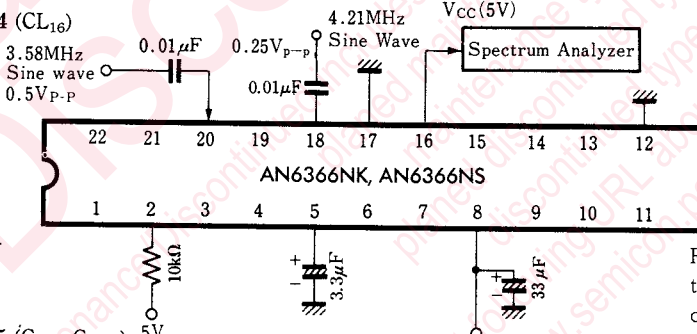


Pin ⑭ output ratio when entire input is +6 dB and -15 dB  
 Pin ⑭ Burst output ratio when a  $C_Y$  signal is 0.2 V<sub>p-p</sub> and O V<sub>p-p</sub>, with constant Burst of 0.1 V<sub>p-p</sub>

**Test Circuit 3** ( $G_{V-16}$ )

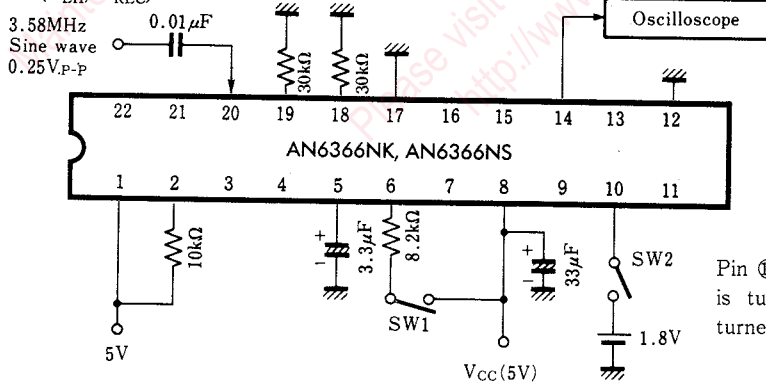


**Test Circuit 4** ( $CL_{16}$ )



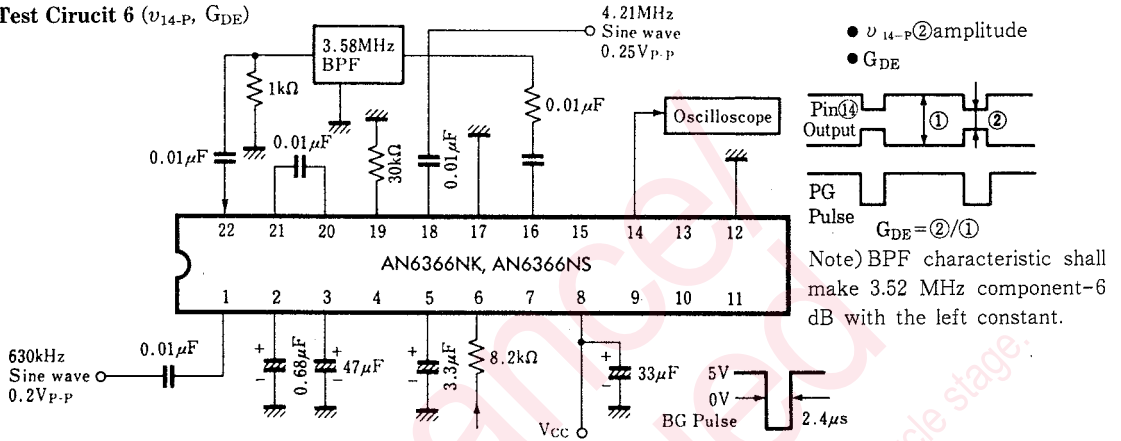
Ratio of 4.21 MHz component to Pin ⑭ 3.58 MHz output component

**Test Circuit 5** ( $G_{EH}$ ,  $G_{REC}$ )

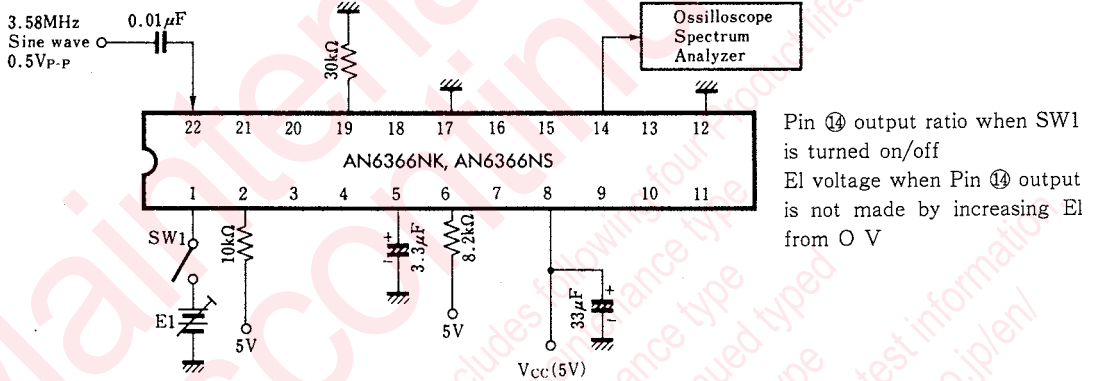


Pin ⑭ output ratio when SW1 is turned on/off with SW2 turned off

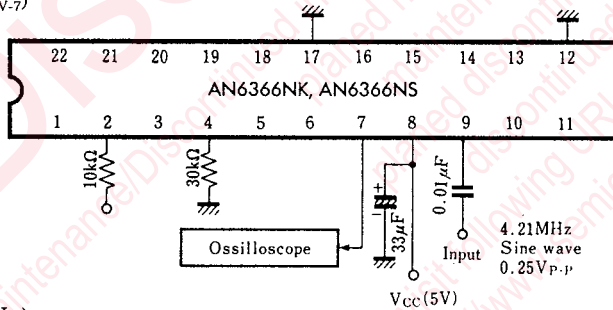
Test Circuit 6 ( $V_{14-P}$ ,  $G_{DE}$ )



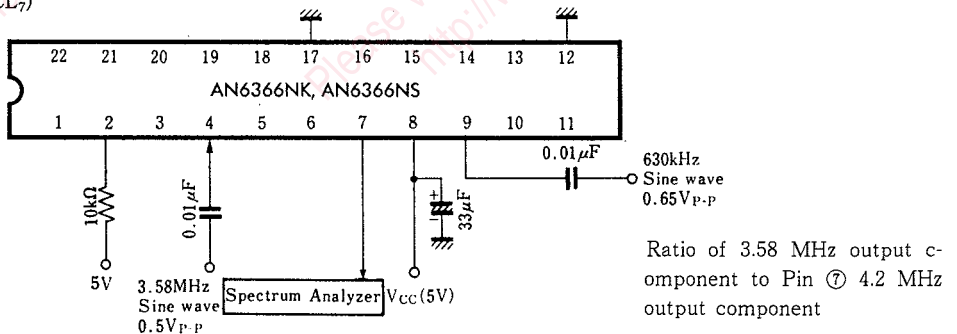
Test Circuit 7 ( $CT_{14-P}$ ,  $S_{1-REC}$ )



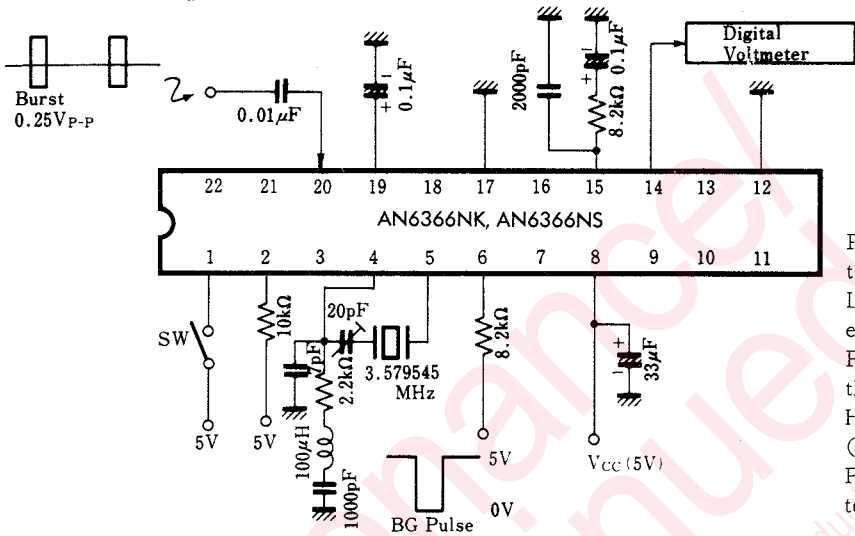
Test Circuit 8 ( $G_{V-7}$ )



Test Circuit 9 ( $CL_7$ )

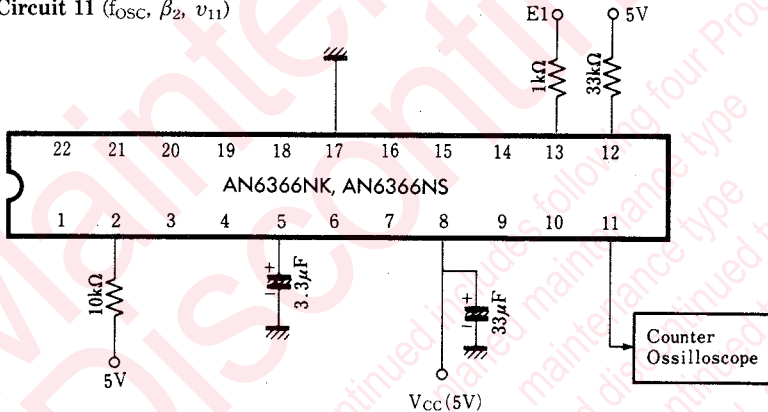


Test Circuit 10 ( $K_{gate1}$ ,  $K_{gate2}$ ,  $V_{14-L}$ )



Pin 20 Burst input level when the Pin 14 is turned from H to L by lowering the Pin 20 level (0.25 V<sub>p-p</sub> = 0 dB)  
 Pin 20 Burst input level when the Pin 14 is turned from L to H by raising the Pin 20 level (0.25 V<sub>p-p</sub> = 0 dB)  
 Pin 14 voltage in case of K gate2

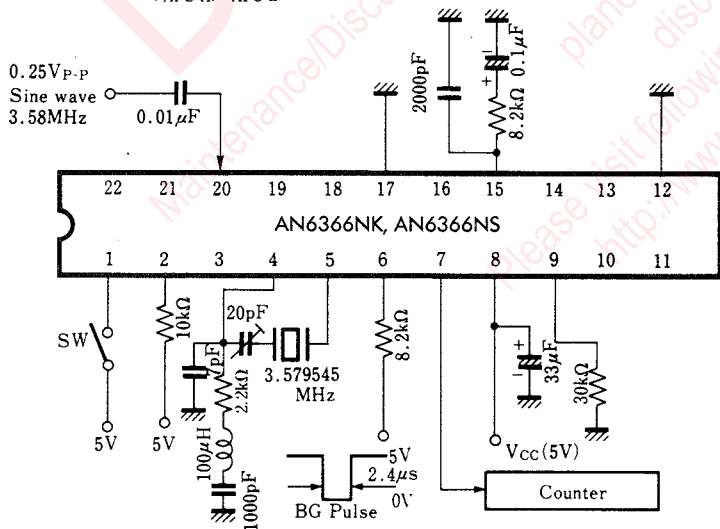
Test Circuit 11 ( $f_{osc}$ ,  $\beta_2$ ,  $v_{11}$ )



Assuming that output frequencies are  $f_1$  and  $f_2$  when  $E_1 = 2.4$  V and 2.6 V, respectively ;

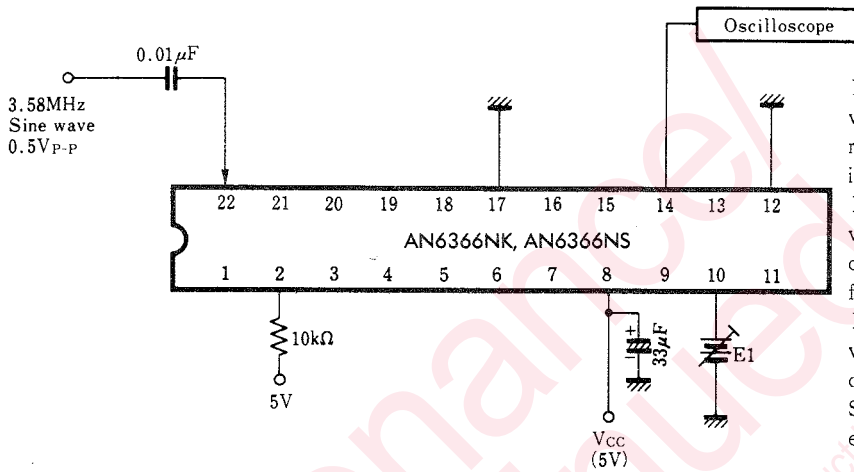


Test Circuit 12 ( $f_{APC-H}$ ,  $f_{APC-L}$ )



Frequency difference between a Pin 20 input frequency and 3.579545 MHz when the former is lowered from 3.581 MHz and a Pin 7 output frequency coincides with the former.  $f_{APC-H} = \text{Pin 20 frequency} - 3.579545$  MHz  
 Frequency difference between the Pin 20 input frequency and 3.579545 MHz when the former is raised 3.57 MHz and a Pin 7 output frequency coincides with the former.  $f_{APC-L} = \text{Pin 20 frequency} - 3.579545$  MHz

Test Circuit 13 (S<sub>10-1</sub>, S<sub>10-2</sub>, S<sub>10-3</sub>)

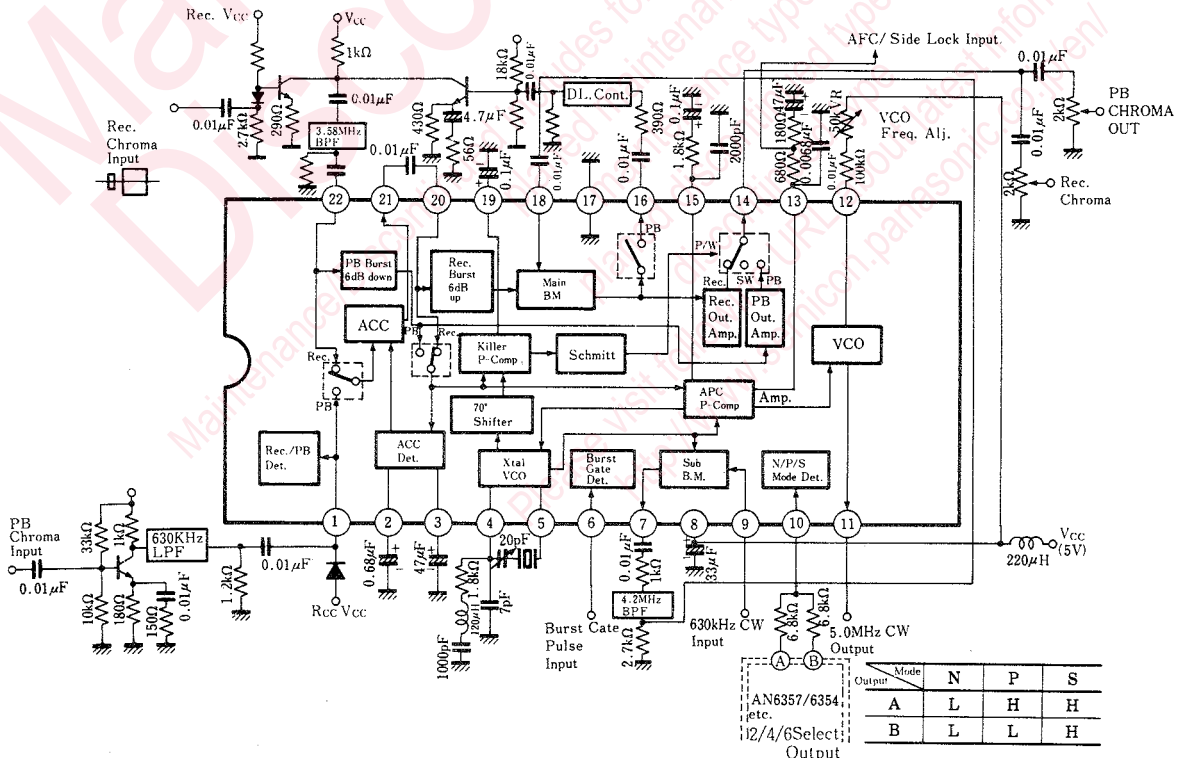


Pin ⑩ voltage range within which a ⑭ output level is raised up by about 6 dB by increasing E<sub>1</sub> from 0 V

Pin ⑩ voltage range within which an increase of about 6 dB is maintained, with E<sub>1</sub> further increased

Pin ⑩ voltage range within which ⑭ output maintains a decrease of about 6 dB from S<sub>10-2</sub>, with E<sub>1</sub> further increased

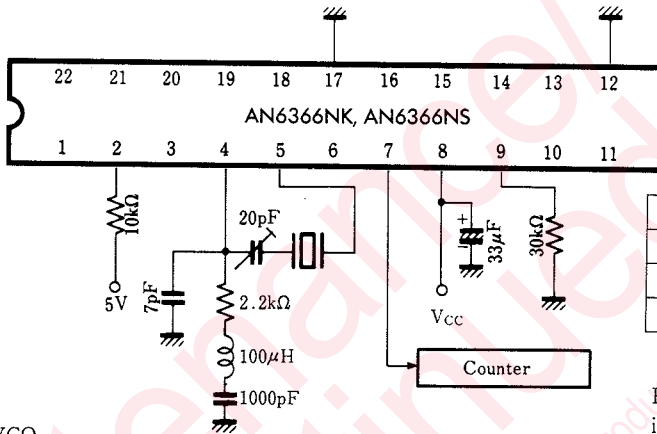
Application Circuit



Precautions for Use

- (i) Allowable power supply range : 4.5V to 5.5 V
- (ii) Adjusting X'tal VCO

In the PB mode, connect 30 kΩ between the Pin ⑨ and, GND, and adjust a trimmer so that a Pin ⑦ frequency will be 3.579545 MHz.

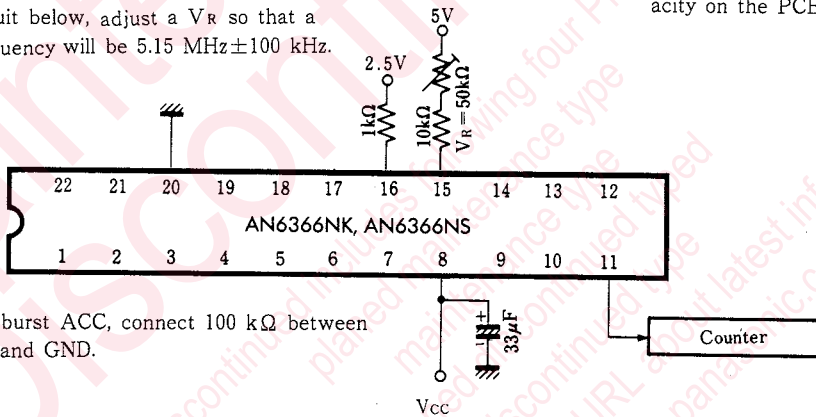


	NTSC	3 Systems
R	2.2kΩ	1.8kΩ
L	100 μF	47 μF
C	1000pF	1000pF

Note) For 7PF between the Pin ④ and GND, select taking into account an optimum capacity on the PCB, etc.

(iii) Adjusting VCO

In the circuit below, adjust a V<sub>R</sub> so that a pin ⑩ frequency will be 5.15 MHz ± 100 kHz.



(iv) For forced burst ACC, connect 100 kΩ between the Pin ③ and GND.

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	PB Chroma Input Rec. Changeover Input	12	VCO Frequency Adjustment
2	ACC Burst Det.	13	VOC Control Terminal
3	ACC Ref. Level	14	Chroma Output
4	X'tal Osc. Input	15	X'tal APC Control Terminal
5	X'tal Osc. Output	16	PB Main BM Output
6	Burst Gate Pulse Input	17	GND
7	Sub. BM Output	18	Main BM Input
8	V <sub>cc</sub>	19	Killer Control Terminal
9	Sub BM Input	20	ACC Input
10	2H/4H/6H Mode Selective Input	21	ACC Output
11	VCO Output	22	3.58MHz Chroma Input



## Request for your special attention and precautions in using the technical information and semiconductors described in this book

- (1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.
- (2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.
- (3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).  
Consult our sales staff in advance for information on the following applications:
  - Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
- (4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
  - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
- (7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.