SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

EASY APPLICATION DESIGN WITH THE L4970A, MONOLITHIC DC-DC CONVERTERS FAMILY

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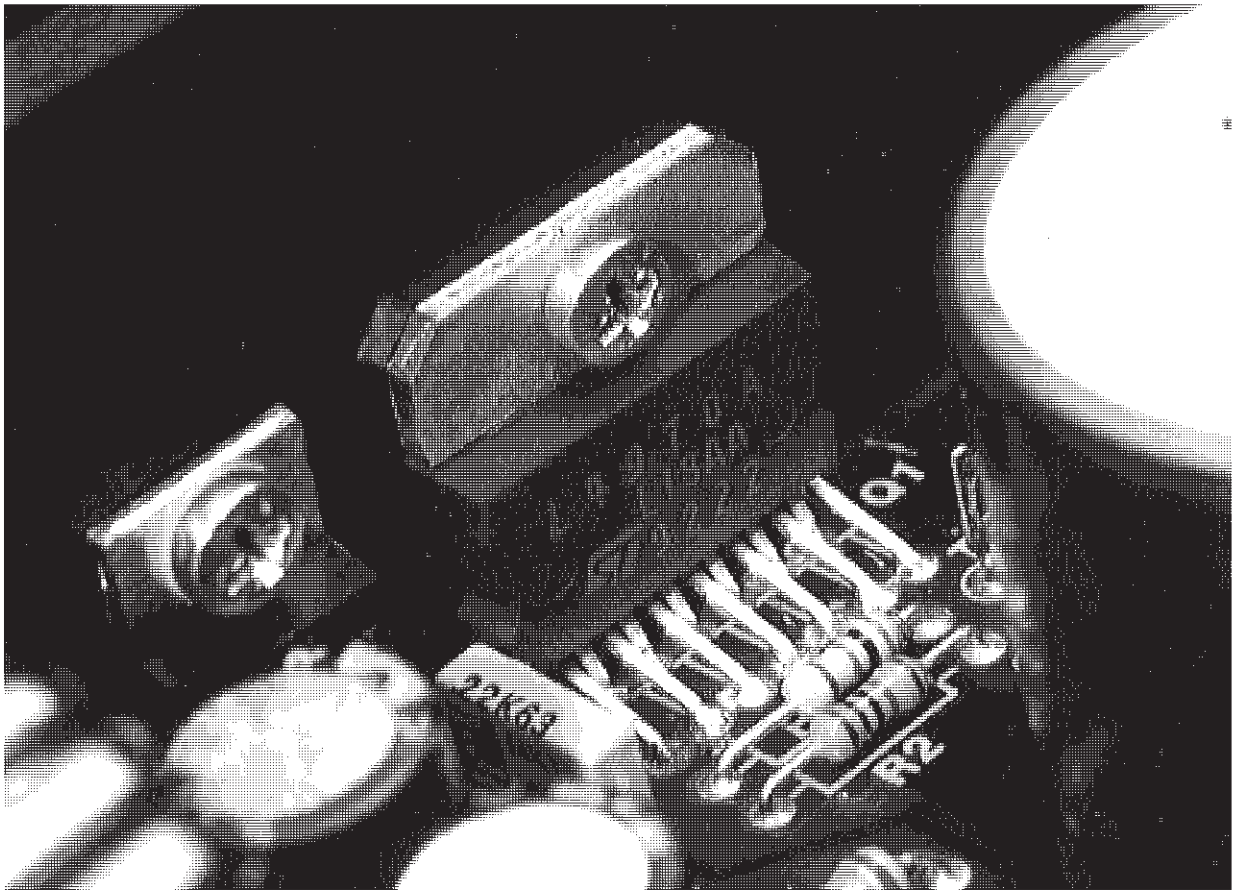
The L497XA series of high current switching regulator ICs exploit Multipower-BCD technology to achieve very high output currents with low power dissipation – up to 10A in the Multiwatt power package and 3.5A in a DIP package .



THE TECHNOLOGY

The technology architecture is based on the vertical DMOS silicon gate process that allows a channel length of 1.5 micron ; using a junction isolation technique it has been possible to mix on the same chip Bipolar and CMOS transistors along with the DMOS power components (Fig. 2). Figure 1 shows how this process brings a rapid increase in power IC complexity compared to conventional bipolar technology.

In the 70's class B circuits and DC circuits allowed output power in the range of 70W. By 1980, with the introduction of switching techniques in power ICs, output powers up to 200W were reached ; with BCD technology the output power increased up to 400W.

Figure 1: BCD process and increase in power ICs complexity.

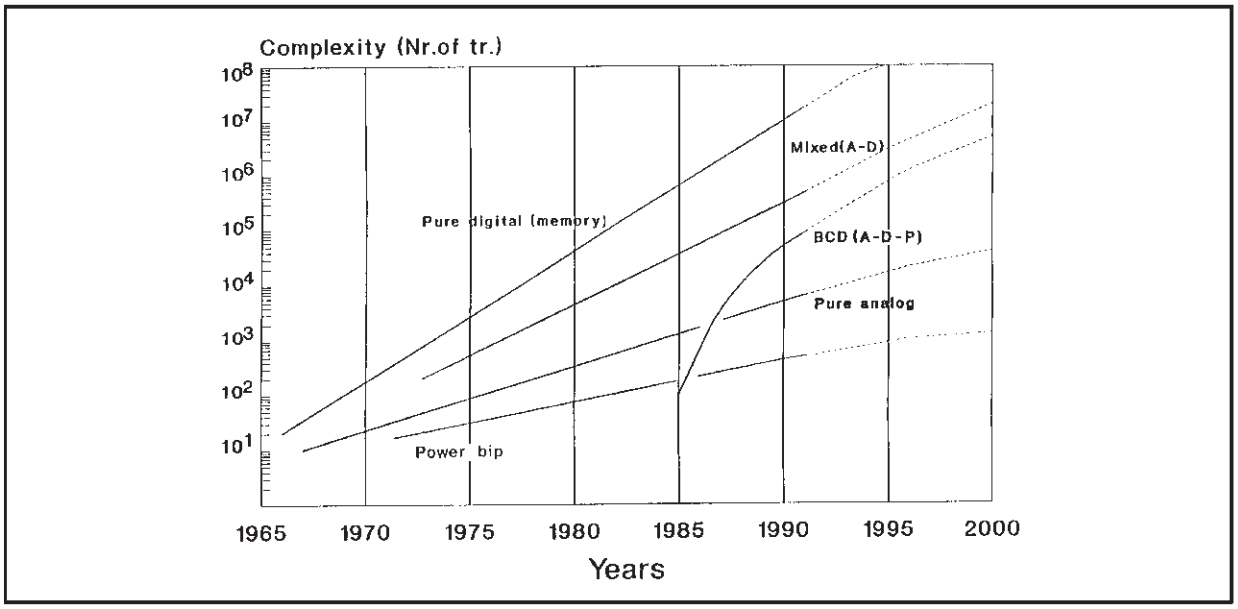
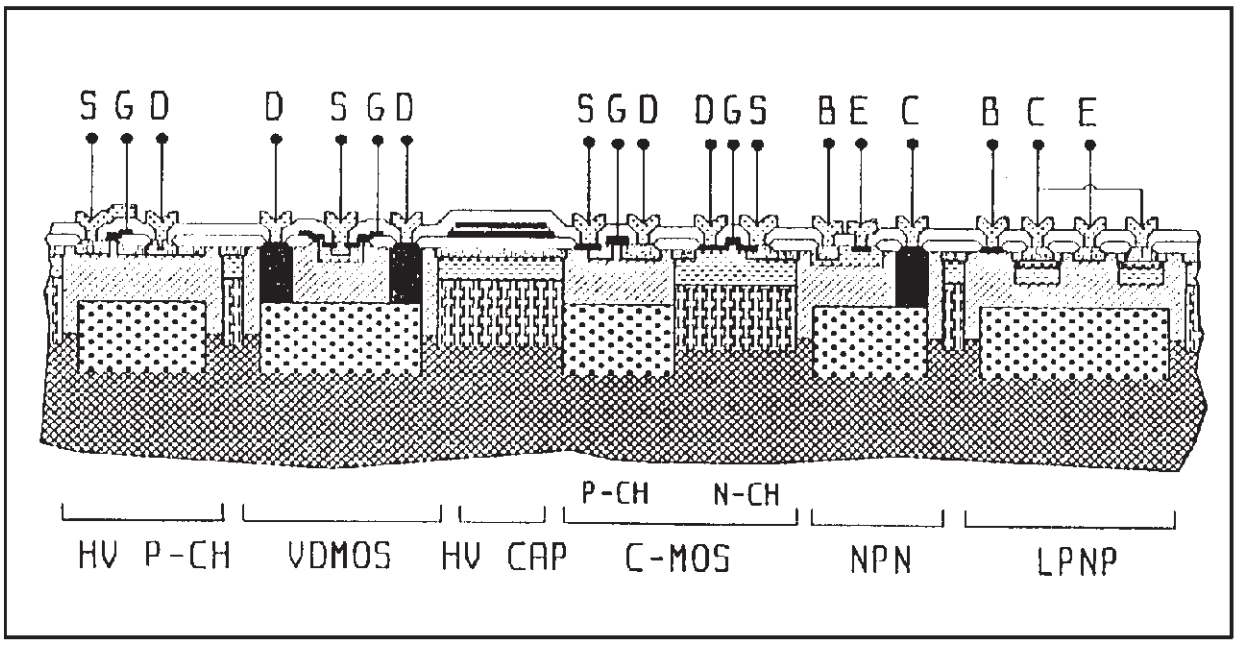


Figure 2: Cross Section of the BCD Mixed Technology.



THE STEP-DOWN CONFIGURATION

Fig. 3 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows : Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component super-imposed on it, ΔI_L, due to the voltage across L.

Figure 3: The Basic Step-down Switching Regulator Configuration

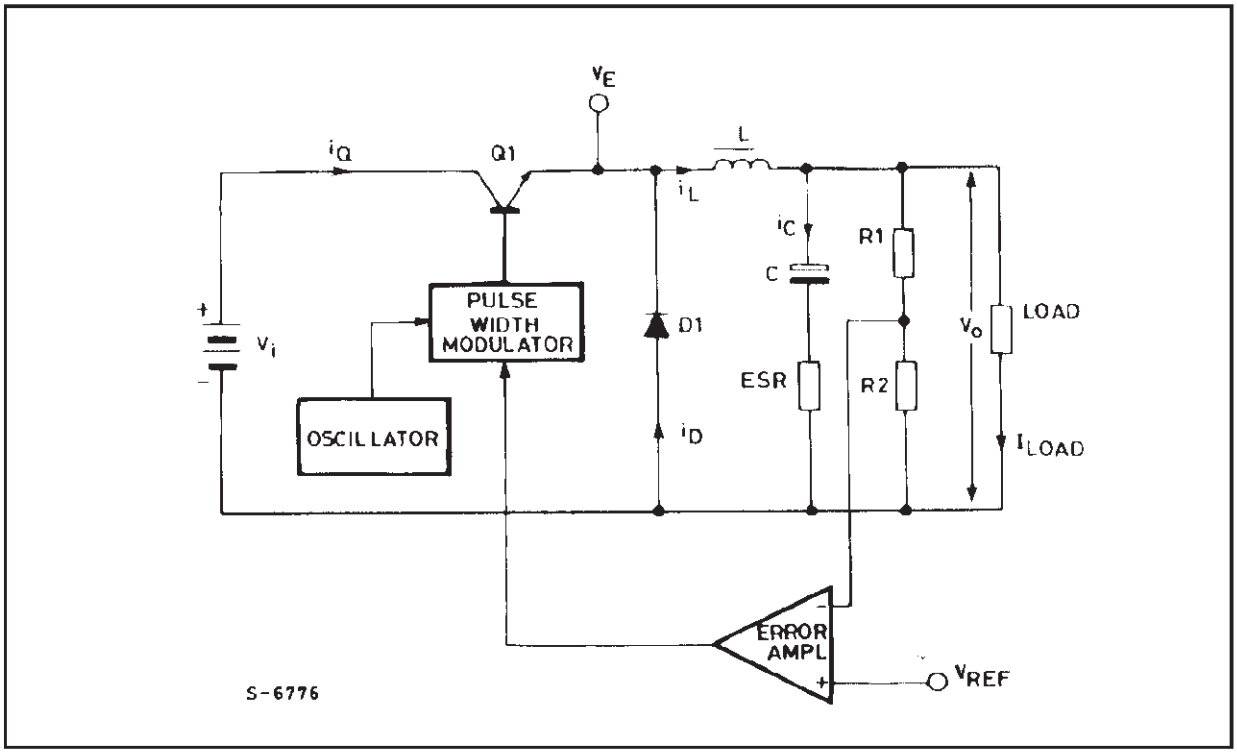


Fig. 4 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode era taken into account.

The ON and OFF times are established by the following expression :

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 4b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 4c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in Fig. 4e. In balanced conditions the ΔI_L^+ current increase occuring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula :

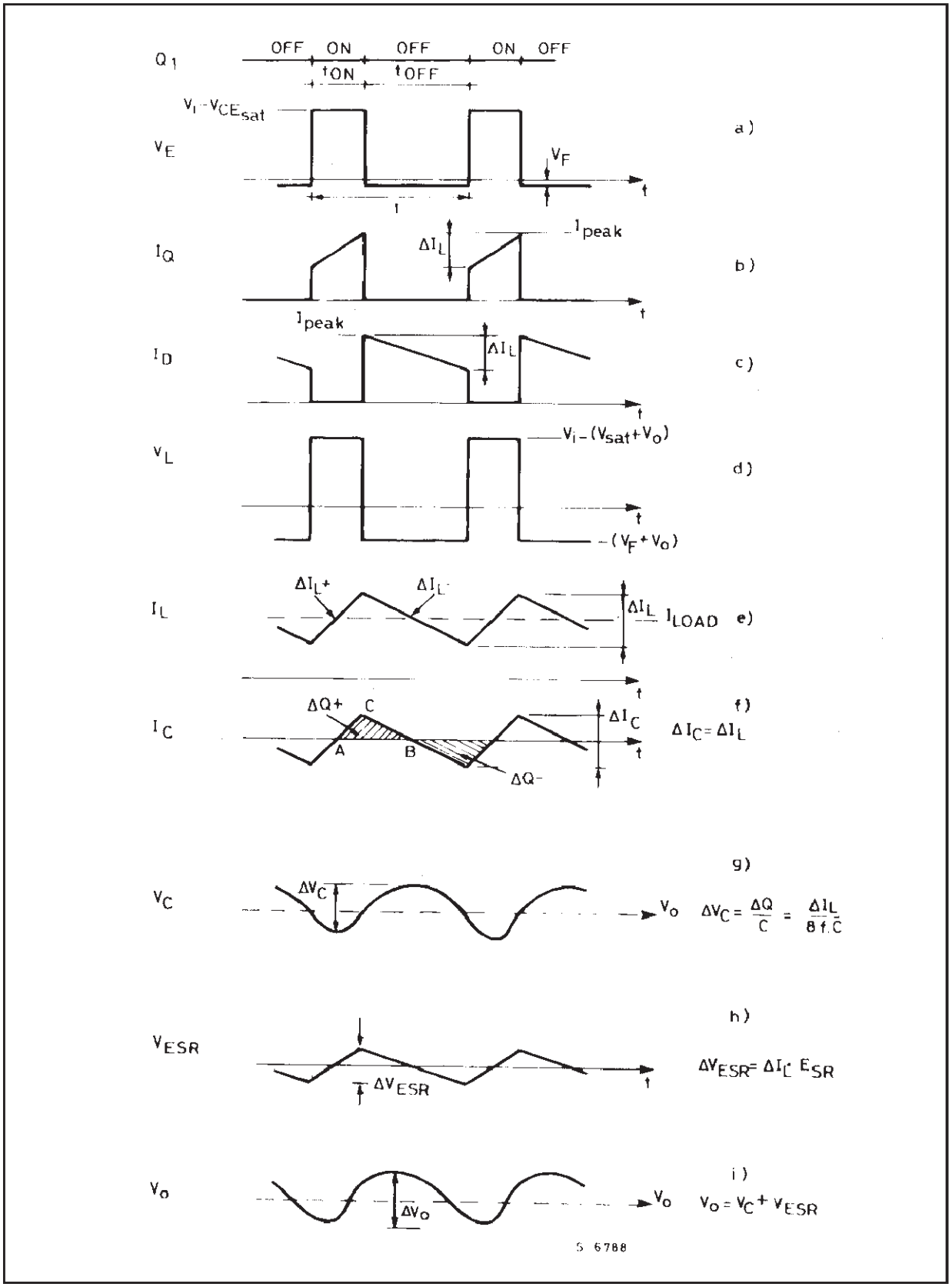
$$\Delta_{IL}^{+} = \Delta_{IL}^{-} = \frac{(V_i - V_{sat}) - V_O}{L} T_{ON} = \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect to $Io_{MIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 4d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 4f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.
This ripple consists of two components : a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Fig. 4g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in Fig. 4f :

Figure 4: Principal Circuit Waveforms of the figure 1 Circuit.



$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

Which therefore gives:

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 4h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is V_{ESR} (t) = i_C (t) · ESR. Fig. 4i shows the overall ripple V_o, which is the sum of the two previous components. As the frequency increases (> 20kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in Fig. 4 into account.

Starting from the initial conditions, where Q = ON, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression :

$V_i = v_L + v_C$ (V_{sat} is neglected against V_i).

$$V_i = L \frac{d_{IL}}{dt} + v_C = L \frac{d_{IL}}{dt} + V_o \quad (1)$$

which gives :

$$\frac{d_{IL}}{dt} = \frac{(V_i - V_o)}{L} \quad (2)$$

The current through the inductance is given by :

$$I_L = \frac{(V_i - V_o)}{L} \quad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that :

$$\Delta I_L^+ = \frac{(V_i - V_o)\ T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot very instantaneously, the voltage across the ased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present :

$v_C(t) = V_o$, i_L (t) = i_D (t) = I_{peak}

And the equation associated to the following loop may be written :

$$V_F + L \frac{d_{IL}}{dt} + v_C = 0 \quad (5)$$

where :

$v_C = V_o$

$$\frac{dI_L}{dt} = -(V_F + V_o) / L \quad (6)$$

It follows therefore that :

$$i_L (t) = -\frac{V_F + V_o}{T}\ t \quad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs :

$$I_L = \frac{V_o}{L}\ t \quad (8)$$

therefore :

$$\Delta I_L^+ = \frac{V_o}{L} T_{OFF} \quad (9)$$

But, because

$\Delta I_L{}^+ = \Delta I_L{}^-$ if follows that :

$$\frac{(V_i - V_o)\ T_{ON}}{L} = \frac{V_o\ T_{OFF}}{L}$$

which allows us to calculate V_o :

$$V_o = V_i \frac{T_{ON}}{T_{ON}\ T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relation-ship between the currents is the following :

$$I_{iDC} = Io_{DC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula :

$$\eta\ \% = \frac{P_o}{P_i} \cdot 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o,

plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \quad (12)$$

DC LOSSES

P_{sat} :saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} + V_{sat}\ I_o \frac{V_o}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power

transistor saturation at current Io.

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F\ I_o \frac{V_i - V_o}{V_i} = V_F I_o\ (1 - \frac{V_o}{V_i}) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S\ I_o^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current :

$$P_q = V_i\ I_q, \quad (16)$$

in which Iq is the operating supply current at the operating switching frequency.
Iq includes the oscillator current.

SWITCHING LOSSES

P_{sw} :switching losses of the power transistor :

$$P_{sw} = V_i\ I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculation T_{ON} and T_{OFF} through (4) and (9) respectively it follows that :

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \qquad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

But because :

$T_{ON} + T_{OFF} = T$ and $\Delta I_L^+ = \Delta I_L^- = \Delta I_L$,

it follows that :

$$T_{ON} = \frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T \quad (17)$$

Calculating L, the previous relation becomes :

$$L = \frac{(V_i - V_o)\ V_o}{V_i\ \Delta\ I_L} T \quad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that :

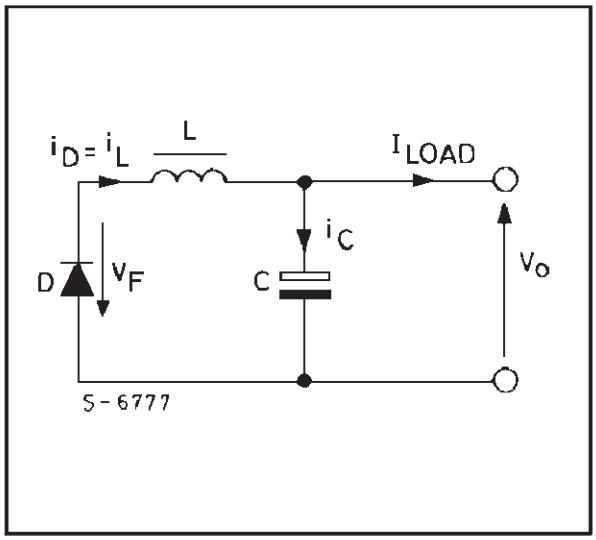
$L = \frac{(V_i - V_o)\ V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$ where L is in Henry and f in Hz

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by :

$i_c\ (t) = i_L\ (t) - I_o$

Figure 5: Equivalent Circuit Showing Recirculation when Q1 is Turned Off.



From the behaviour shown in Fig. 4 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that :

$$\Delta V_C = \frac{\Delta I_L}{4C} \frac{T}{2} = \frac{\Delta I_L T}{8C} = \frac{\Delta I_L}{8fc} \quad (19)$$

but, remembering expression (4) :

$$\frac{\Delta I_L^+ = (V_i - V_o) T_{ON}}{L} \text{ and } T_{ON} = \frac{V_o}{V_i} T$$

therefore equation (19) becomes :

$$\Delta V_C = \frac{(V_i - V_o) V_o}{8 V_i f^2 L C}$$

Finally, calculating C it follows that :

$$C = \frac{(V_i - V_o) V_o}{8 V_i \Delta V_C f^2 L} \quad (20)$$

where : L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true :

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \quad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C (dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.
Moreover, the following is true :

$$v_L = L \frac{di_L}{dt} \quad (23)$$

where $di_L = \Delta I_o$

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and (23) and equalizing, it follows that :

$$L \frac{di_L}{v_L} = C \frac{dv_C}{i_C}$$

Calculating dv_c and equalizing it to ΔV_o, it follows that :

$$\Delta V_o = \frac{L \Delta I_o^2}{C (V_i - V_o)} \quad (24) \quad \text{for} + \Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \quad (25) \quad \text{for} - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the under-shoot, which could trigger the reset function.

DEVICE DESCRIPTION

For a better understanding of how the device functions, a description will be given of the principle blocks that compose the device. The block diagram of the device is shown in fig.6

POWER SUPPLY

The device contains a stabilized regulator (Vstart = 12V) that provides power to the analogic and digital control blocks as well as the section of the bootstrap. The Vstart voltage also powers the blocks that operates the internal reference voltage of 5.1V, with a precision of ±2%, necessary for the feedback.

OSCILLATOR, SYNC. AND VOLTAGE FEEDFORWARD FUNCTIONS

The oscillator block generates a sawtooh wave signal that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal that will then sent to the power output stage. The oscillator also contains the voltage feedforward function that, being completely integrated, does not require additional external components to function. The VFF function operates with supply voltages from 15V to 45V. The $\Delta V/\Delta t$ of the sawtooh is directly proportional to the supply voltage Vi.

As Vi increases, the conduction time (ton) of the power transistor decreases in such way as to provide to the coil, and therefore to the load, the product Volt x Sec constant.

Figure 6: Block Diagram of the 10A Monolithic Regulator L4970A.

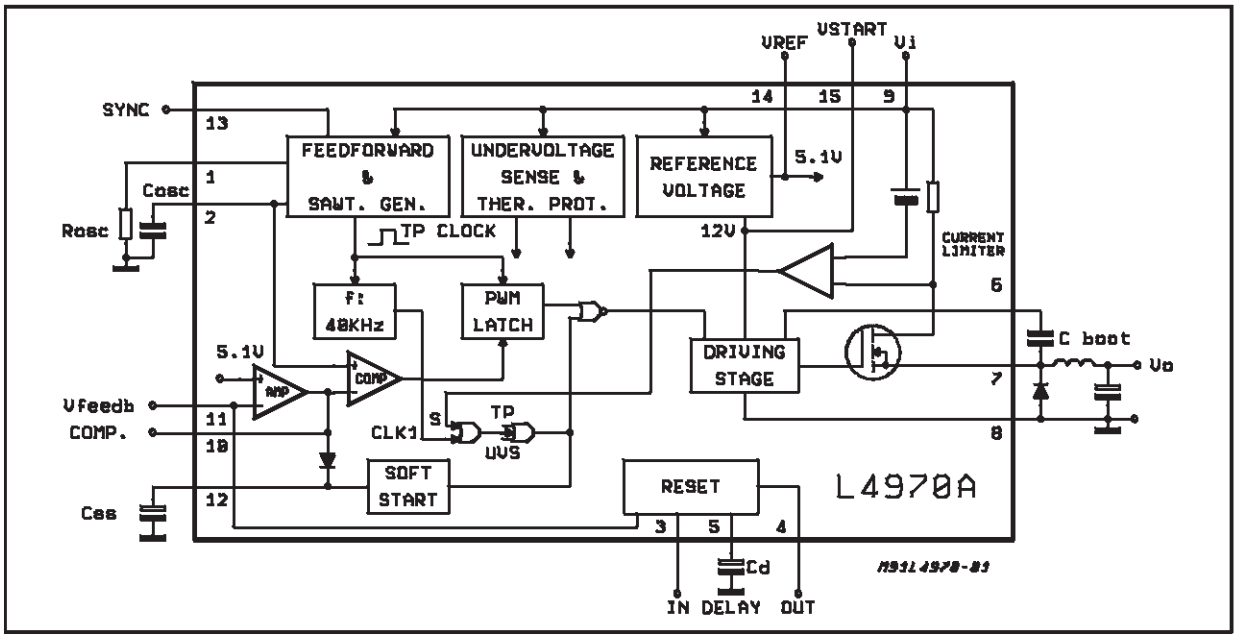


Figure 7: Voltage Feeforward Waveform.

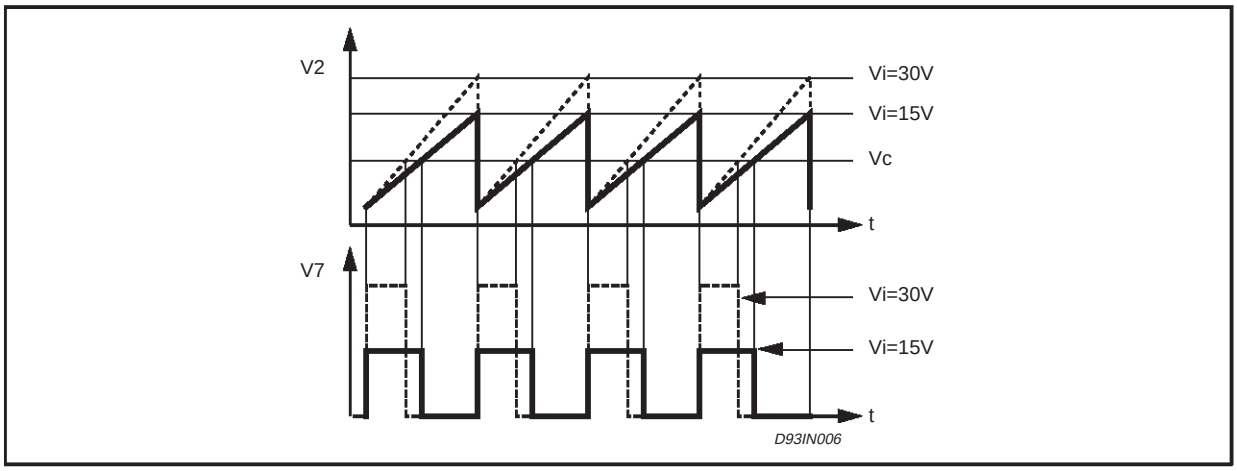


Fig. 7 shows the duty-cycle varies as a result of the changes in slope of the ramp with the input voltage Vi. The output of the error amplifier should not change to maintain the output voltage in regulation. This function allows for the increase of speed in response to the rapid change of the supply voltage and for a greatly reduced ouput ripple at the mains frequency.

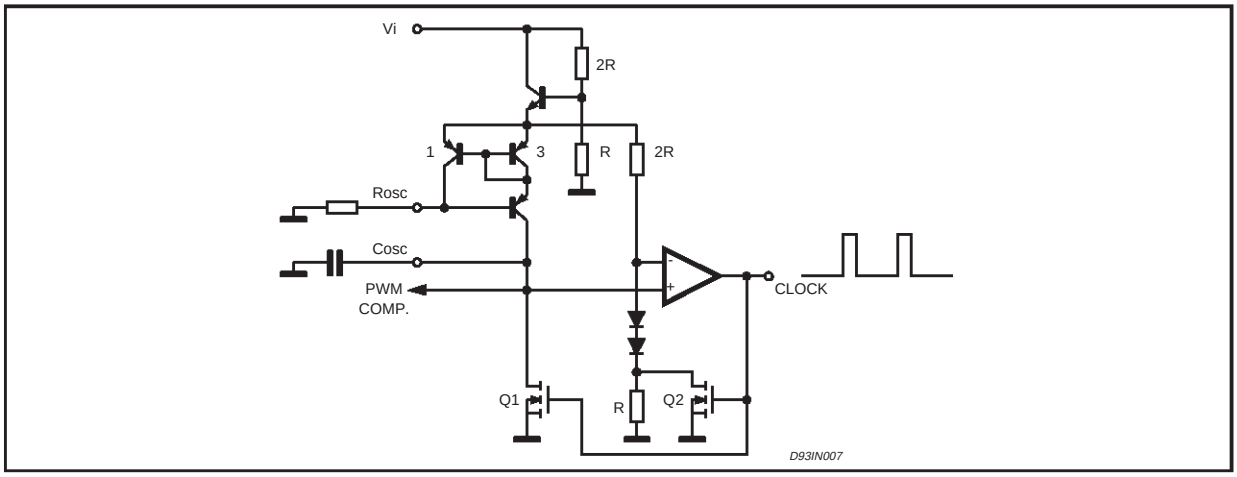
In fact, the slope of the ramp is modulated by the ripple, generally present in the order of several volts on the input of the regulator, particularly when the solution with a mains transformer is used.

Fig. 8 shows the simplified electrical diagram of the oscillator.

A resistor, connected between the Rosc pin and GND, sets the current that is internally reflected in the pin Cosc, in order to charge the external capacitor to which it is connected. The voltage to the Rosc pin is not fixed, but is tied to the instantaneous value of Vi; this is needed to achieve the feedforward voltage function, in which the slope of the ramp is directly proportional to the supply voltage. A comparator senses the voltage at the Cosc capacitor. When the voltage reaches the value present at the inverting input of the comparator, the output from the comparator goes high and is sent to the two transistors Q1 and Q2.

Q1 is responsible for discharging the external Cosc capacitor with a current of approx. 20mA, while Q2 imposes at the inverted input of the comparator a voltage of 2Vbe (approx. 1.3V) that is the low-threshold of the ramp. Some useful formulas for calculating the various parameters of the oscillator block are:

Figure 8: Oscillator Circuit.



1) Oscillator charge current:

$$I_{CHARGE} = \frac{V_i - 9V_{be}}{R_{osc}} \quad \text{(For } 15V < Vi < 45V\text{)}$$

2) Oscillator discharge current:

I_{DISCH} = 20mA

3) Peak voltage ramp:

$$V_{th-H} = \frac{V_i - 9V_{be}}{Rosc} + 2V_{be}$$

This formula is obtained in the following way: indicating with Ve the voltage of the emitter of the NPN transistor connected to Vcc, and V- the voltage at the inverted input of the comparator, one has:

$$\text{(a)} \quad V_e = \frac{V_i}{3} - V_{be}$$

$$\text{(b)} \quad V- = \left(\frac{V_e - 2V_{be}}{3R} \cdot R\right) + 2V_{be}$$

by substituting (a) into (b), one obtains:

$$V- = \frac{(\frac{V_i}{3} - V_{be}) - 2V_{be}}{3} + 2V_{be} = \frac{V_i - 9V_{be}}{9} + 2V_{be}$$

4) Valley voltage ramp:

$V_{th-L} = 2V_{be}$

5) Switching frequency:

$$f_{SW} = \frac{9}{R_{osc}\, C_{osc}}$$

It should be noted that formula (5) does not take into account the discharge time of Cosc which cannot be neglected when one is working at frequencies equal or higher than 200KHz. The discharge time is also tied to the value of Cosc itself.

Analitycally one has:

$$6) \quad T_{DISCH} = \frac{V_{th-H} - V_{th-L}}{20mA} \cdot C_{osc}$$

from which is obtained the more closely approximate expression of the oscillator frequency:

$$7) \quad f_{SW} = \frac{1}{\frac{R_{osc} \cdot C_{osc}}{9} + T_{DISCH}}$$

During the discharge time of Cosc, a clock pulse is generated internally that is made subsequently available on the Sync. pin and that can be used to synchronize other regulators. (3 devices of the same family maximum). The Sync. pulse generated has a typical range of 4.5V and the current availability is 4.5mA. In general, it is better that the Sync pulse is at least 300-400ns in order to be able to synchronize a range of existing regulators; to obtain this result, values of suggested capacitors, in different test circuits, have been selected. The typical duration of the synchronizing pulse with the suggested values of Cosc are as follows:

L497X Family (MULTIWATT PACKAGE)	
C_{osc} (nf) - R_{osc} = 16KΩ	Sync (ns)
0.68	140
1	230
1.2	270
1.5	330
2.2	450
3.3	680
4.7	1100

L497X Family (POWERDIP PACKAGE)	
C_{osc} (nf) - R_{osc} = 30KΩ	Sync (ns)
1.2	230
1.5	280
2.2	420
3.3	600
4.7	900

Obviously, synchronize pulses of eccessive duration can greatly reduce the max duty-cycle and produce distortions in the sawtooth of the synchronized regulator working as slave.

P.W.M.

Comparing the sawtooth signal generated by the oscillator and the output of the error amplifier, generates the PWM signal which is sent to the driver of the output power stage. The PWM signal, in the path towards the output stage, also encounters a latch block to prevent other pulses from being sent at same period to the output, possibly damaging the power stage. In the PWM block, a duty-cycle limiter has also been introduced. Such a limiter is obtained by taking advantage of the synchronizing pulse generated, the power output stage is inhibited. Even if the error amplifier gives a large signal to the peak of the ramp, the power stage will not be able to operate in DC, but will be switched off at each clock pulse.

The max. obtainable duty-cycle is higher than 90%; this, however depends on the working frequency and the value of Cosc. Using the formulas 6) and 7) a precise calculation can be done.

SOFT START

The Soft Start function is essential for a correct startup of the device and for an output voltage that, at the switch on, increases in a monotonous mode without dangerous output overvoltages and without overstress for the power stage.

Soft Start operates at the startup of the system and after an intervention of the thermal protection. Fig. 9 shows the simplified diagram of the startup functions. The function is carried out by means of an external capacitor connected to the Soft Start pin, which is charged with a constant current of about 100µA to a value of around 7V. During the charging time, the output of the error transconductance amplifier, because of Q1, is forced to increase at the same rising edge time of the external softstart capacitor Css.

Figure 9: Soft Start Circuit.

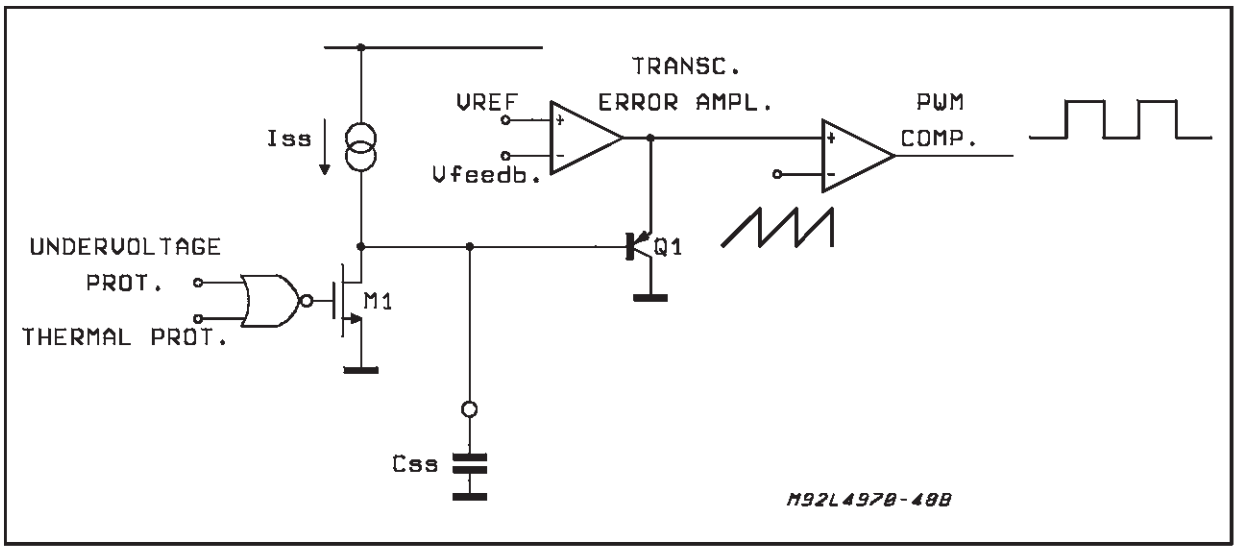
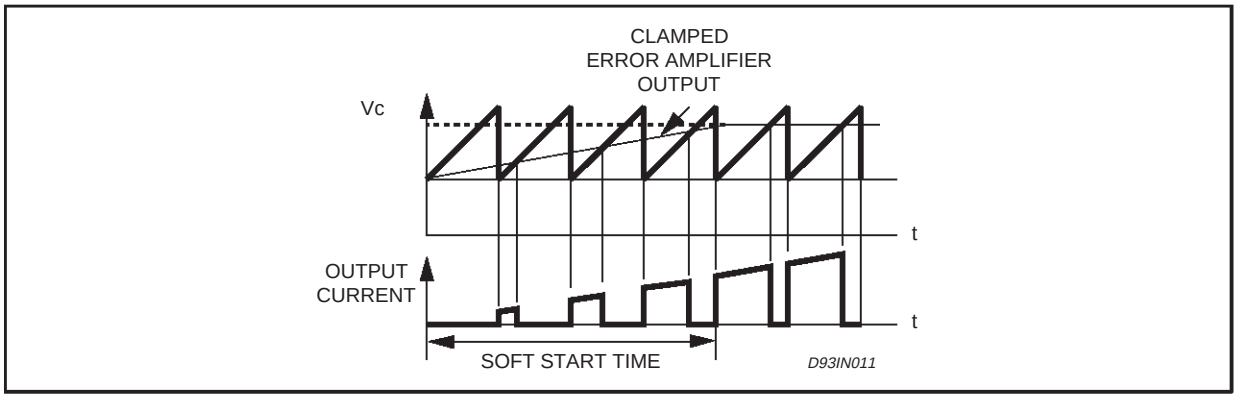


Figure 10: Soft Start Waveforms.



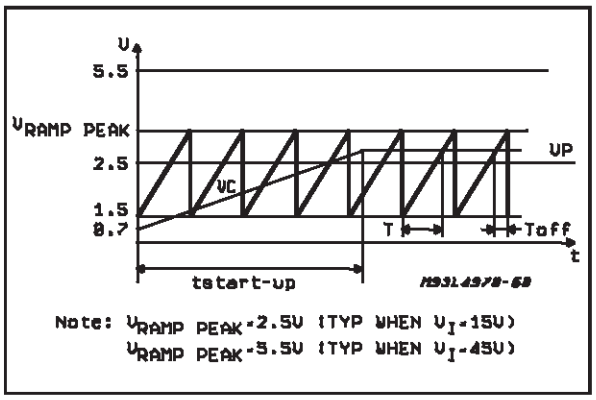
The PWM signal begins to be generated as soon as the output voltage of the error amplifier crosses the ramp; at this point the output stage begins to commutate, slowly increasing its ON time (see fig. 10).

The charge of the Css capacitor, as already mentioned, begins each time the device is supplied with power and after which an anomalous condition is created, as the intervention of thermal protection or of the undervoltage lockout.

CALCULATING THE DUTY-CYCLE AND SOFT-START TIME

Let us suppose that the discharge time of the oscillator capacitor, Cosc, is neglected. This is an approx. valid for switching frequencies up to 200KHz. Let us indicate with Vr the output voltage of the error amplifier, and with Vc the voltage of the oscillator ramp.

Figure 11: Soft Sart Time Waveform.



The PWM comparator block commutates when Vr = Vc. Therefore:

$$8)\quad V_r = V_c = \frac{V_{pp}}{T}\cdot t = \frac{V_i - 9V_{be}}{9\cdot T}\cdot t$$

from which is obtained

$$9)\quad t = \frac{V_r \cdot T \cdot (V_i - 9V_{be})}{9}$$

The time **t** obtained from this equation is equal to the ON time of the power transistor. The corresponding duty-cycle is given by:

10)

$$D = \frac{t_{on}}{T} = \frac{V_r \cdot T \cdot (V_i - 9V_{be})}{9T} = \frac{V_r \cdot (V_i - 9V_{be})}{9} = \frac{V_O}{V_i}$$

Consequently, after leaving the discharged capacitor of Soft Start, the output of the regulator will reach its value when the voltage across the Css capacitor, charged with constant current, has reached the value Vr - 0.5V.

The time necessary in order that the output rises from zero to the nominal value is given by:

$$11)\quad t_{start-up} = C_{ss}\cdot\frac{(V_r - 0.5V)}{I_{ss}}$$

in which Css is the Soft Start capacitor and Iss the Soft Start current. Considering Soft Start time as tss, the required time for the Soft Start capacitor to change itself approx from (2Vbe - 0.5V) = (1.2V - 0.5V) to Vr - 0.5V, is:

$$12)\quad t_{ss} = C_{ss}\cdot\frac{(V_r - 1.2V)}{I_{ss}}$$

By taking Vr from (10):

$$13)\quad V_r = \frac{V_o}{V_i}\cdot\frac{9}{V_i - 9V_{be}}$$

and substituting it in (12), we obtain:

$$14)\quad t_{ss} = \frac{C_{ss}}{I_{ss}}\left(\frac{V_o}{V_i}\cdot\frac{9}{V_i - 9V_{be}} - 1.2V\right)$$

UNDERVOLTAGE LOCKOUT

The device contains the protection block of undervoltage lockout which keeps the power stage turned-off as long as the supply voltage does not reach at least 12V. At this point the device starts up with Soft Start.

The function of undervoltage is also provided with an hysteresis of 1V to make it better immune to the ripple present on the supply voltage.

ERROR AMPLIFIER

The error amplifier is a transconductance type and deliver an output current proportional to the voltage inbalance of the two inputs. The simplified diagram is presented in fig 12.The principal characteristics of this uncompensated operational amplifier are the following:

Gm = 4mA/V, Ro = 2.5Mohm, Avo = 80dB, Isource-sink = 200uA, Input Bias Current = 0.3uA.

The frequency response of the op. amp. is given in fig. 13.

Ignoring the high frequency response and hypothesizing that the second pole is below the 0 dB axis in the all the conditions of loop compensation, it is possible to make a first approximation with the equivalent circuit of fig. 14

Figure 12: Error Amplifier Circuit.

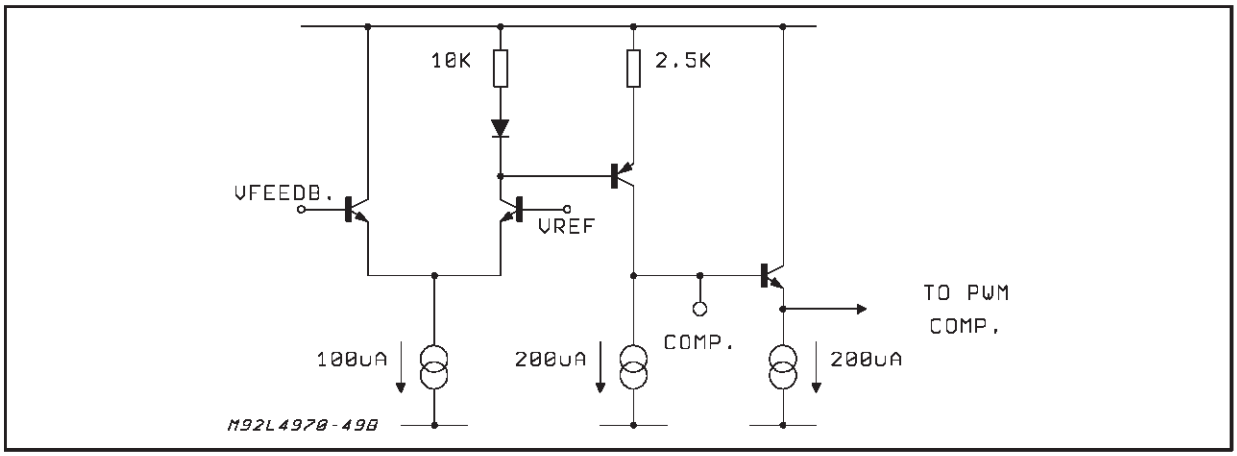


Figure 13: Open loop gain (error amplifier only)

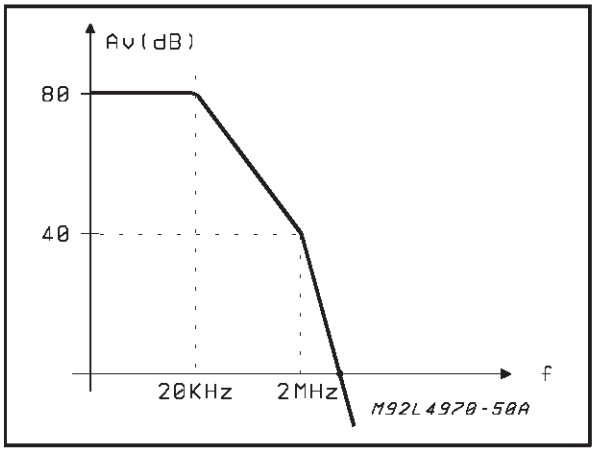
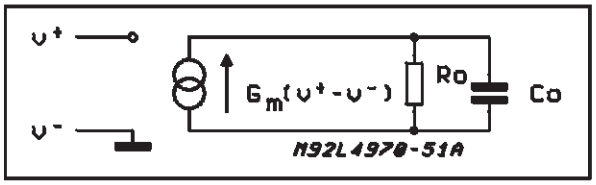


Figure 14: Error amplifier equivalent circuit.



In which:

15) $Av(s) = Gm \cdot \frac{R_O}{1 + sR_O C_O}$ where $C_O = 3pF$

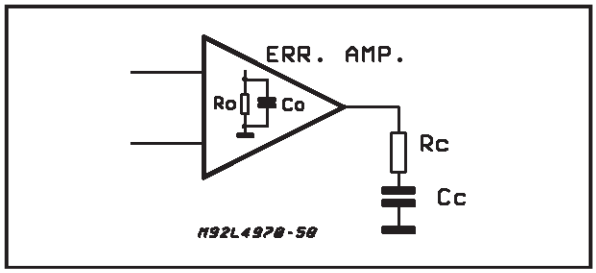
The error amplifier can be easily compensated thanks to the high output impedance (see fig. 14)

The resulting transfer function is as in the following:

(16)

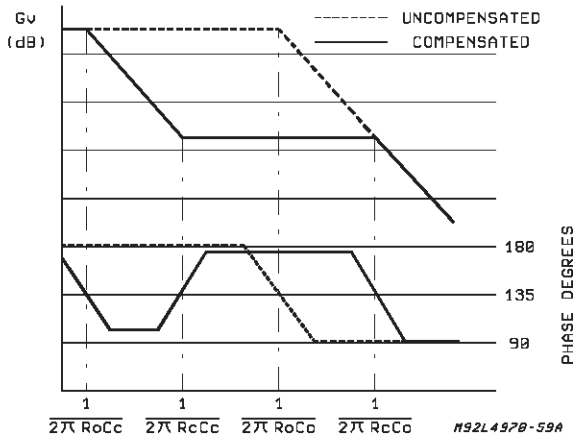
$$Av(s) = Gm \cdot \frac{R_O \cdot (1 + sRcCc)}{s^2 R_o C_o R_c C_c + s (R_o C_c + R_o C_o + R_c C_c) + 1}$$

Figure 15: Compensation network of the error amplifier



The Bode diagram is shown in fig.16.

Figure 16: Bode plot showing gain and phase of compensated error amplifier



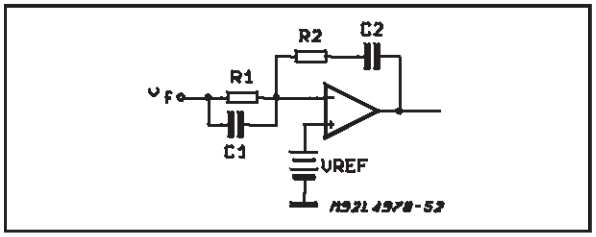
The compensation circuit introduces a pole at low frequency and a zero that is generally calculated to be put in the proximity of the resonance frequency of the output LC filter.

The second pole at high frequency generally falls in a zone of no interest (for the system stability, one must consider the zero introduced by ESR

characteristic of the output capacitor. Not all the designers agree on this solution).

If necessary, however, one can turn to more sophisticated compensation circuitry. An example is shown in fig. 17.

Figure 17: One pole, two zero compensation network



Such a circuit introduces a pole at low-frequency and two zeros.

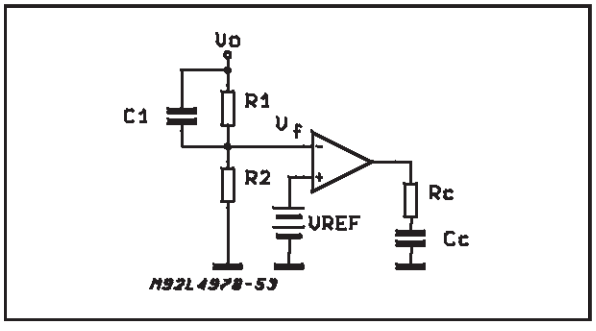
$$17)\quad Z1 = \frac{1}{2\Pi\ R1\ C1} \qquad Z2 = \frac{1}{2\Pi\ R2\ C2}$$

It must be remembered, however, that because of the high output impedance of the error amplifier, a second pole is also present:

$$18)\quad P2 = \frac{Gm}{2\Pi\ C1}$$

We normally suggest a high value for R1 to reduce the value of the capacitor C1 and allocate the pole P2 at the highest possible frequency. The essential limitation to the max value of R1 is the offset introduced by the input bias current of the error amplifier. In the case of output voltage regulated higher than 5.1V, an external divider should be introduced. It's than possible to introduce a second zero using the following network:

Figure 18: Compensation network for output voltages higher than 5.1V



Two zeros and two poles are introduced:

$$19)\quad Z1 = \frac{1}{2\Pi\ R_O\ C_C} \qquad Z2 = \frac{1}{2\Pi\ R1\ C1}$$

$$P1 = \frac{1}{2\Pi\ R_O\ C_C} \qquad P2 = \frac{1}{2\Pi\ Rx\ C1}$$

$$\text{Where } Rx = \frac{R1 \cdot R2}{R1 + R2}$$

APPLICATION EXAMPLE

Consider the block diagram of fig. 19, representing the internal control loop section, with the application values:
Fswitch = 200KHz, L = 100µH, C = 1000µF,
Po = 50W, Vo = 5.1V, Io = 10A and Fo = 500Hz.
G_{loop} = PWM · Filter

Figure 19: Block diagram used in stability calculation

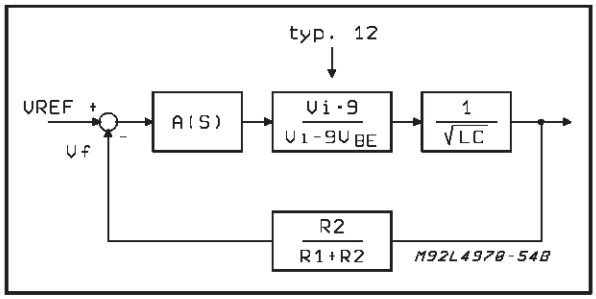
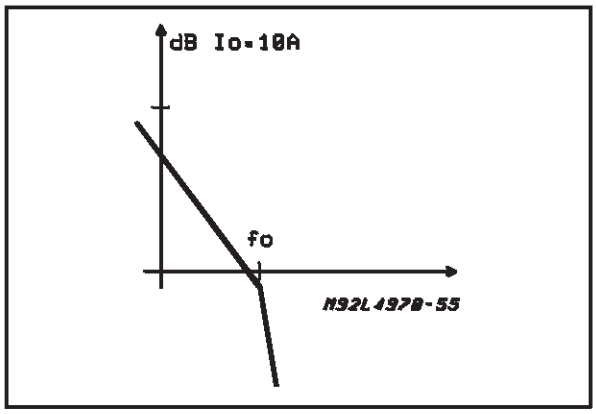


Figure 20: Frequency behaviour of the circuit of fig. 19



The system requires that DC gain is maximum to achieve good accuracy and line rejection. Beyond this a bandwidth of some KHz is usually required for a good load transient response. The error amplifier transfer function must guarantee the above constrainst. A compensation network that could be used is shown in fig. 21.

$$A(s) = \frac{(1 + sR1\ C1)\ (1 + sR2\ C2)}{sR1\ C1\ (1 + s\ \frac{C1}{Gm})}$$

Figure 21: Compensation network.

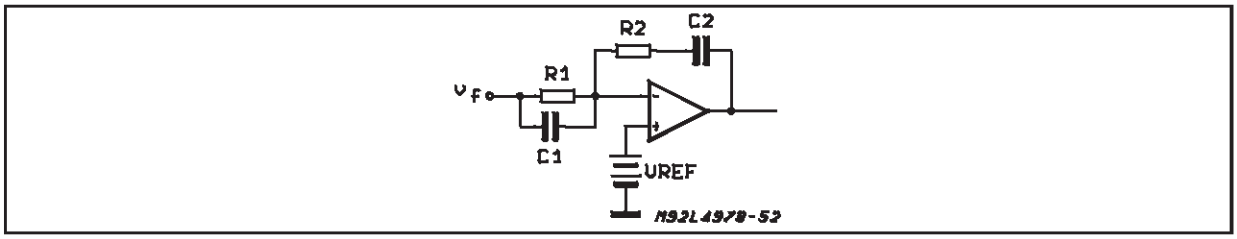
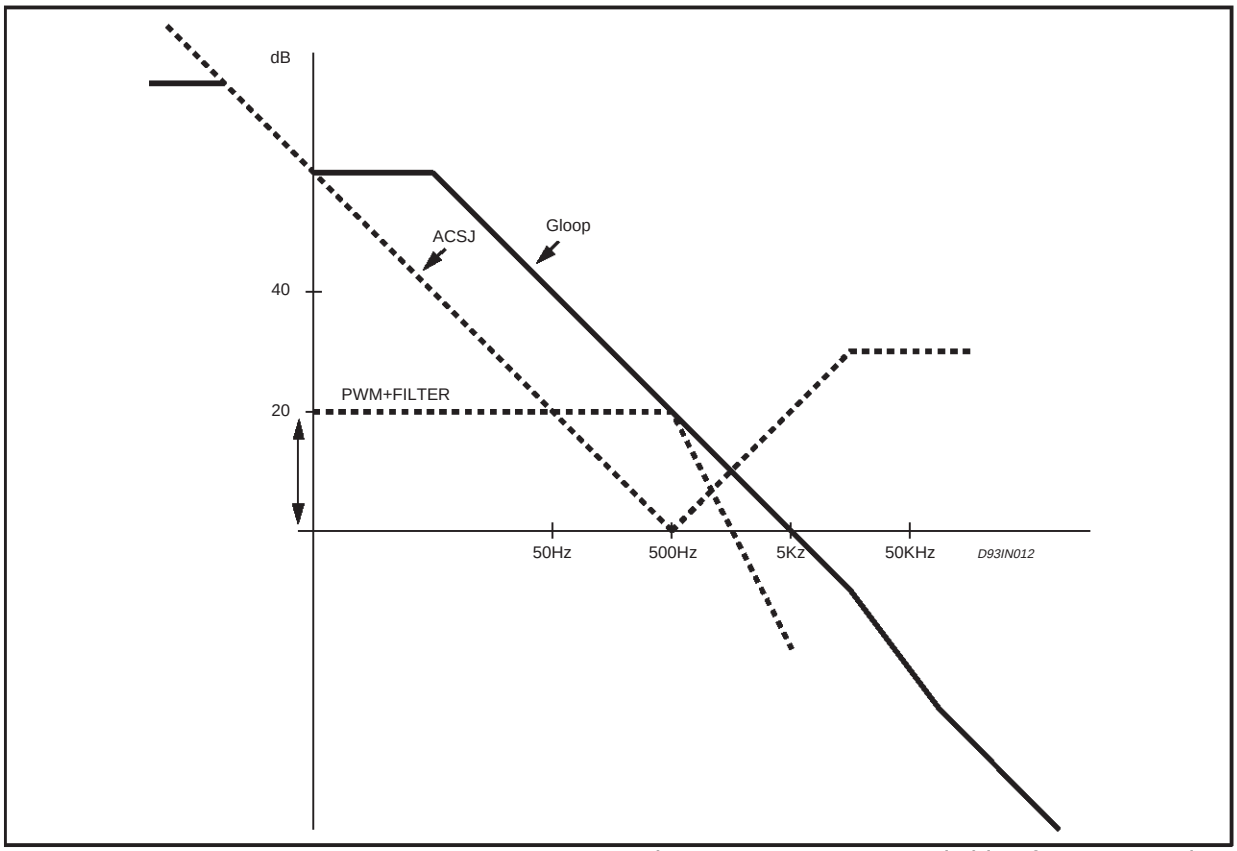


Figure 22: Bode plot of the regulation loop with the compensation network of fig. 21.



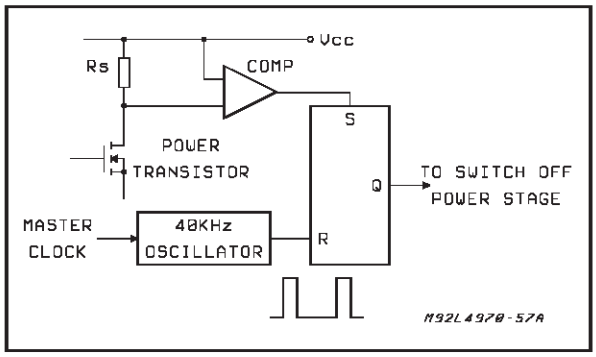
The criterium is to define Z1, Z2 close to the resonant pole of the output LC filter. The Gm/2ΠC1 pole must be placed at a frequency at which open loop gain is below 0dB axis (fig. 22).

CURRENT LIMITING

A complete regulation system will be equipped with a good current limiter able to protect from load breaking and operator error controlls.
The current limiting function is totally integrated and does not require any external component. The output current is sensed by an internal low-value resistor, in series with the drain of the DMOS vertical power transistor..

A precision current limitation of ± 10% relative at the peak current is guaranted. During overcurrent situation the pulse by pulse current limitation produce an output stage switching frequency reduction. The block diagram of the current limiting is shown in fig. 23.

Figure 23: Current protection circuit.



In overcurrent situation the comparator send a signal at the flip-flop set input, an inhibit pulse is immediatly generated from it and sended at the output stage switching off the power mos.

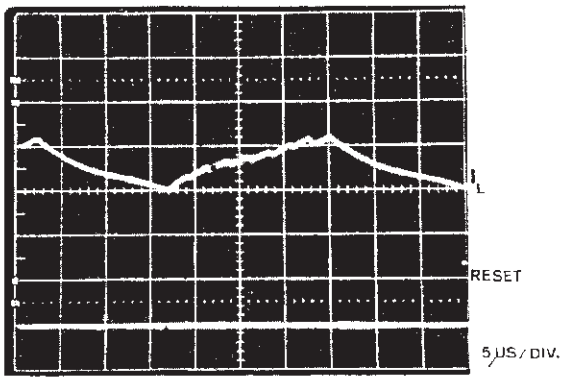
A reset pulse input in generated from an 40KHz internal oscillator.

After the first reset pulse the control loop will start to regulate the system an the output current will increase following the principal oscillator frequency. If overcurrent condition is still present the current limiting will be activate again.

This type of current limiting ensure a constant output current in overload or short circuit condition and allow a good reliability at high frequency (500KHz) reducing the problems relative at the internal signal delay through the protection blocks.

The inductor current in overload condition in shown in fig. 24.

Figure 24: Overload inductance current.



The 40KHz internal oscillator is synchronized with the principal one. If the system work with a oscillator tracks the principal oscillator frequency. In this way the switching frequency will not increase in overload situation.

A particular care has to be taken in the inductor value in order to avoid problems during overload or short circuit conditions. A critical situation is present with high switching frequency, (more than 200KHz) where a small inductor value is used and with high capacitive load.

In order to return in nominal condition after a short circuit the inductor ripple at 40KHz with the nominal output voltage and current has to be lower than the current limitation value.

Example

Let us consider L4970A, 10A. (the same approach can be used for all the family).

The inductor ripple current is given by the following formula:

$$\Delta I_L = \frac{(V_i - V_o) \cdot V_o}{V_i \cdot fsw \cdot L}$$

where fsw = 40KHz ±10%

In order to get the maximum inductor ripple current, the previous formula becomes:

$$\Delta I_L = \frac{(V_{imax} - V_{omax}) \cdot V_{omax}}{V_{imax} \cdot f_{sw\,min} \cdot L}$$

The current limitation for L4970A will start to work at 13A.

therefore:

$$I_{lim\,min} > I_{onom} + \frac{\Delta I_L}{2}$$

where I_{onom} = 10A for L4970A.

POWER FAIL-RESET CIRCUIT

The L4970A include a voltage sensing circuit that may be used to generate a power on power off reset signal for a microprocessor system. The circuit senses the input supply voltage and the output generated voltage and will generate the required reset signal only when both the sensed voltages have reached the required value for correct system operation. The Reset signal is generated after a delay time programmable by an external capacitor on the delay pin. Fig 25 shows the circuit implementation of Reset circuit. The supply voltage is sensed on an external pin, for programmability of the threshold, by a first comparator. The second comparator has the reference threshold set at slightly less the ref. voltage for the regulation circuit and the other input connected internally at the feedback point on the regulated voltage. When both the supply voltage and the regulated voltage are in the correct range, transistor Q1 turns off and allows the current generator to charge the delay capacitor discharges completely before initialization of a new Reset cycle. The output gate assures immediate take of reset signal without waiting for complete discharge of delay capacitor. Reset output is an open collector transistor capable of sinking 20mA at 200mV voltage. Fig 26 shows reset waveforms.

Figure 25: Power fail and reset circuit.

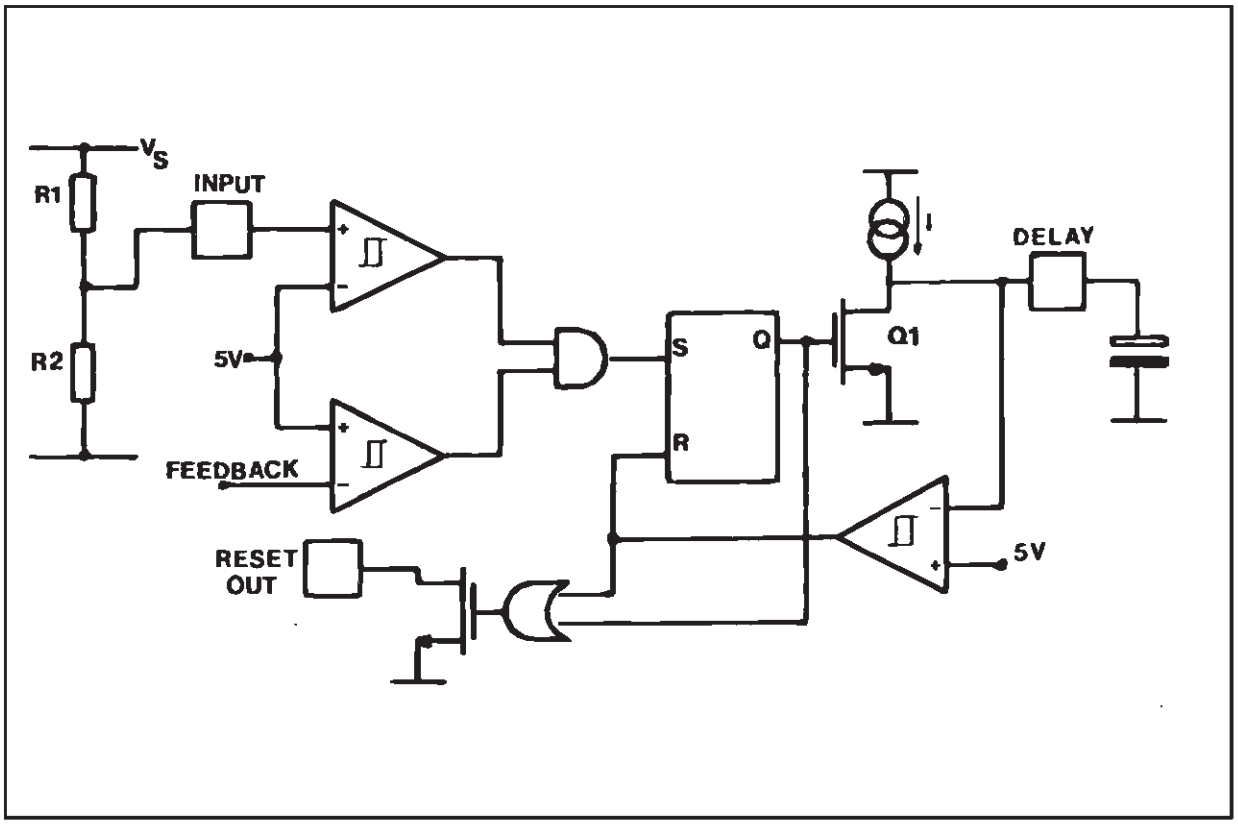


Figure 26: Reset and power fail and reset circuit.

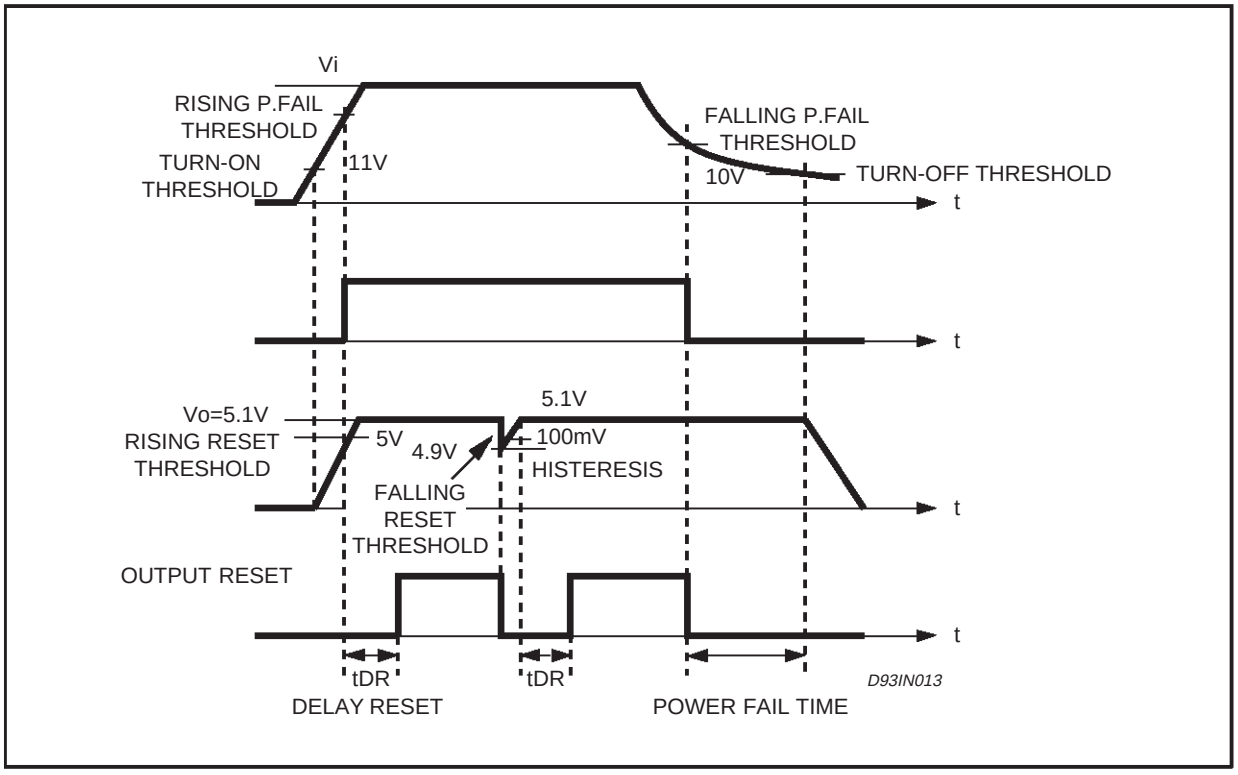
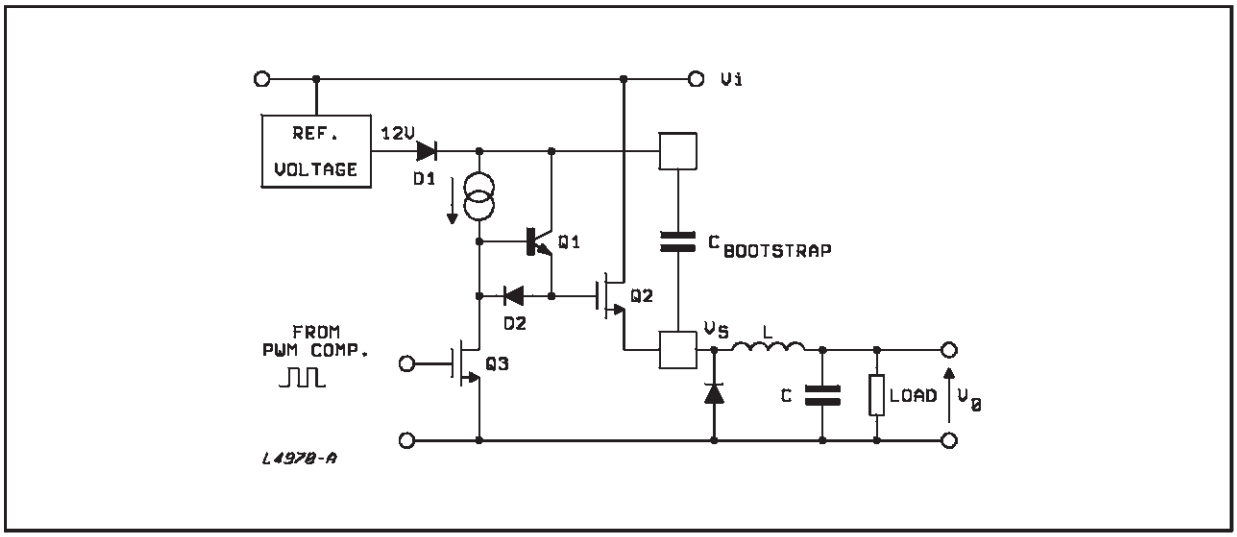


Figure 27: Power stage circuit.



POWER STAGE

The simplified diagram of the output stage is shown in the fig. 27.

The power stage and the circuit connected with it are by far the most important and critical components when one wants to obtain good performance at high switching frequency.

The power transistor must have excellent characteristics from the point of view of both the switching speed and the robustness.

The transistor DMOS, with its intrinsic characteristics of elevated speed, no second breakdown phenomenom and easy driving proves to be particularly suitable for this type of application that normally works at high frequency.

For a properly driving of the DMOS gate it is necessary to use an external bootstrap capacitor.

When the voltage Vs is low the Cboot capacitor is charged through the internal diode D1, at the value of voltage equal to that of Vstart, which is about 12V; the next step oversees that Q3 is turned off, Q2 is driven in gate by Q1 so that Q1 can go in saturation, and its source can go up rise towards Vi.

Cboot maintains its charge and guarantees a voltage equal Vi+12V at the gate of Q7, so that can enter into region of low resistance.

At this point the diode D1 turns on to be inversely polarized, disconnecting the 12V section from that of the driving power stage.

When Q2 is ON the driven current of the power stage requires from the bootstrap capacitor a typical current of 400uA.

When Q2 is Off a current of 2.5mA is required to mantain Q2 in that state. This current however is not delivered from the bootstrap capacitor, but rather from the internal regulator of 12V, while the output current flowing in the freewheeling diode.

The circuit described is capable of obtaining commutation, rise and fall time, a typical value of 50ns.

In principle, it would have been feasible to reduce furthermore the commutation time whithout any reliability problems.

This was not believed to be advantageous since it would not have been of any benefit if one thinks of the trr time of the catch diode (with trise of 50ns also the Schottky diodes begin to show limitations) and of the conseguent increase of different disturbances caused bt too higly elevated dI/dt.

Ther following table shows the main features of the DMOS transistor.

Figure 28: Gate-charge curve for the power

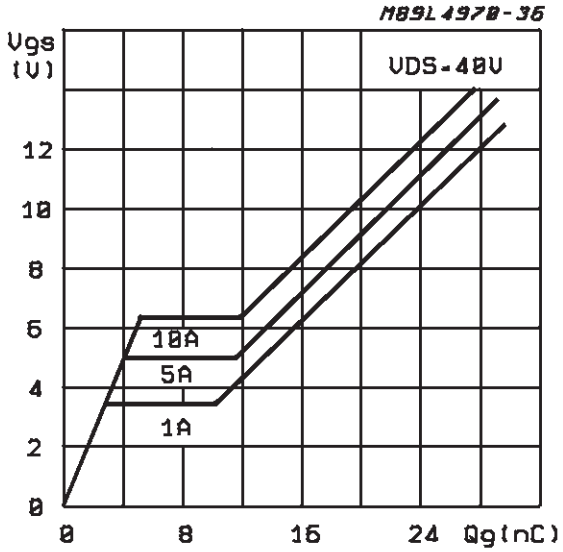


Table 1.

B_{VDSS} > 60V	at I_D = 1mA		V_{GS} = 0V
$R_{DS(ON)}$ = 100mΩ	at I_D = 10A	T_j = 25°C	V_{GS} = 10V
$R_{DS(ON)}$ = 150mΩ	at I_D = 10A	T_j = 150°C	V_{GS} = 10V
V_{TH} = 3V	at I_D = 1mA		

THERMAL SHUTDOWN

The thermal protection intervenes when the junction temperature reaches 150°C; it intervenes directly on the output stage turning it off quikly and in the meantime discharging the soft start capacitor.

The reference voltage and the oscillator will continue to work regularly.

The thermal shutdown has a hysteresis, after its intervention, it is necessary to wait for the junction temperature to lower around 30°C before the device will begin to work properly again.

The device restart to work by using the soft start function.

Table 2: High Current Switching Regulator ICs.

Parameter	L497X FAMILY					
	L4970A	**L4977A**	**L4975A**	**L4974A**	**L4972A**	**L4972AD Surf. Mount.**
Max. Input Operating Voltage	50V	50V	50V	50V	50V	50V
Output Voltage Range	5.1V (±2%) to 40V					
Max. Output Current	10A	7A	5A	3.5A	2A	2A
Power Switch R_{DSON} at 25°C	0.13Ω typ.					
Switching Mode Control System	Continuous Mode, Direct Duty Cycle Control with Voltage Feed-Forward					
Max. Switching Freq.	500KHz	500KHz	500KHz	200KHz	200KHz	200KHz
Efficiency V_{INPUT} = 35V V_{OUT} = 5.1V	10A 80% at 200KHz	7A 80% at 200KHz	5A 85% at 200KHz	3.5A 85% at 100KHz	2A 85% at 100KHz	2A 85% at 100KHz
Current Limiting	Constant Current					
Soft Start	Yes					
Reset and Power Fail	Yes					
Synch	Yes					
Crowbar	No					
Package Max. $R_{th\ j\text{-}case\ (pin)}$ $R_{th\ j\text{-}amb}$	Multiwatt15 1°C/W 35°C/W	Multiwatt15 1°C/W 35°C/W	Multiwatt15 1°C/W 35°C/W	Powerdip 16+2+2 12°C/W 60°C/W	Powerdip 16+2+2 12°C/W 60°C/W	SO20L 6°C/W 80°C/W

APPLICATIONS

Even though the regulators of the L4970A family has been designed to work only in step down configuration we will see next how these regulators can be use in large range of applications.
In same cases the L4970A device will be used as an example for the entire family assembled in Multiwatt package and the L4974A will be used for the types in powerdip package.

Anyway the suggested applications can be extended to any other device of the family by adjusting if necessary the external components using the given equation for the calculation.

Typical Application

The Fig. 29 shows the electrical diagram of the typical application, complete with all the auxiliary functions. The same application suggested in the data sheet as test circuit and is the same used for the final dynamic test. All our devices are 100% tested both in static and dynamic conditions.

Included in the dynamic test are obviously the external components: the coil, catch diode and output capacitor which have been defined for all regulators.

Shown below are the electrical diagrams of 5 devices that compose the family of this regulator complete with the value of the external components and with the relative pcb layout.

Output voltages higher than 5.1V are possible using an output resistive divider. For V_o > 24V, for safety reasons it must be avoided the zero load condition. In the application with high current, connected to the output divider are added two other resistances that permit the separation of sensing and forcing, in such way as to compensate the fall of voltage on the connecting cables between the output and the load.

Connecting directly the output to the feedback pin a 5.1V ±2% is obtained. The following table can be help for a rapid calculation of a resistor divider to obtain some of the most standard output voltage.

Figure 29: L4970A Typical Application Circuit.

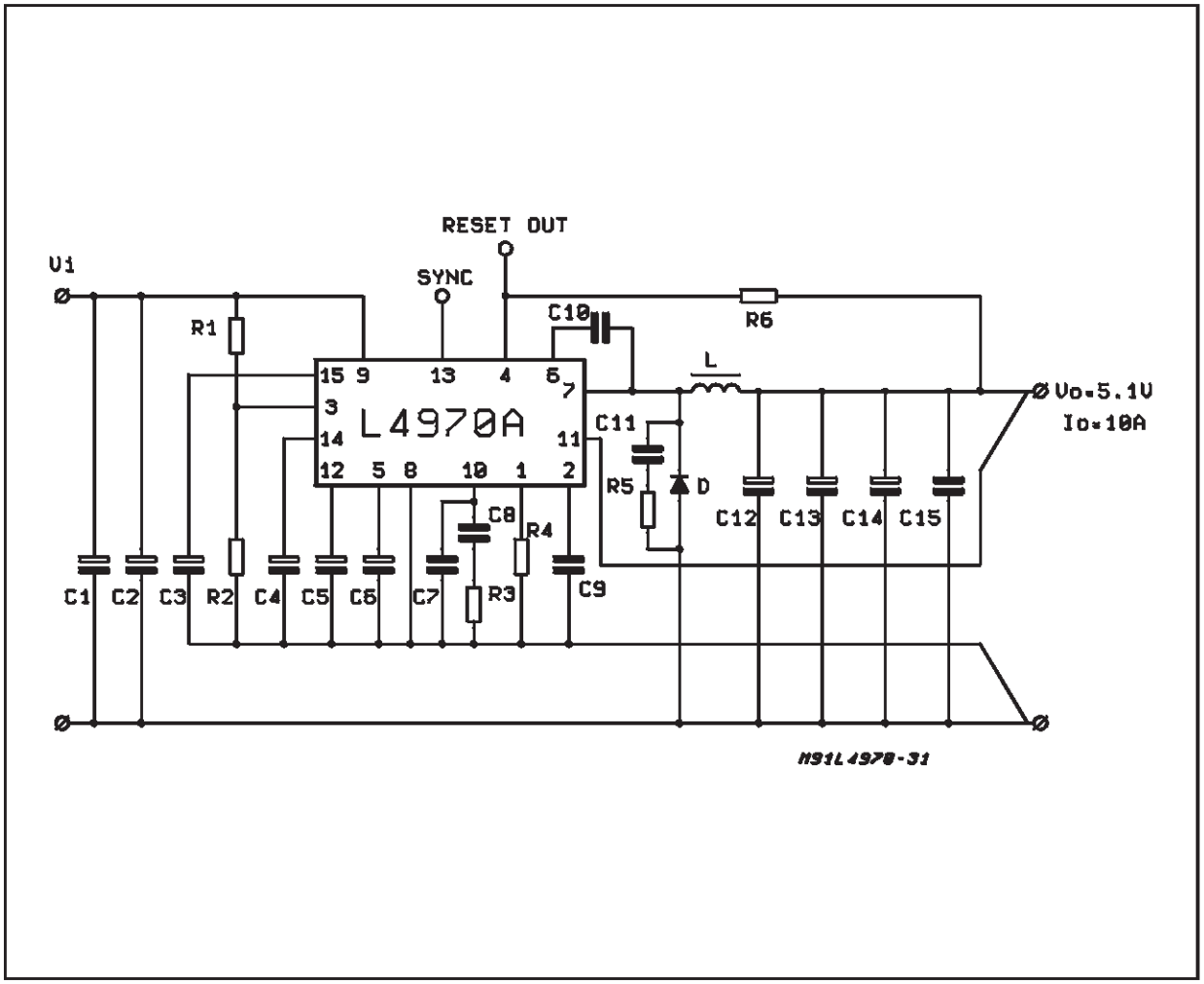
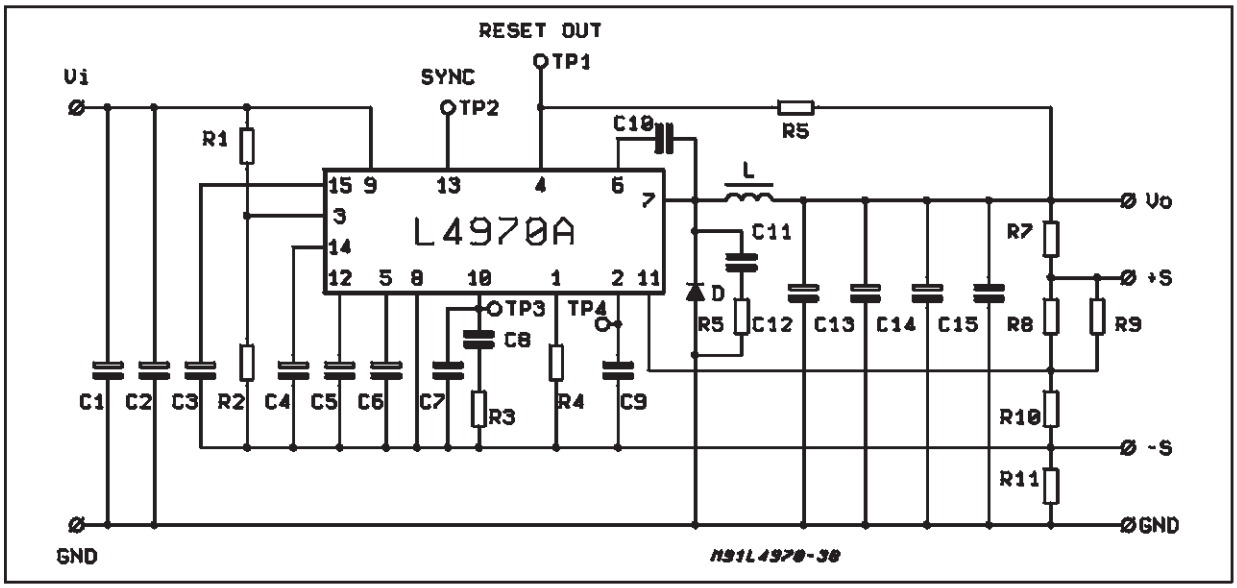


Figure 30: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 10A)
For component values, refer to test circuit part list.

PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 31: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 30. (1:1 scale)

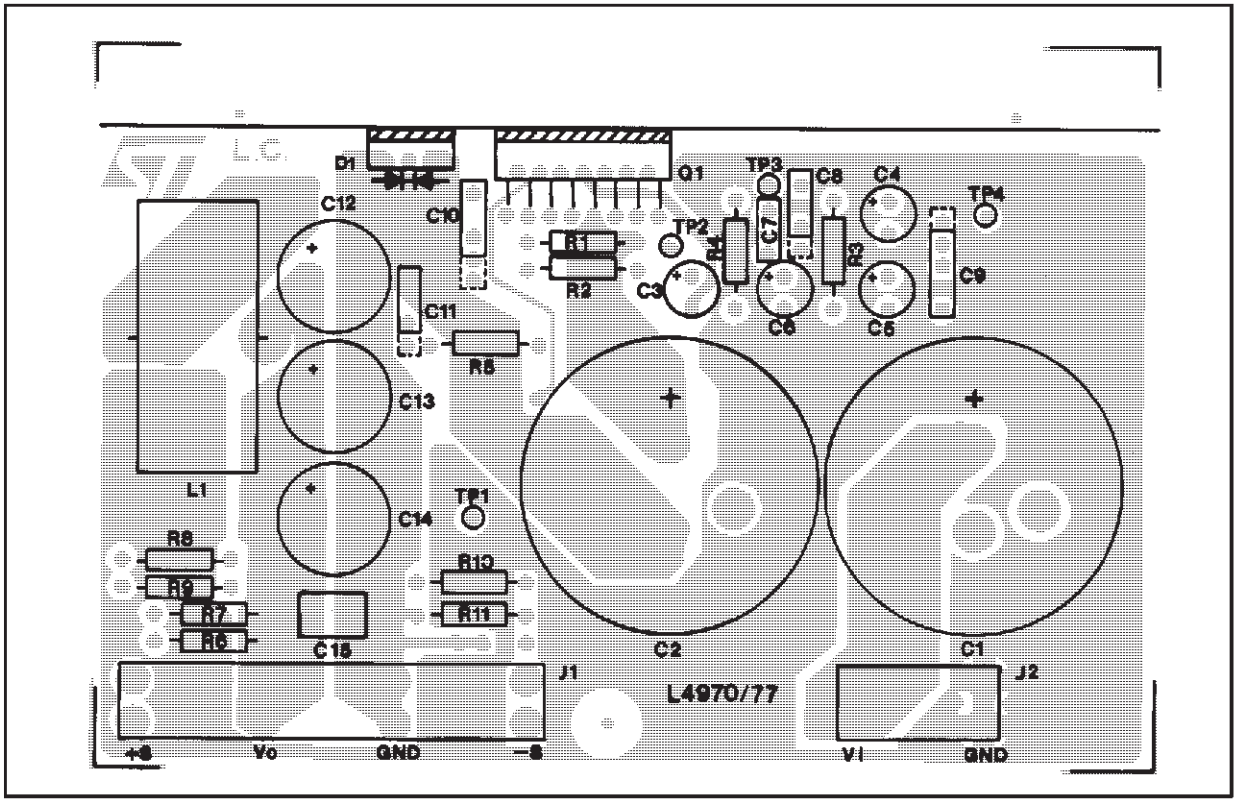


Figure 32: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 30. (1:1 scale)

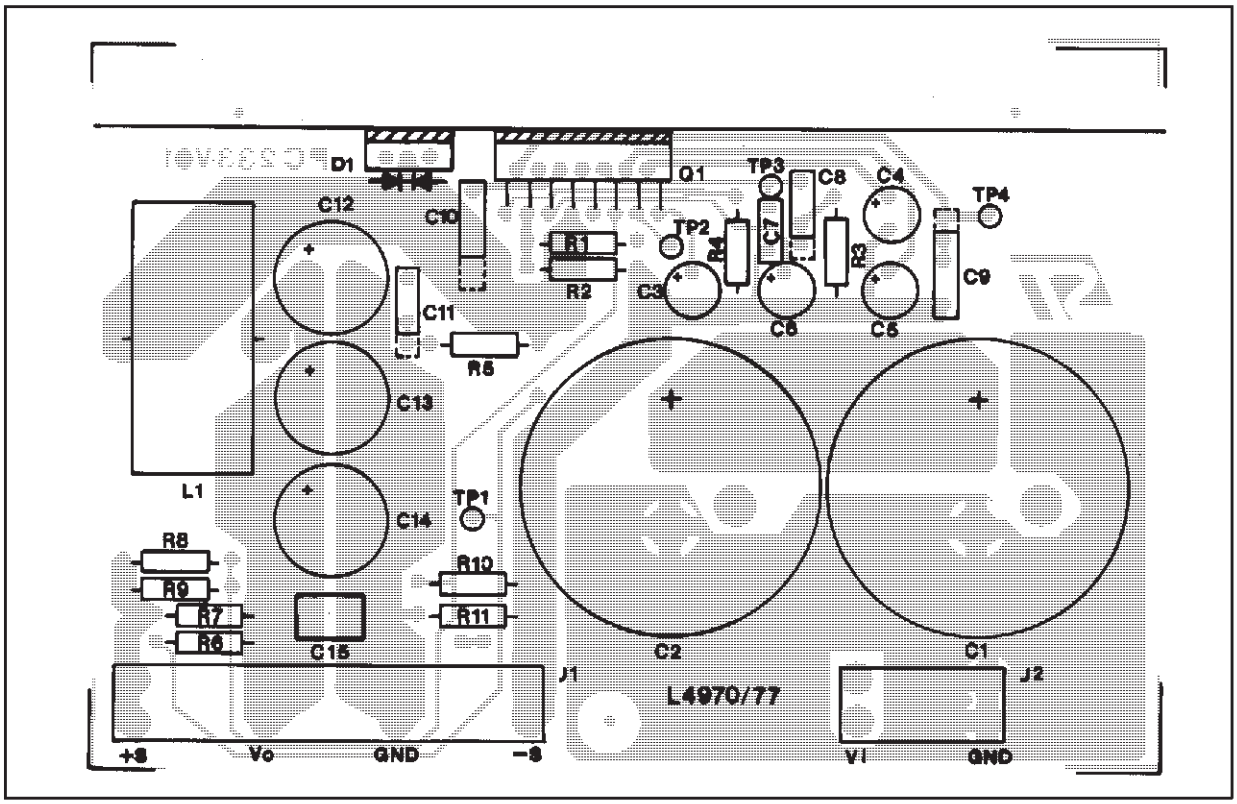
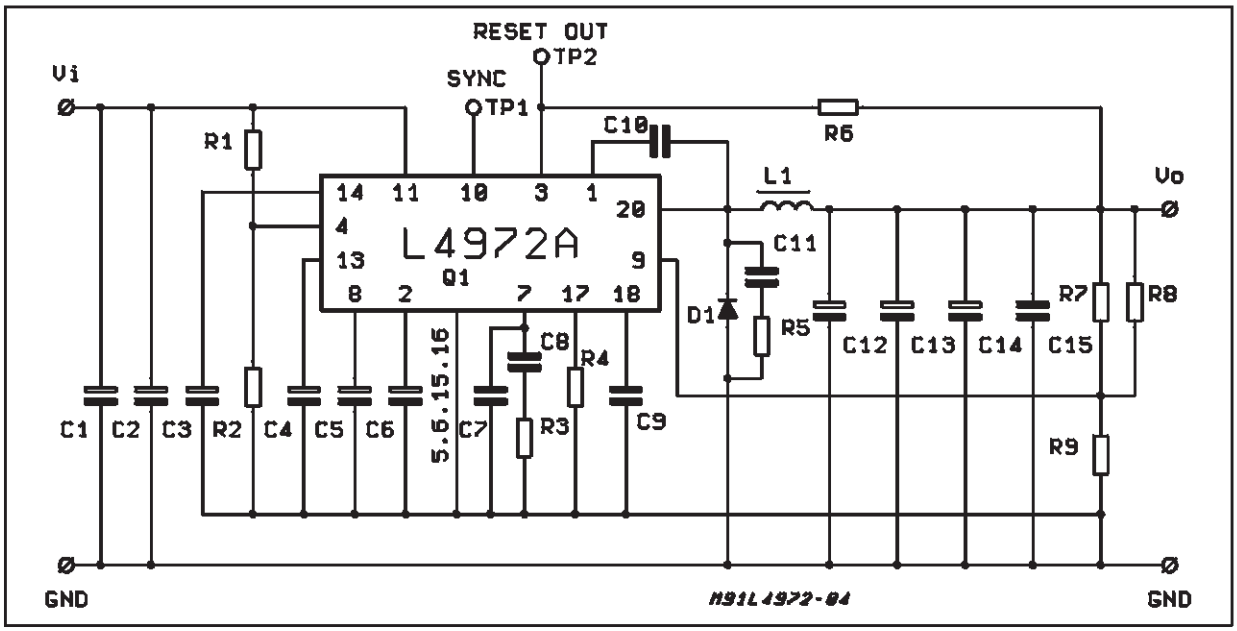


Figure 33: Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 2A ; f_{sw} = 100KHz)
$V_{o\ RIPPLE}$ = 30mV (at 1A)
Line regulation = 12mV (V_i = 15 to 50V)
Load regulation = 7mV (I_o = 0.5 to 2A)
for component values Refer to the fig. 32 (Part list).

PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film
D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B

SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 34: Component Layout of fig. 33 (1:1 scale). Evaluation Board

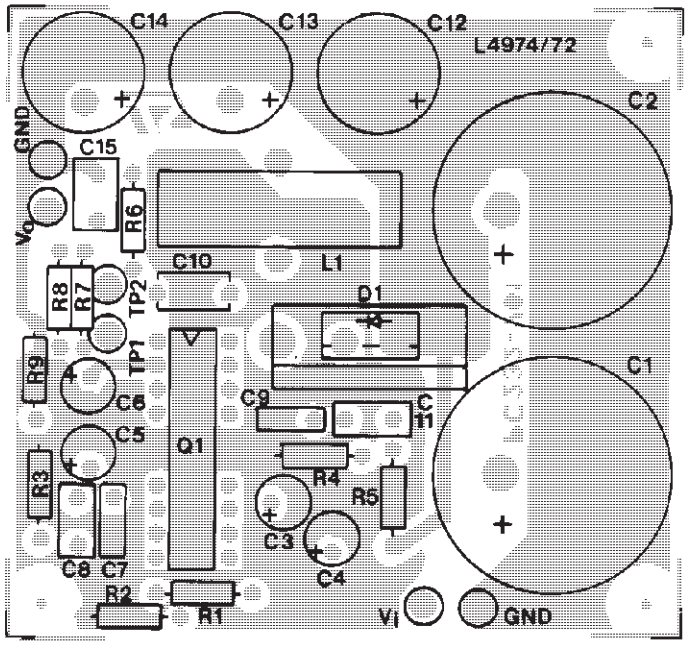


Figure 35: P.C. Board and Component Layout of the ciruit of fig. 33. (1: scale)

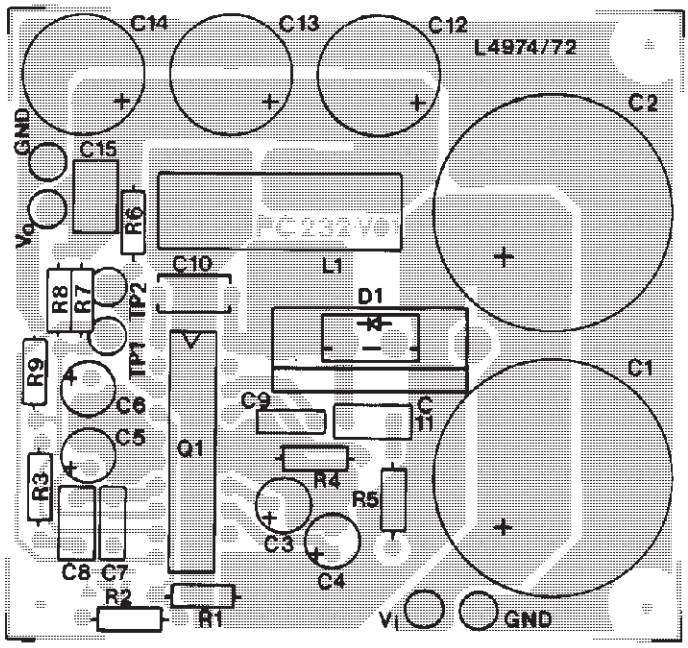
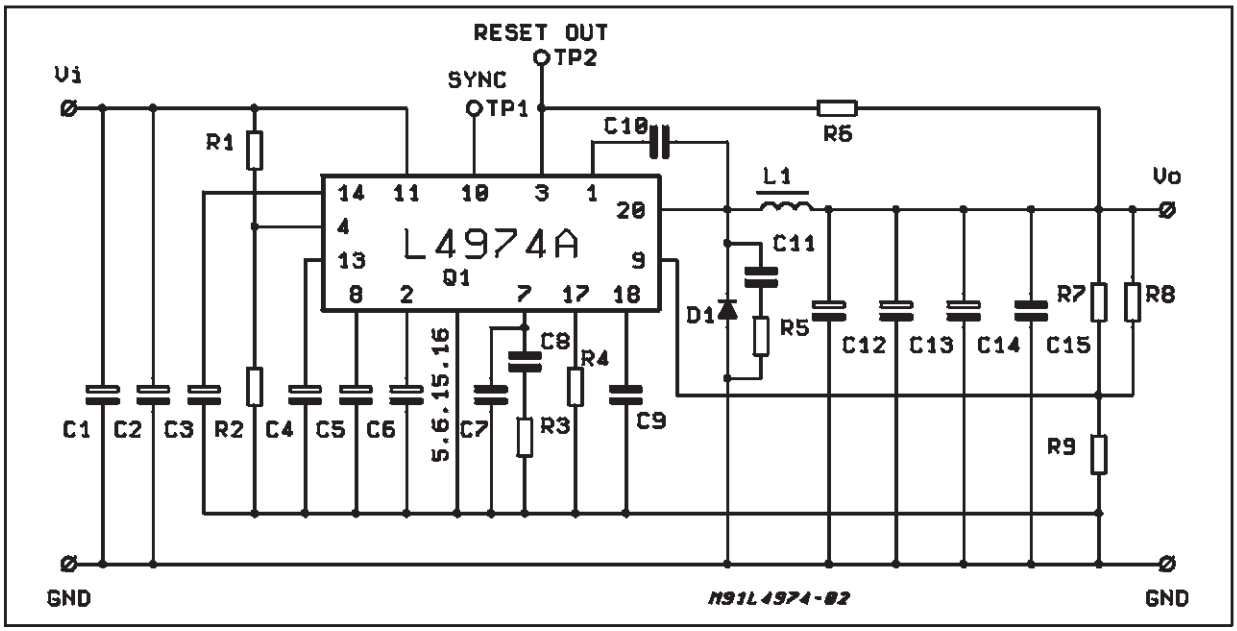


Figure 36: Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 3.5A ; f_{sw} = 100KHz)
$V_{o\ RIPPLE}$ = 30mV (at 1A)
Line regulation = 12mV (V_i = 15 to 50V)
Load regulation = 7mV (I_o = 0.5 to 3.5A)
for component values Refer to the fig. 35 (Part list).

PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film
D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B

SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Figure 37: Component Layout of fig. 36 (1:1 scale). Evaluation Board

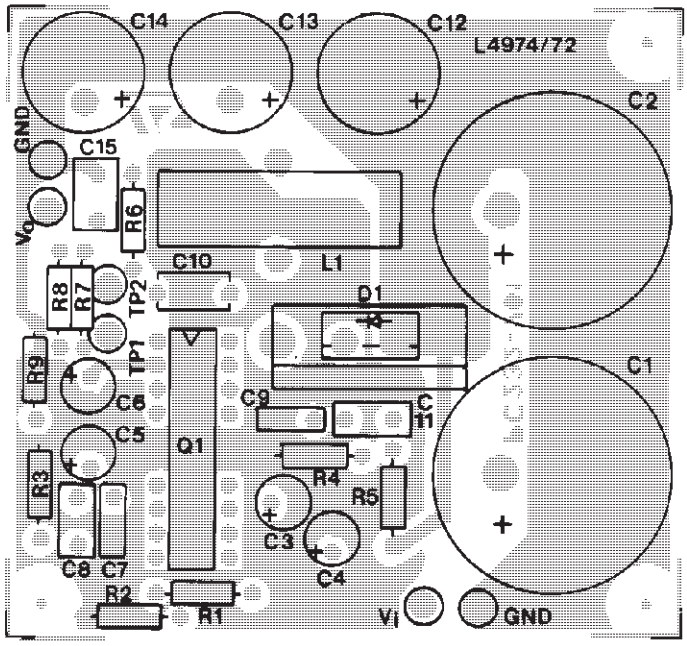


Figure 38: P.C. Board and Component Layout of the ciruit of fig. 36. (1: scale)

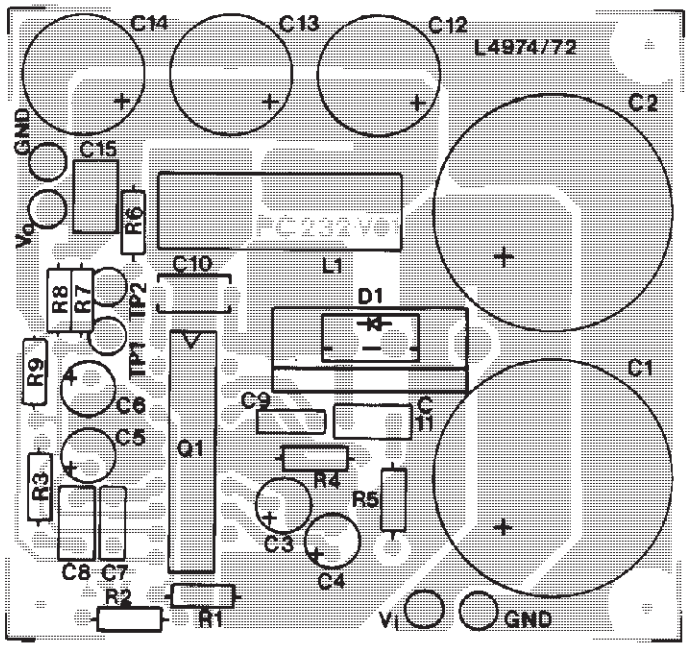
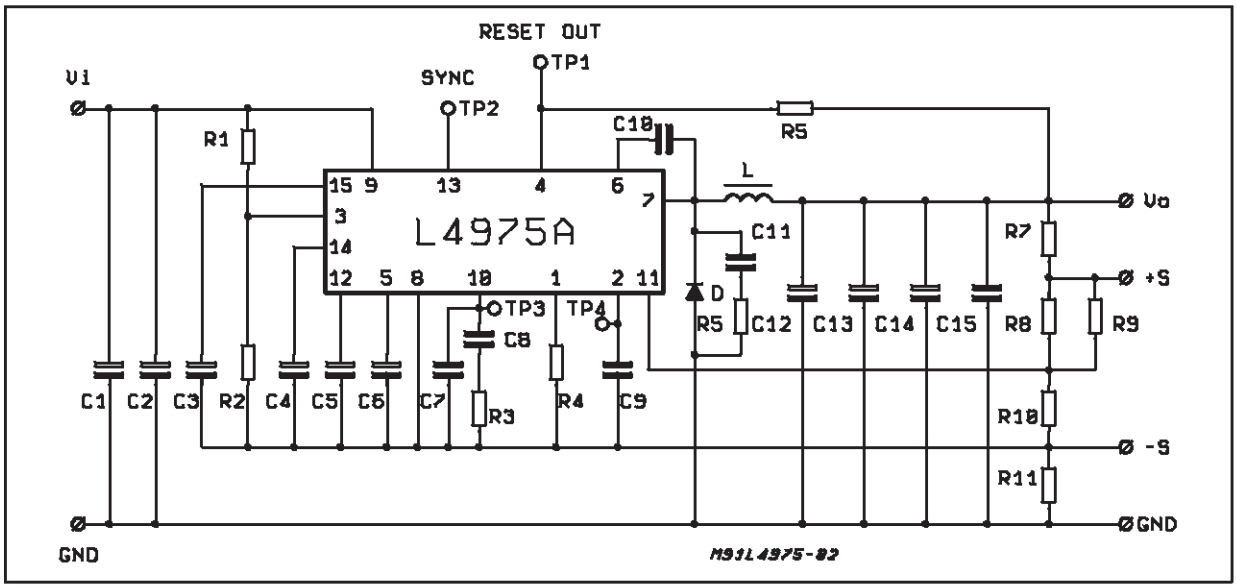


Figure 39: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 5A)
For component values, refer to test circuit part list.

PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 760CT (or 7.5A/60V or equivalent)	
L1 = 80µH	core 58930 MAGNETICS 47 TURNS Ø 113mm (AWG 76) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 40: P.C. Board (component side) and Components Layout of Figure 39. (1:1 scale).

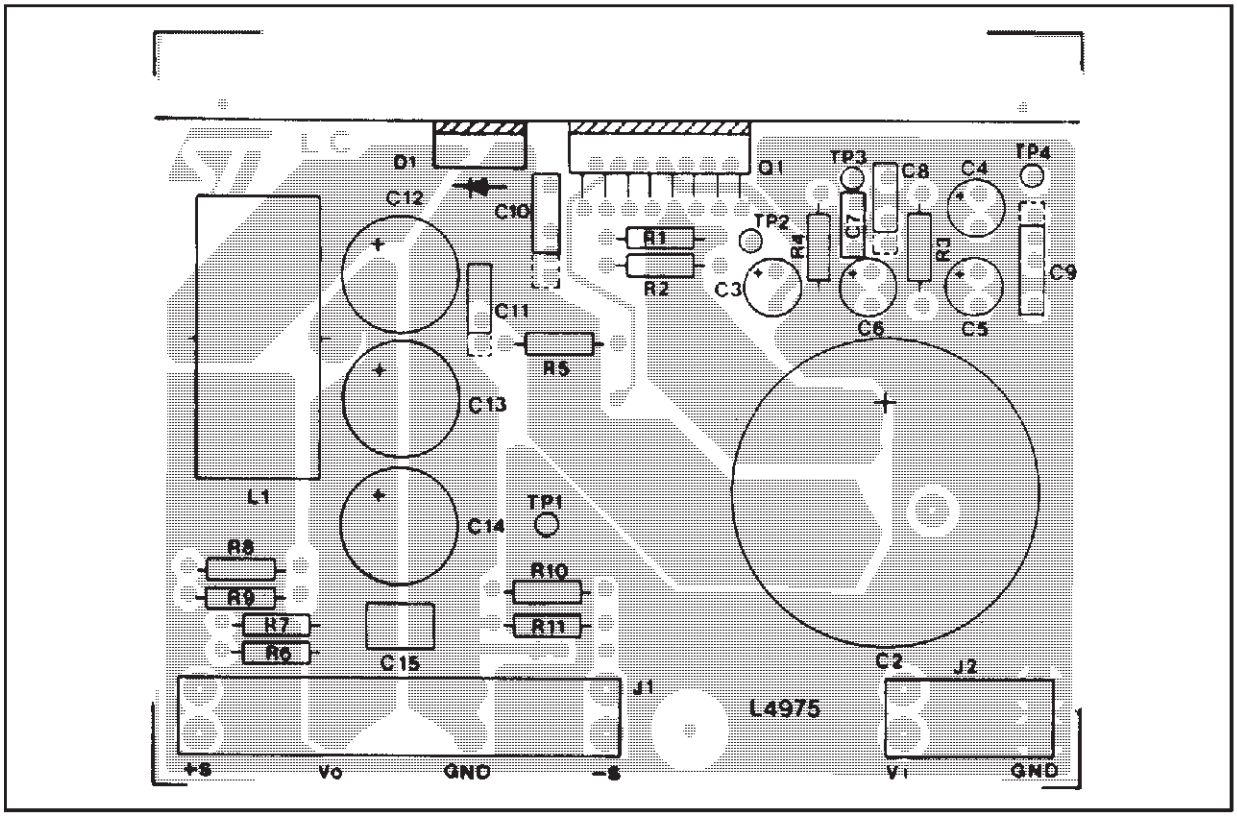


Figure 41: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 39. (1:1 scale)

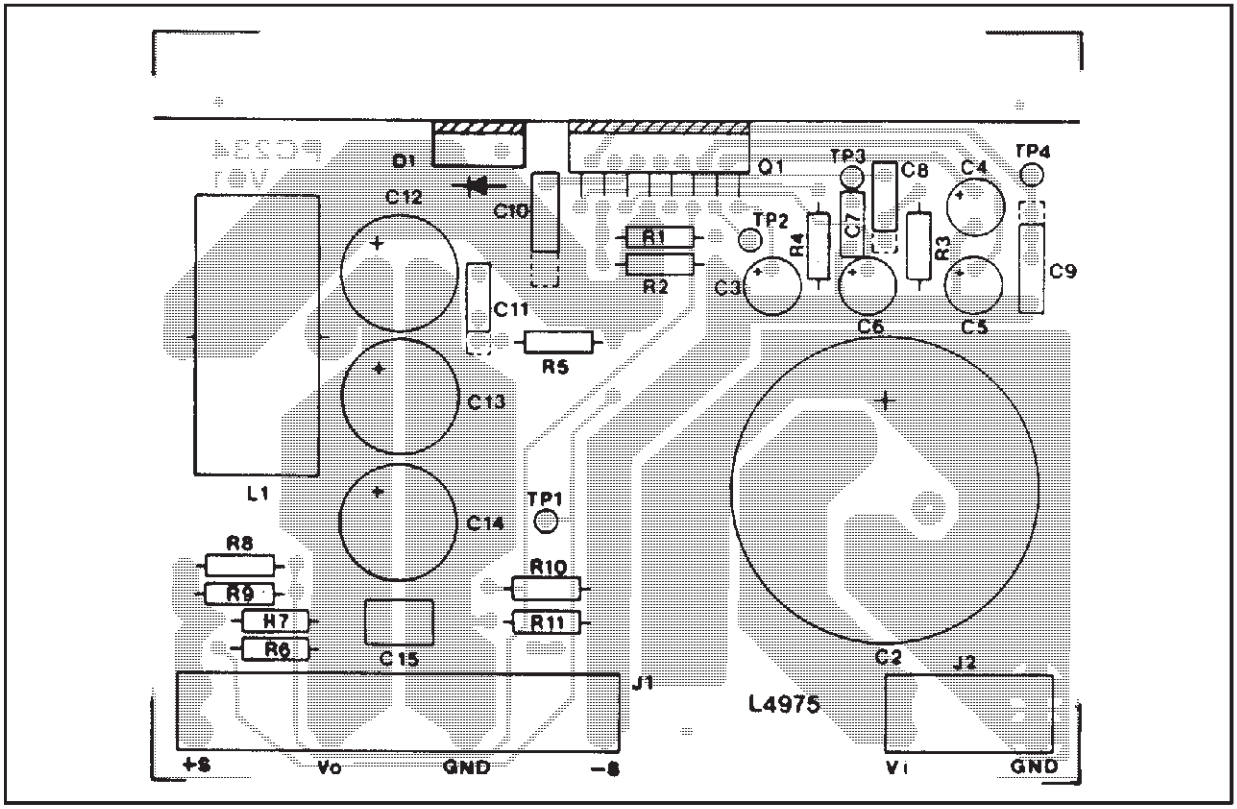
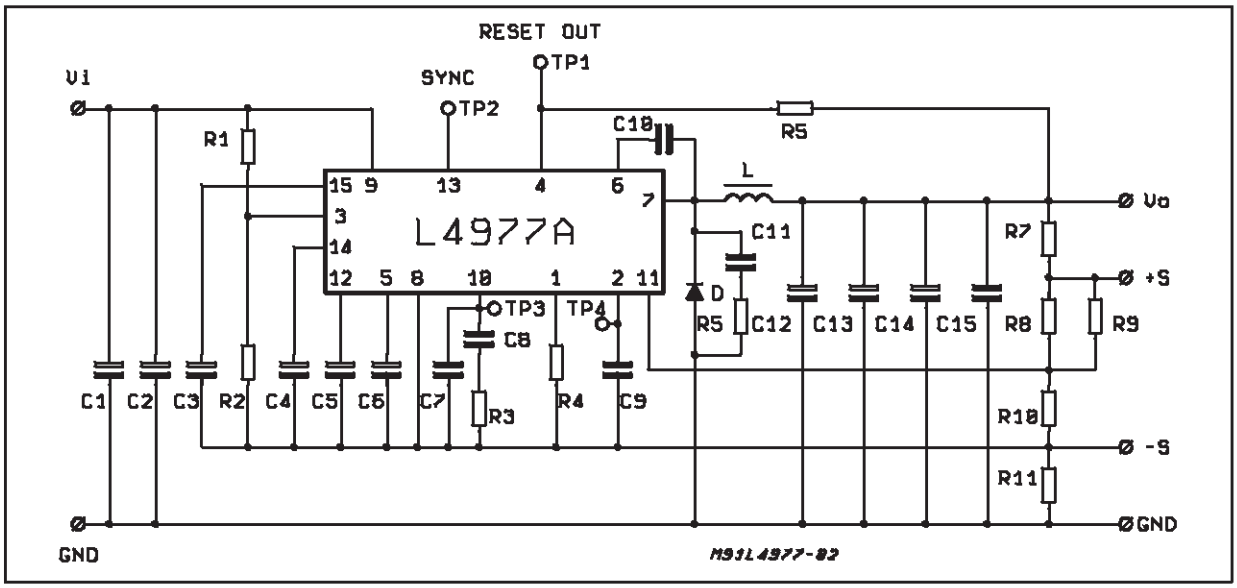


Figure 42: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 7A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 7A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 7A)
For component values, refer to test circuit part list.

PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 43: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 42. (1:1 scale)

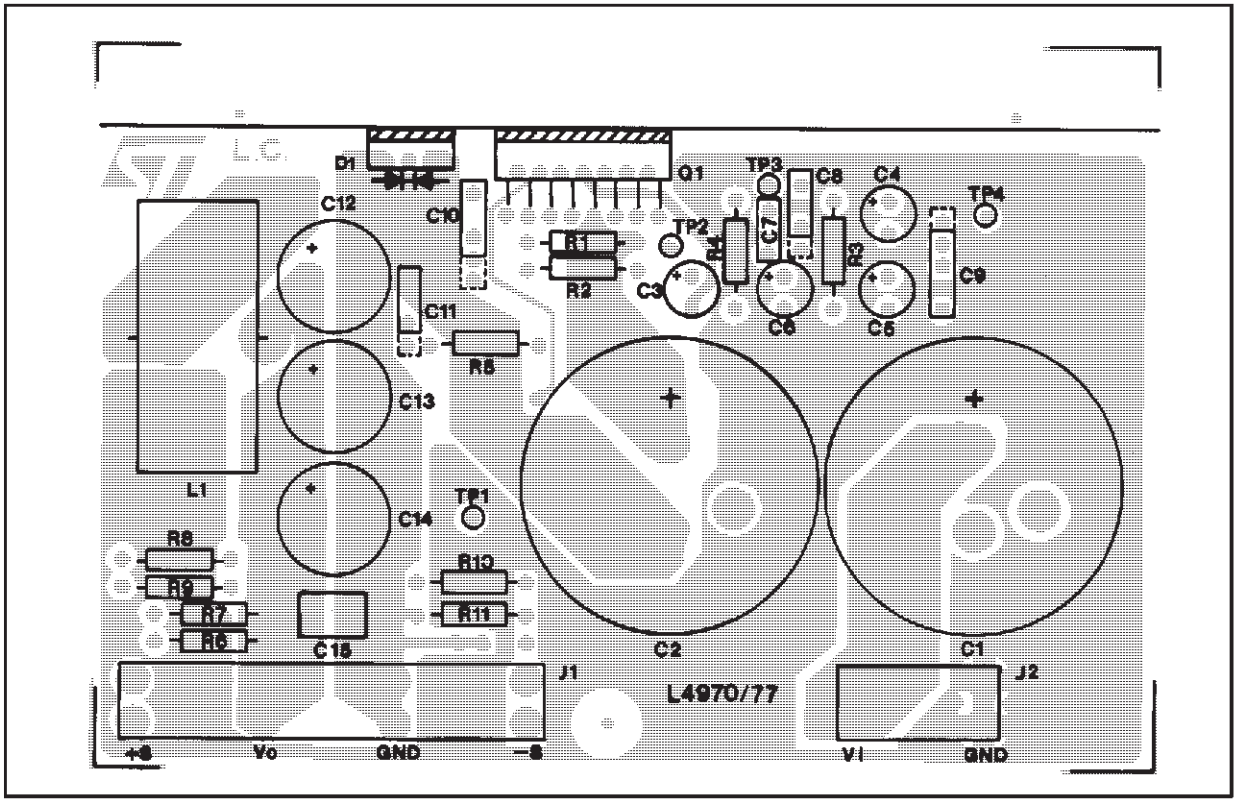
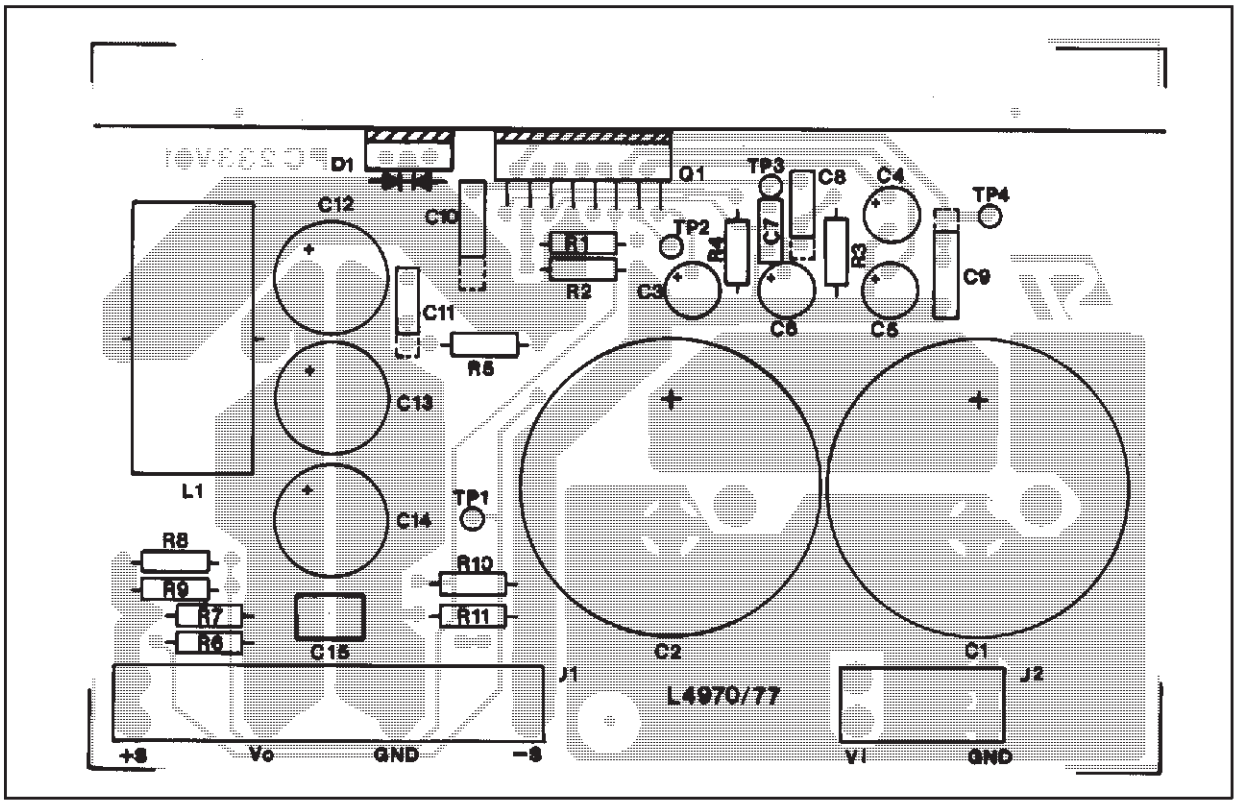


Figure 44: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 42. (1:1 scale)



Resistors value for standard output voltages.

Vo (V)	Rx (kΩ)	Ry (kΩ)
12	4.7	6.2
15	4.7	9.1
18	4.7	12
24	4.7	18

Rx corresponds to R9 for L4974A and L4972A

Ry corresponds to R10 for L4970A, L4977A and L4975A

Rx corresponds to R7 for L4974A and L4972A

Ry corresponds to R8 for L4970A, L4977A and L4975A

The suggested switching frequency, and used in the dynamic tests, is 200KHz for the Multiwatt® package (MW) and 100KHz for the powerdip plastic package (PDIP). The maximum switching frequency allowed is 500KHz.

For the types in plastic package (Powerdip), the lower switching frequency suggested is only depended by the minor dissipating power of a plastic package versus a "power package" because it is well known that switching losses are directly proportional to the commutation frequency.

Higher switching frequencies are possible if limited output current is required and the operating ambient temperature are lower than 70°C. Infact the oscillator of the devices assembled in dual in line is completely equivalent to Multiwatt® package.

Figure 45: Oscillator waveform and sync. pulse for V_i = 35V

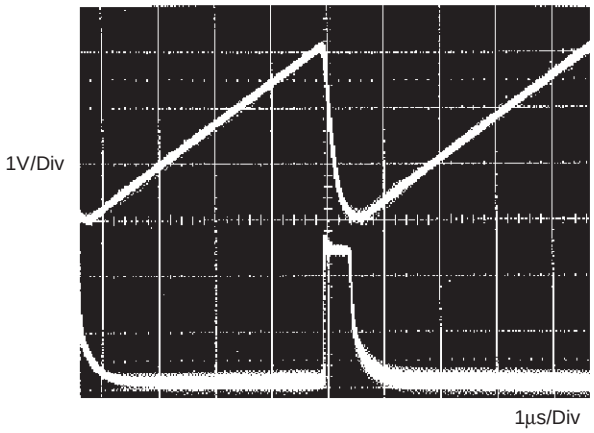


Figure 46: Oscillator waveform and sync. pulse for V_i = 15V

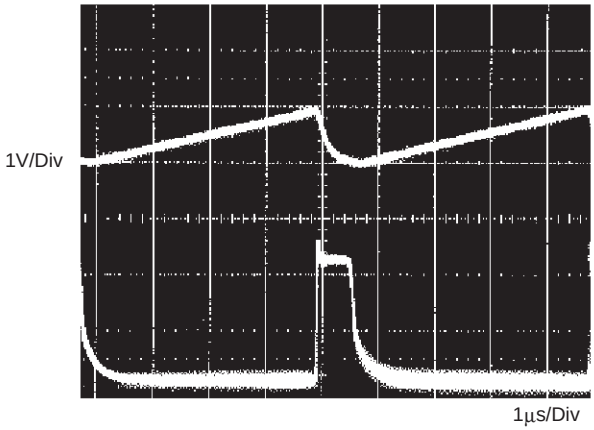
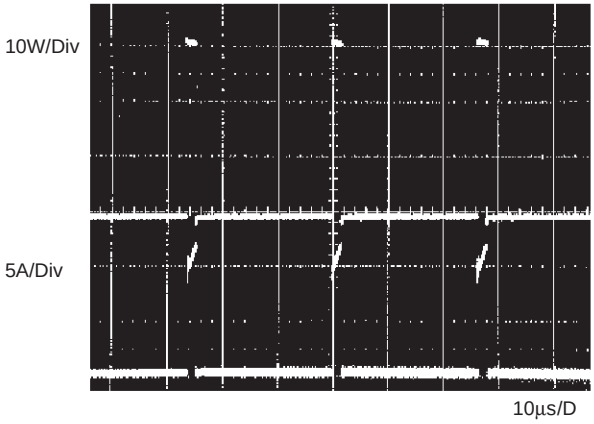


Figure 47: Oscilloscope photograph showing the short circuit output voltage and current waveforms.



The most important external components which need a little more attention (because a properly dimensioning affects on the performance of the application) are the input and output capacitors, the freewheeling diode and the coil.

INPUT OUTPUT CAPACITORS

The output voltage ripple ΔVo, essentially depends on the current ripple in the coil and the ESR of the output capacitor at the switching frequency.

The capacitor that present a low ESR are capable of supporting higher current ripples.

Today, the majority of the constructors of electrolithic capacitors offer in their data book also a wide range of "low ESR" types generally suggested for switching power supply application.

In our case EKR and EKE series (ROE) has been preferred.

Such a series capacitors are designed for applications at high frequency, 200KHz, and built to have a low ESR in order of supporting high current ripple.

In order to minimize the effects caused by the ESR of the capacitors on the output voltage ripple 3 capacitors of 220uF/40V (for high output current application) are connected in parallel.

It is necessary much attention also into the choice input capacitors. Also them be at low ESR, because they must sustain high current ripples. Such current ripples in presents of an inadeguate ESR, would produce a heating of the capacitor itself (which could affect on the reliability of the component, since in general it is sensitive to temperature. Therefore choosing input capacitor at low ESR is necessary for problems of reliability.

In fact such capacitors, when used in applications that make use a mains transformer, must support quite elevated peak current for short periods a double the mains frequency and the same time be capable to deliver the instantaneous peak of energy to the load at the switching frequency.

Some other considerations of a general nature can be done on low ESR capacitors. For example of equal value and type (i.e.: 220µF - EKR), the ESR of the capacitor decreases at the increasing of its value voltage rating, just like its RMS current.

Still, two capacitors of the same value, connected in parallel, withstand an RMS current higher then the only one of double value, and with the same voltage rating.

When however, more capacitors are connected together in parallel, it is important to design with care the layout of the printed circuit, in order to distribute as eventy as possible amongst between the different capacitors the total current ripple. This is used to avoid dangerous current unbalances in the distribution of the total current between the various capacitors charging some more others, that could damage the reliability of the system.

Often it is very difficult to know exactly the RMS current flowing throught the capacitors. To know if the operating condition is a "safe"operating condition or not, a measurement of the package temperature of the capacitor should be done.

The following table 1 and 2, included in the databook of electrical Roederstain, shows the maximum RMS current sustainable by the EKR and EKE capacitor versus the ambient temeperature and overtemperature allowed on the capacitor package.

Table 1.

Low-voltage electrolytic capacitors for switch-mode power supplies with low impedance values, radial, polarized styles.

(EKR)

Rated cap. (µF)	Rated volt. (V DC)	Dimensions D x L (mm) (nominal dimensions)	Dissipation factor tan δ (100Hz; 20°C) Lim. Values	Impedance Z (Ω) (10KHz; 20°C) (Lim. values)	Impedance Z (Ω) (10KHz; 20°C) (Lim. values)	Admissible ripple curr. (mA/100Hz) 85°C	Admissible ripple curr. (mA_{eff}/10-100Hz) 85°C
100	10	8.7 x 12.7	0.12	0.85	0.65	160	250
220	10	10 x 12.7	0.12	0.39	0.31	300	450
470	10	10 x 20	0.12	0.20	0.18	530	800
100	16	10 x 12.7	0.11	0.60	0.40	200	300
220	16	10 x 16	0.11	0.32	0.25	350	550
470	16	12.5 x 20	0.11	0.16	0.13	600	900
100	25	10 x 12.7	0.09	0.5	0.35	250	400
220	25	10 x 16	0.09	0.25	0.17	450	700
470	25	12.5 x 20	0.09	0.13	0.09	650	1000
100	40	10 x 16	0.08	0.4	0.23	450	700
220	40	12.5 x 20	0.08	0.17	0.13	650	1000
470	40	12.5 x 30	0.08	0.09	0.08	1000	1500

(EKE)

Rated cap. (μF)	Rated volt. (V)	Dimensions D x L (mm) (nominal dimensions)	Dissipation factor tan δ (100Hz; 20°C) Lim. Values	Impedance Z (Ω) (100KHz; 20°C) (Lim. values)	Impedance Z (Ω) (100KHz; - 10°C) (Lim. values)	Impedance Z (Ω) (10KHz; - 40°C) (Lim. values)	Admissible ripple curr. (mA)100Hz 105°C
22	10	5 x 11	0.19	1.30	3.90	20	154
33	10	5 x 11	0.19	1.30	3.90	20	154
47	10	5 x 11	0.19	1.30	3.90	20	154
100	10	5 x 11	0.19	1.30	3.90	20	1 54
220	10	6.3 x 11	0.19	0.60	1.80	9.80	260
330	10	8 x 11.5	0.19	0.33	0.99	5.80	400
330	10	8.5 x 12.5	0.19	0.33	0.99	5.80	400
470	10	8 x 11.5	0.19	0.33	0.99	5.80	400
100	16	6.3 x 11	0.16	0.60	1.80	9.80	260
220	16	8 x 11.5	0.16	0.33	0.99	5.80	400
220	16	8.5 x 12.5	0.16	0.33	0.99	5.80	400
330	16	8 x 11.5	0.16	0.33	0.99	5.80	400
470	16	10 x 12.5	0.16	0.25	0.75	3.20	510
100	25	6.3 x 11	0.14	0.60	1.80	9.80	260
220	25	8 x 11.5	0.14	0.33	0.99	5.80	400
330	25	10 x 12.5	0.14	0.25	0.75	3.20	510
470	25	10 x 16	0.14	0.19	0.57	2.20	635
100	35	8 x 11.5	0.12	0.33	0.99	5.80	400
100	35	8.5 x 12.5	0.12	0.33	0.99	5.80	400
220	35	10 x 12.5	0.12	0.25	0.75	3.20	510
330	35	10 x 16	0.12	0.19	0.57	2.20	635
470	35	10 x 20	0.12	0.14	0.42	1.50	860

Table 2: Admissible ripple current.

Ambient Temp. δ_u in °C	Admissible % of the 85°C value	Surface Temp. in °C	Admissible % of the 105°C value	Surface Temp. in °C
≤ 40	220 %	55	230 %	55
45	210 %	59	220 %	60
50	200 %	63	210 %	64
55	190 %	67	200 %	68
60	180 %	70	190 %	72
65	170 %	74	180 %	76
70	155 %	77	170 %	80
75	140 %	81	160 %	84
80	120 %	84	150 %	88
85	100 %	88	140 %	92
90	90 %	92	130 %	96
95	80 %	97	120 %	100
100	70 %	101	110 %	104
105	60 %	106	100 %	108

CATCH DIODE

Because of quickly rise and fall time of the current (about 40-50ns) the use Schottky diode is reccomanded. Ultra-fast diodes with 30-50ns of trr (reverse recovery time) are not considered sufficiently fast for this family of converters, since they would give too elevated peaks of current at the turn on of the internal power transistor, so high thatcould affect the reliability of the complete system, as well as drastically reduce the efficiency. The oscilloscope photographs show the Output Voltage and Output Current waveforms obtained with diode having different trr value.

Figure 48: Schottky Diode.

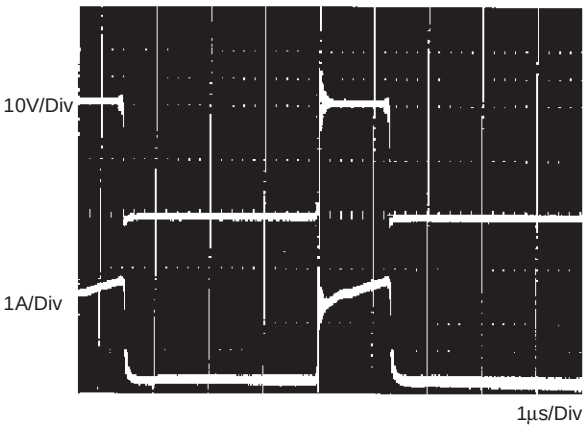
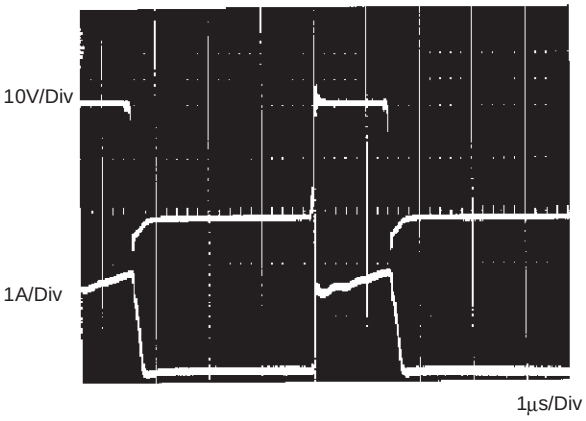


Figure 49: Ultra Fast Diode (trr < 100ns).



In the test circuits used for this family of converters, Schottky diodes from 60V (breakdown reverse voltage) are suggested since the device can support a max. input power voltage of 55V (for specific applications, Schottky diodes with a reverse breakdown voltage higher or equal to the maximum supply voltage should be used), with current rating and packaging to satisfy all the conditions of duty cycle, and therefore also of power dissipation.

COIL

Concerning the coil, a molypermalloy toroidal cores has been suggested, so that it would be easy for everybody to obtain samples, wrap them with a right number of turns in order to evaluate and correlate the measurements and performance of the devices.

In addition since the devices are dynamically tested 100% in production, with a "jig" of testing which uses the same coil suggested in the applications, in the case of contests for example on a guaranteed parameter like the efficiency, should be easier to solve the objections; in this case should be remembered that changing the magnetic material, the dimension, the wire and the number of the winding, also change the losses in the coil reducing the total efficiency of the application.

This can be easily verify using for example toroidal cores in iron powered rather that those suggested in molypermalloy.

Moreover, it is important to dimension properly the coil in order to avoid its saturation, a good choice is to dimension that its saturation; current is not equal to the maximum nominal current capable to deliver to the load, but rather higher by about 20% then the maximum guaranted current of the device, in short circuit condition.

Only in this way it is possible to guarantee that the coil never saturate in all the possible working conditions, i.e.: in presence of a load transient, in short circuit in output and in the case of elevated temperature of the magnetic part.

At last, it should be remembered that the suggested inductors values, are referred to the inductors values that the coil must have at the maximum output current of the application. Oscilloscope Photographs showing the device output voltage and current waveforms obtained with different inductor.

Figure 50: Waveforms for L = 50µH

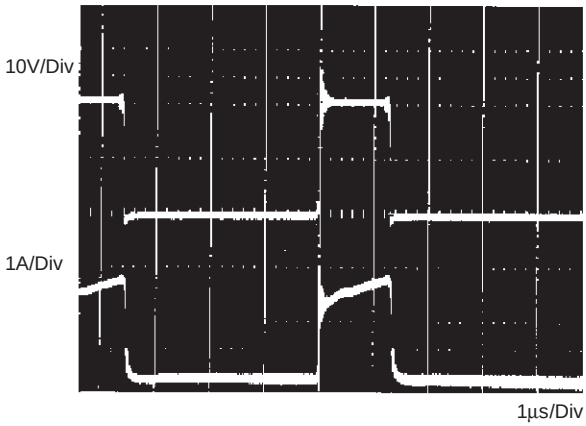


Figure 51: Waveforms for L = 230µH

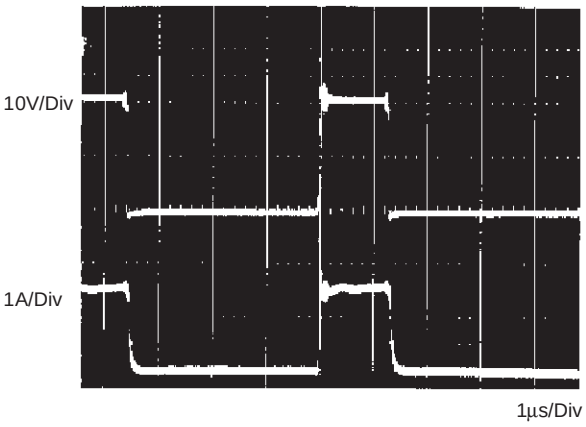
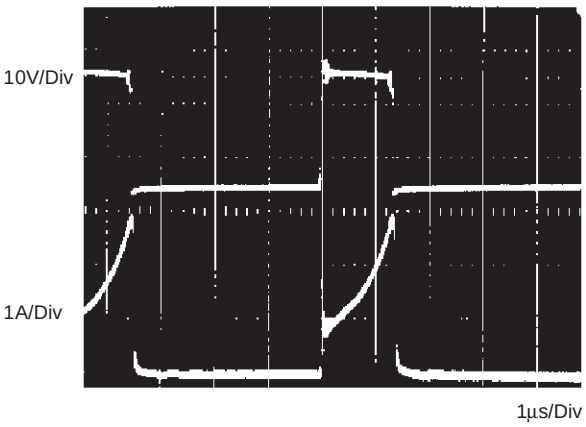


Figure 52: Waveforms in case of core saturation



Anyway some general rules should be observed in order to avoid any "poor functioning". These rules include:

a) the catch diode, that further to be the suggested type in the test circuit, it has to be assembled on the printed circuit very close to the output of the regulator, in order to minimize the leakage inductance and avoid over voltage due to the long connection:

b) The inductor, avoiding the saturation at the maximum current guaranted by the current limitation of the device.

If oscillations on the output voltage at low ambient temperature (i.e.: below 0^{o}C) are originated an output low ESR capacitor has to be used.

Oscillations on the output al low frequency indicate instability of the control loop; in this case a changing of the network compensation is suggested (see Error Amplifier section).

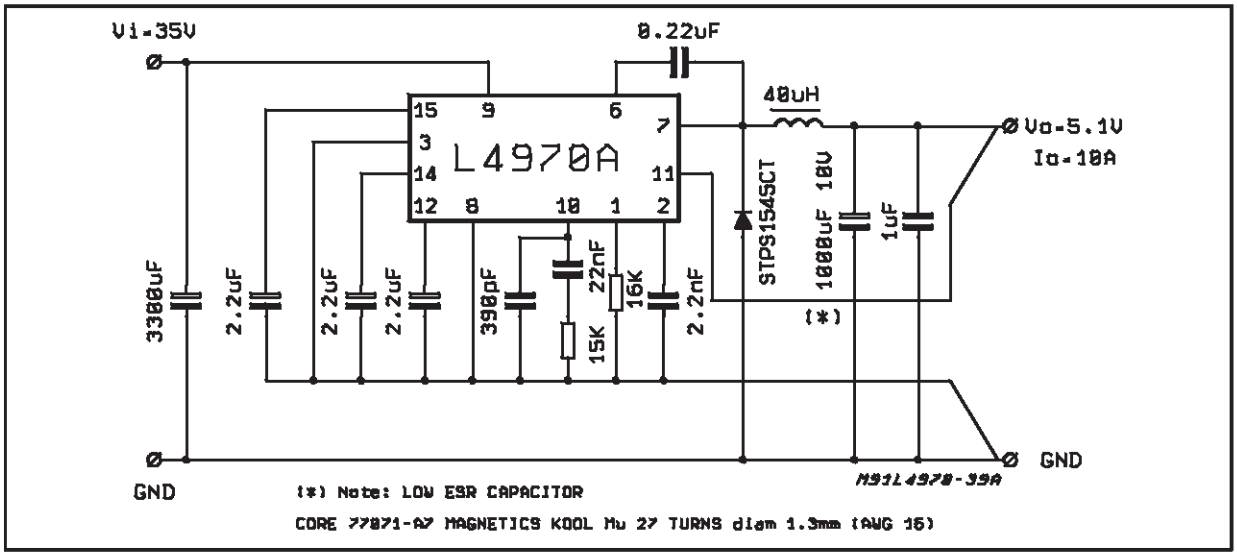
LOW COST APPLICATION

The fig. 53 shows the low cost application of a power supply of 10A and 5.1V.

In comparison of the complete application (and this is valid for all the devices of the family) the external components relative to the reset and power fail functions can be missed.

When a lower output voltage ripple is not required it is possible to eliminate the capacitors connected at the reference voltage pin of 5.1V (i.e.: pin 14 for Multiwatt package. pin 13 for plastic package)
The reset input pin is suggested to connect it to ground.
The soft start capacitor value can be reduced to 100nF for 5v output voltage.

Figure 53: Low Cost Application Circuit.



POWER SUPPLY COMPLETE WITH MAINS TRANSFORMER

The fig. 54 shown a power supply with mains 110/220Vac transformer, diode bridge and filter capacitor with output voltage adjustable between 5.1V. and 24V.

Output capacitors have to be chosen with low ESR in order to reduce the output ripple.Particular care has to be taken for input filter capacitors, in fact they have to support high current spikes at mains frequency and at the same time current peak bigger than the output current at the switching frequency.

Therefore they must be chosen with low ESR and able to substain high current ripple in order to guarantee a good reliability to all the system.

The trasformer can be chosen with a single winding and 4 diodes or a center tap with only 2 diodes with higher reverse voltage.

A cost reduction of the trasformer can be reached using an active power factor corrector.

It work at low voltage and the external components are relatively cheap, more details can be obtained looking on the power factor corrector application note.

POWER SUPPLY WITH MAINS HIGH FREQUENCY PREREGULATOR.

When it is necessary to eliminate the mains trasformer at 50/60Hz for reasons like weight, dimensions or cost, a high frequency preregulator can be used.

A ferrite trasformer reduces the rectifier and filtered mains voltage in a convenient voltage to supply directly the device, providing for the isolation requirements.

Using a free running solution or one of the voltage/current mode controller available, it is possible to compensate the input variation while the output voltage variations due to the load are usually very low. Some examples regarding how to use this regulator in off-line power supply are now showed:

Flyback Topology

Using a flyback topology with single or double transistors is possible to fix a single output voltage of 35-40V; it can be a bit increased if using a backup battery of 48 nominal Volts.
From this preregulator (±10%) tolerancevoltage is possible to get one or more indipendent outputs, with its own current limitation and thermal protection.

Moreover a possibility to syncronize more devices together is available, remembering to fix the master frequency at least 5% higher than the others device (working as slave) one.
In case of necessity is possible to synronize devices on the trasformer secondary with the swithcing frequency of the controller (See Fig. 55).

Figure 54: Typical power supply showing the mains transformer.

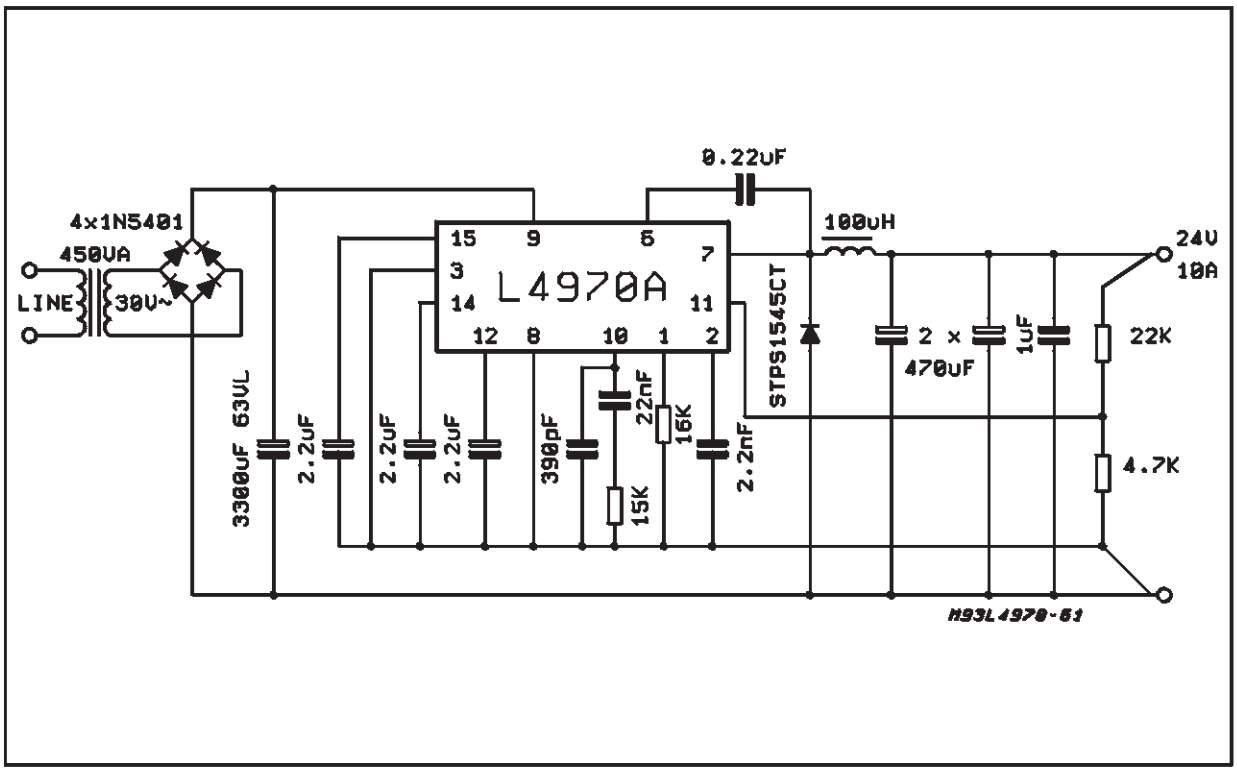
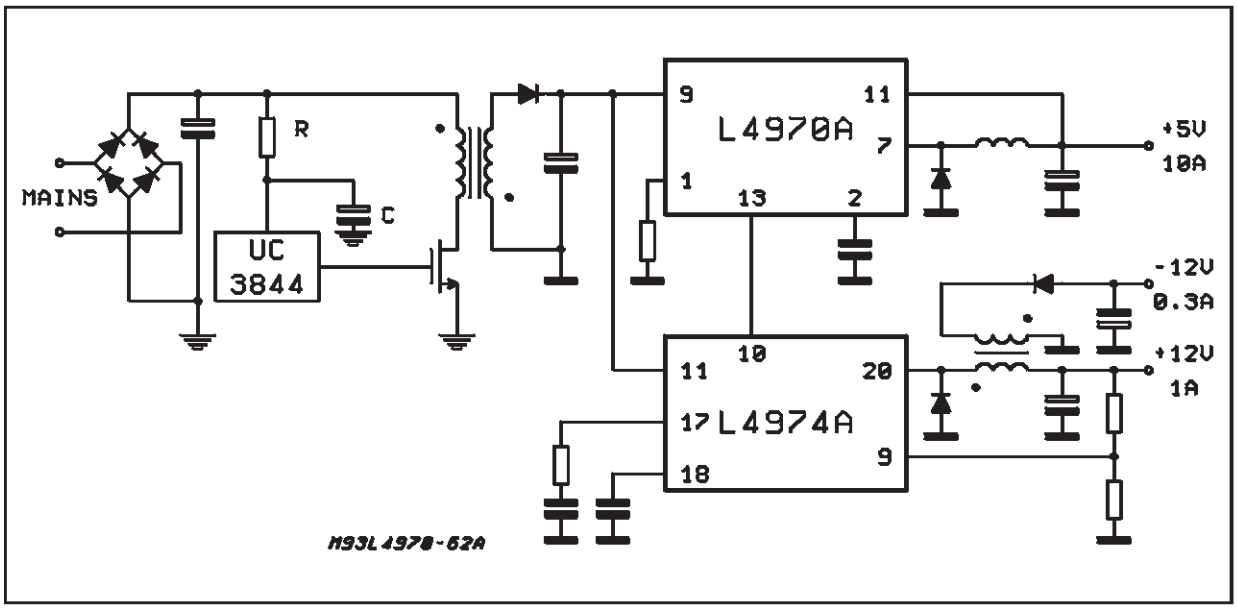


Figure 55.



Forward Topology

Further is showed an smps forward circuit, where the dc-dc converter is used as post-regulator for an auxiliary output, (35V.) while the main one (5.1V. or 3.3V) is controlled directly with the feedback (See Fig. 56).

Using a PFC preregulation

When an optimized power factor is required it is possible to use the following two pricinple diagram that make use of an active power factor corrector.

1) using the standard boost topology (Fig. 57)
2) using a flyback topology (Fig. 58)

The idea is that to generate a stabilized voltage, around 30V - 35V, already isolated, avoiding to use an isolation after the PFC section.

Figure 56.

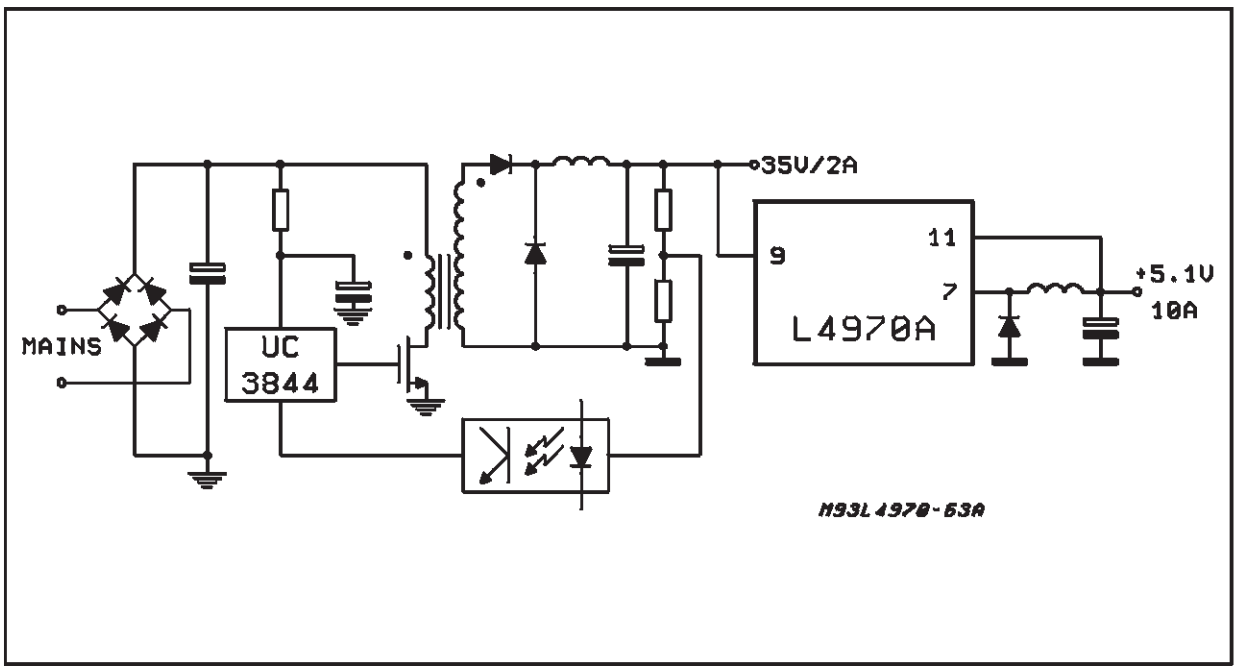


Figure 57.

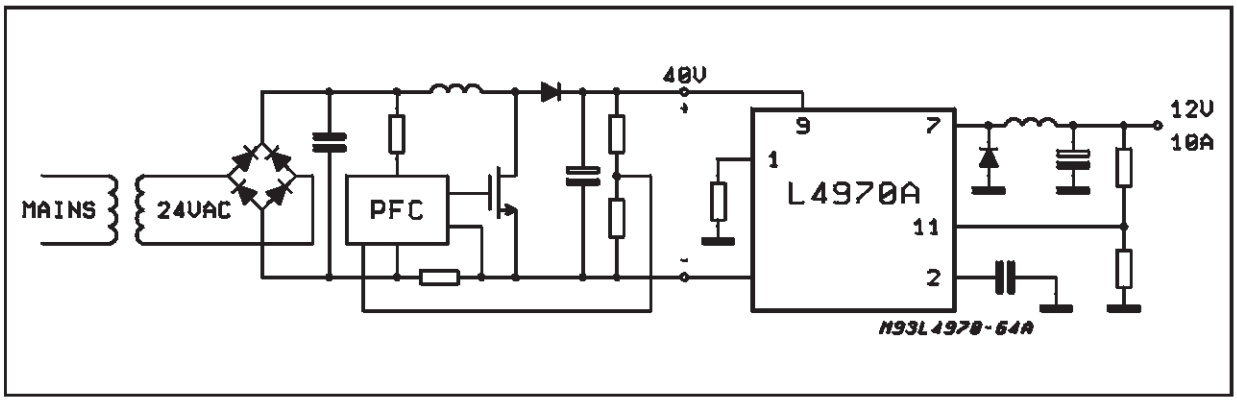
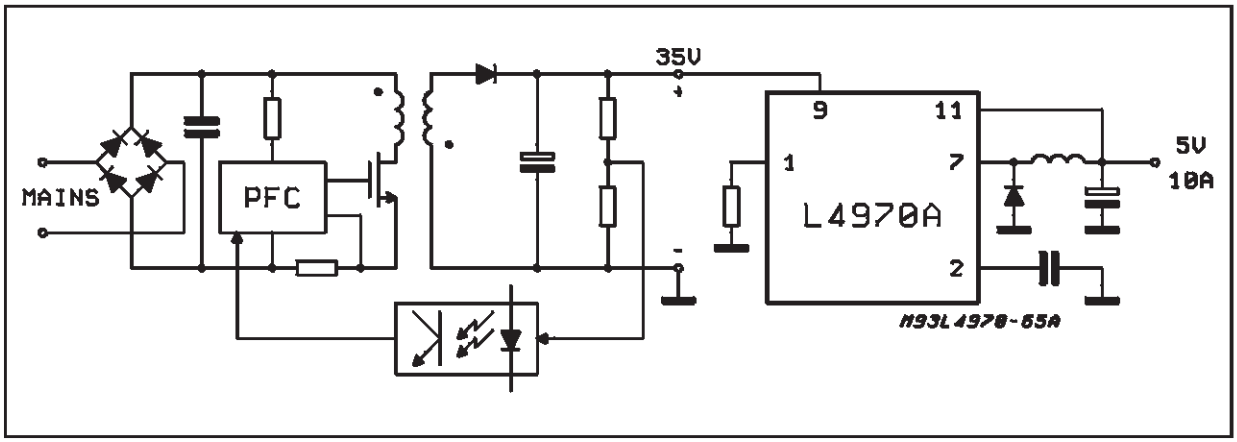


Figure 58.



POWER SUPPLY WITH 0 TO 25V ADJUSTABLE OUTPUT VOLTAGE

a) It is a classical solution with high performance that make use of a negative reference voltage equal to the value of the internal voltage of the device (5.1V).

To generate this negative reference voltage, it is useful to equip the mains trnsformer with another secondary winding at a low voltage of around 8Vac and capable of delivering a few dozen of mA.

During the phase of starting up and stopping of the mains, it is important to avoid generating oscillations around the value of the output voltage , including the zero voltage.

For this reason a network consisting of two NPN signal transistors TR1 and TR2 and some resistors has been introduced.

The transistor TR2 remains is saturation when TR1 is off, untill the output voltage of the negative regulator reaches 4.3V

At this point TR1 goes in saturation, sending off TR2. In this way the soft start is blocked and the device begins to work starting in soft start.

Switching off the mains voltage, the regulator generating the negative volatge is still in regulation when the input voltage of the switching converter has already dropped below the turn on threshold.

Carefull attention must be given therefore to calculate the input capacitor of the two sections in order to avoid possible malfunctioning during the turning on and turning off.

b) a solution that presents a cheaper costs and tha doesn't use a negative reference voltage is the following:

Setting the cursor "P" to the adjustable resistance at 0V, using R1 and R2 the maximum output voltage can be fixed.

In this case we set R1 = 24Kohm and R2 = 4K7ohm.

In R1 the maximum flowing current will be limited at 1mA; with 1mA flowing in R1, Vo = 30V.

Now by reducing the current in R1 the output voltage Vo can be adjusted till to 0V.

Figure 59: 10A Switching Regulator, Adjustable from 0V to 25V

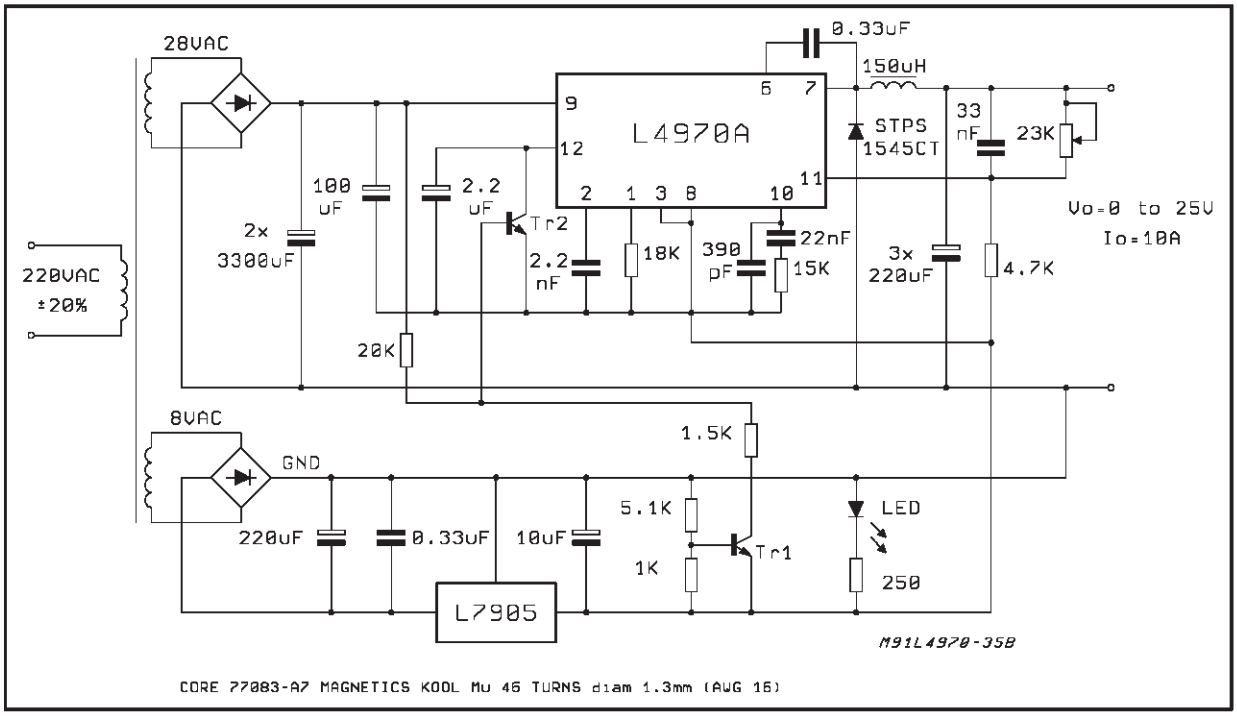
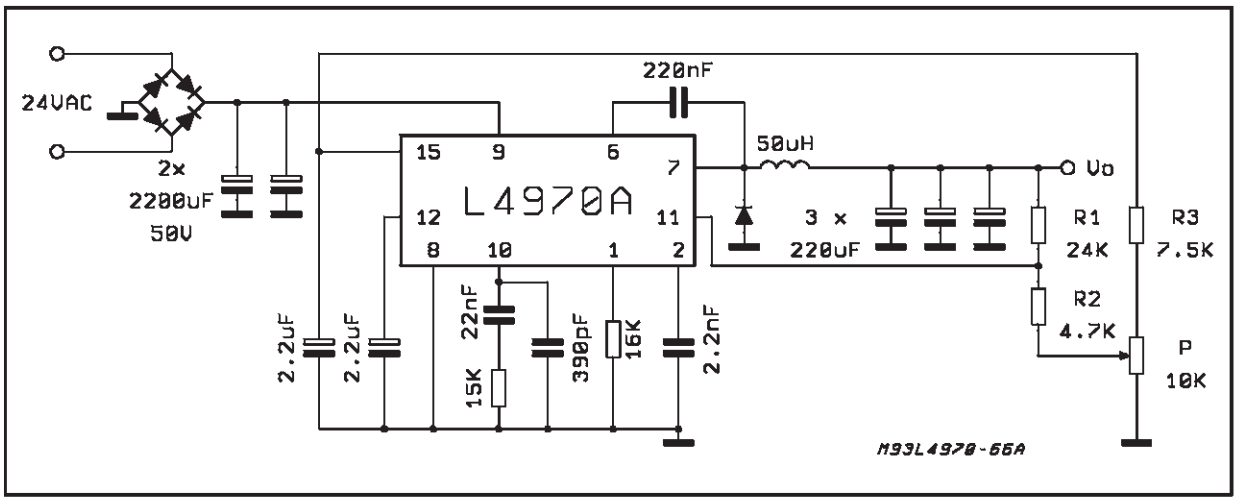


Figure 60.



The current, flowing in backward, to have 0V it will be:

$$I1 = \frac{V_{ref}}{R1} = \frac{5.1V}{24K} = 0.21mA$$

$$\Delta V_{R2} = R2 \cdot 0.21 = 4.7k \cdot 0.21 = 1V$$

Therefore, when the cursor "P" reaches Vref + 1V the output voltage goes to zero.

At this point we are able to define as well the values of P1 and R3.

When the "P" cursor is completely moved to high, there should be 6V of dropping to "P", and in this way 0.6mA will flow.

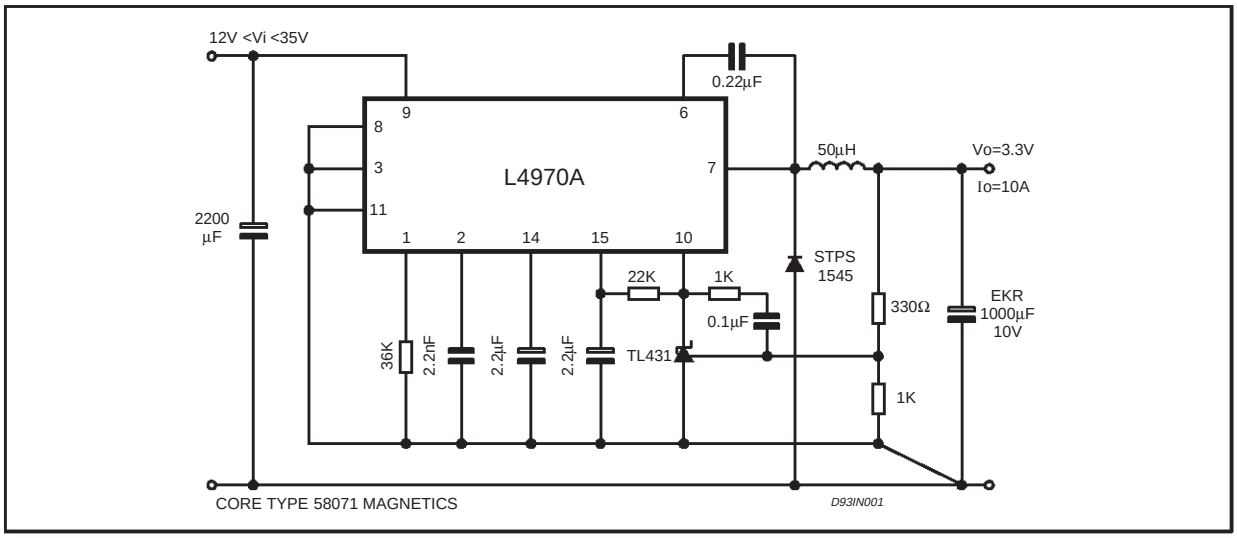
The current flowing in R3, considering that the voltage at pin 15 has a typical value of 12V, it will be of 0.8mA.

In this case the R3 value will be 7K5ohm.

3.3V / 10A DC-DC CONVERTER

When an output voltage lower to the reference voltage of 5.1V must be stabilized with a good result from stability and regulation point of view, and

Figure 61.



not having available the not-inverting input of the error amplifier, it is possible to use an external reference.

In this case a TL431C reference has been chosen, which is cheaper and widespread used.

In this case more than a simple reference, it is a true shunt regulator, containing a reference, an error amplifier and a transistor capable of absorbing a max current of 100mA.

Such component can be compensated like a common OP/AMP, and therefore in our application can substitute both the internal reference and the error amplifier.

The fig. 61 represents the electrical diagram of the application at 3.3V.

The operating input voltage is between 12V (due to the internal UVLO) and 35V, with a minimum operating switching frequency of 100KHz.

The maximum operating input voltage is limited only 35V because the minimum "ON" time, which should not be reduced below 1 microsecond.

At input voltage of 35V, output voltage of 3.3V and fs=100KHz the Ton time is already about of 1 microsecond.

Infact we have:

$$V_O = V_i \frac{T_{on}}{T} \quad \text{therefore:} \quad T_{on} = \frac{V_o}{V_i} T$$

The inductor can be calculated using the usual formula, that is:

$$L = \frac{(V_i - V_o) \cdot V_O}{V_i \cdot \Delta I_L \cdot fsw}$$

with ΔI_L = 10% I_{omax}, L = 30µH

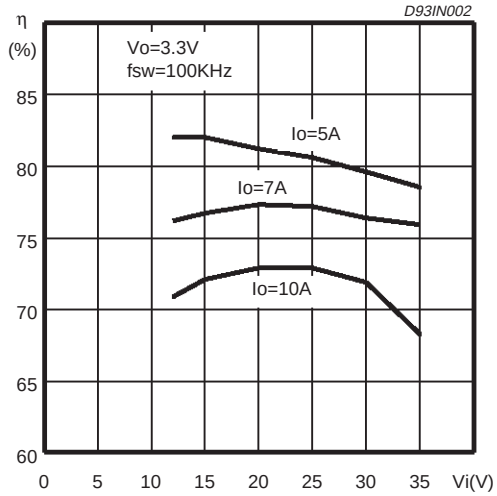
When one operates with input voltage below of 5V, it' very difficult to obtain a good efficiency. In our case having the conduction losses and switching losses of the internal power transistor fixed by both external operating electrical condition and the electrical characteristics of the itself power transistor, since integrate, it's necessary to optimize the losses of the catch diode, using new type at lower forward voltage drop, as soon as available on the market or by appropriately overdimensioning.

In some case a Power MOS used as a synchronouos switch can contribute to elevate the overall efficiency of the system.

Following are citated the principle results obtained by using our evaluation board:

The same solution, obviously can be applied also to the other types of the family, adjusting if needed the compensation network and the coil.

Figure 62: Efficiency vs. Input Voltage



Efficiency vs. Input Voltage

V_i (V)	I_o = 10A η%	I_o = 7A η%	I_o = 4A η%
12	70.9	76.2	82
15	72.1	76.7	82
20	72.9	77.3	81.2
25	72.9	77.2	80.6
30	71.9	76.4	79.6
35	68.3	75.9	78.5

Figure 63: Load Transient Response

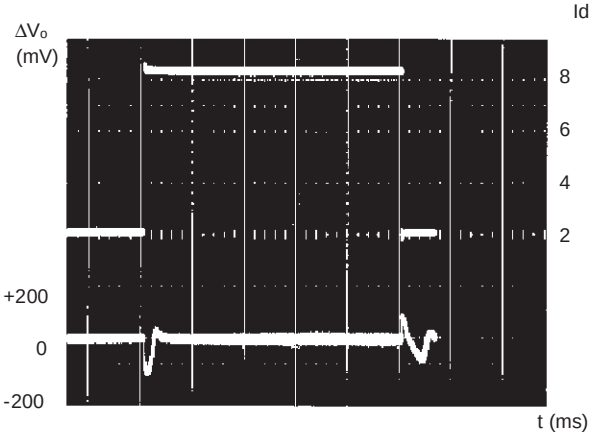
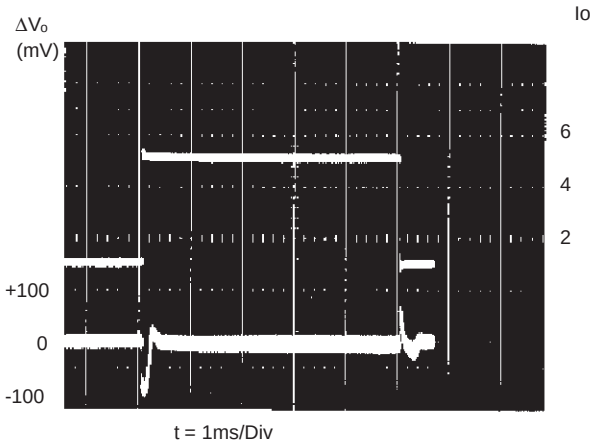


Figure 64: Load Transient Response



Output voltage ripple vs inductor value.
C_o = 1000µF/10V - EKR; ESR = 10mΩ

L	L = 30µH	L = 50µH	L = 60µH	L = 100µH
ΔV_{Omax}	80mV	60mV	40mV	25mV

CURRENT GENERATOR

Often it is required to generate constant current , fixed or adjustable, for various applications, such as chemical process, lamp powering, battery charger for lead acids, ni-cd and ni-me-hyd batteries.

Figure 65: Constant Current Generator and battery chargers.

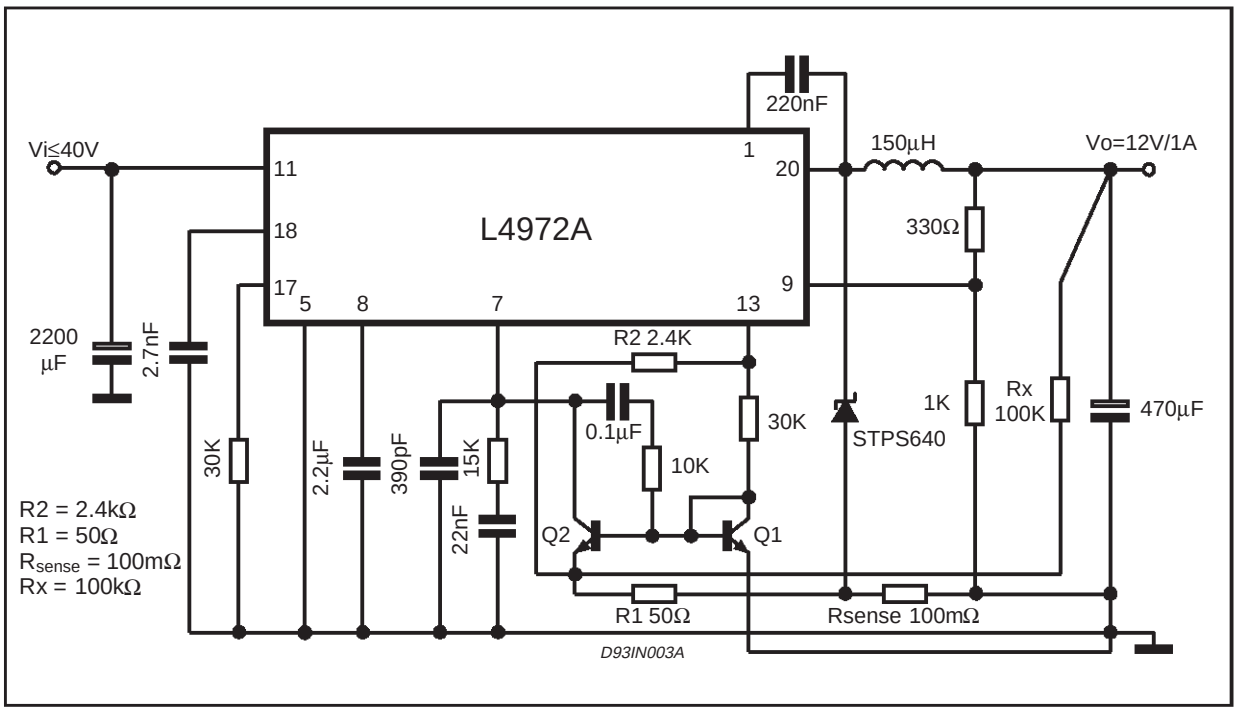
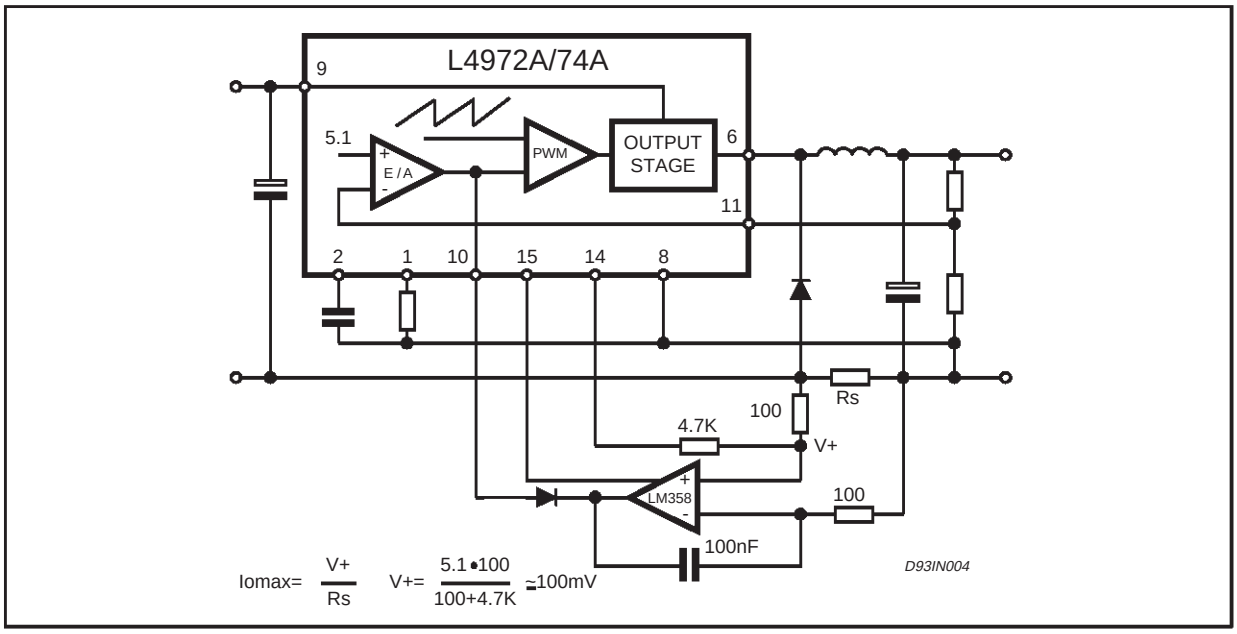


Figure 66.



In this paragraph some suggestions will be given for how to abtain generators of constant current, more or less sophisticated according to the need.

The examples given are time by time applicable to the different devices of this family of regulators, with the necessary adjustement according to the current required by the application.

The diagram of fig. 66 propose a simple solution that makes use of two esternal small signal-transistor best if matched in Vbe, and some other passive components. For a cost reduction Q1 can be substitute by a simple diode 1N4148.

The divider composed by R2 and R1 fixes a voltage at the whished voltage value (for example 50 -100mV) on the Q2 emitter.

Q2 will be reversed bias untill the emitter voltage of Q1 will raech the same value as itself.

At this point Q2 will be direct bias and will begin to absorb current from its collector; in the moment in which Q2 will enter into conduction, a variation /\Vsc at the current sense resistor will give a variation of the Q2 current equal to:

$$\Delta I_{CQ2} = \frac{\Delta V_{SC}}{R1}$$

When the current absorbed by Q2 will reach the maximum current delivered by the error amplifier output (or by the current of the soft-start if this pin is prefered to use), the error amplifier will fall out of regulation and its output voltage will begin to decrease reducing, conseguentely, the duty cycle; then the regulator will begin in this way to behave as a generator of current instead of voltage. The emitter voltage of Q2 is fixed by the following formula:

$$V_{EQ2} = \frac{V_{REF}}{R1 + R2}\ R1 = 5.1V\ \frac{R1}{R1 + R2}$$

A general criterium, is that of fixing the divider "R1R2" in such way as to make a current flow that is greater than the necessary lowering the output voltage of the error amplifier.

The maximum current delivered by the output of the transconduttance error amplifier is 200µA; the current that has to flow in the divider R1R2 should be around of 2-3mA to have a very precise intervation or around only 1mA for slightly more soft interventions.

By varying the value of R2, the point of intervention of the current limitation will be moved.

The resistor Rx contributes to introducing a more or less accentuate foldback effect, on the output current.

In the following table suggest a few values of Rsense according to the nax output current.

R_{sense} (mΩ)	I_o (A)	Device
10	10	L4970A
15	7	L4977A
30	5	L4975A
50	3.5	L4974A
100	2	L4972A

The criterium used to defined the value of the sense resistor is essentially tied to the max power dissipated by the resistance, as well as to the market availability.

If the mains objective is to maximize the efficiency

when (delivering for example 10A), it is convenient to use two current transformers instead of a dissipative resistor, one in series to the source of the internal DMOS and one in series to the catch diode.

Using such solution, a quite simple and fine regulation of the current is possible to implement.

Figure 66 shows a current generator solution with high precision on the current, using an op/amp instead of two small signal transistors.

Higher input voltage.

Since the maximum operating input voltage of this family is 50V, when one of these devices must be supplied with more elevated voltages, it is necessary to introduce a preregulator.

Fixing the output voltage of the preregulator of 45V, the power dissipation of the preregulator is:

$P_d = I_i \cdot V_{CE} \cdot = I_i \cdot (V_i - 45)$

In the buck converter, the average input current is:

$$I_i = I_o \cdot \frac{T_{on}}{T} = I_o \cdot \frac{V_o}{V_i}$$

DESIGN EXAMPLE FOR L4974A

(a)	(b)
Vo = 5.1V Io = 3.5A Po = 17.85W	Vo = 12V Io = 3.5A Po = 42W
Ii = 0.388A	Ii = 0.933A
With an operating input voltage of 60V the preregulator will dissipate:	
Pd = 5.82W	Pd =13.4W
The overall efficiency will be:	
n = 68%	n = 70%

Figure 67: Design Example for L4974A

Up Down Converter

In some applications it is required to stabilize a voltage starting from an input voltage which can be lower or higher then the output regulated voltage.

In this case a well known buck-boost topology is suggested.

The fig. 68 which shows the electrical diagram of the up-down converter, makes use of the L4974A to generate an output voltage of 12V at 3A.

For output current lower or higher than 3A other devices of this family can be used. For input voltage less than 20V the zener diode can be avoided.

Such circuit can also be used as a simple step-up. In this case there is a structure of the "asymmetrical two transistor converter" type, that in the case of a short circuit is automatically protected since the internal transistor turn-off, disconnecting the power supply.

This doesn't happen in the classical step-up converter topology, in which, during the short circuit only the power transistor is protected, but the current in the coil and the freewheeling diode is not limited.

Negative Output Voltage

Often it becomes necessary, in the multioutput power supplies, to generate negative voltages with current higher than 1A maintaining an elevated efficiency of the system.

Such outputs must have a good precision and stability and must be protected from short circuiting.

With the application circuit suggested below, one the aime is to satisfy the performance listed above, and to contributing to the simplification of

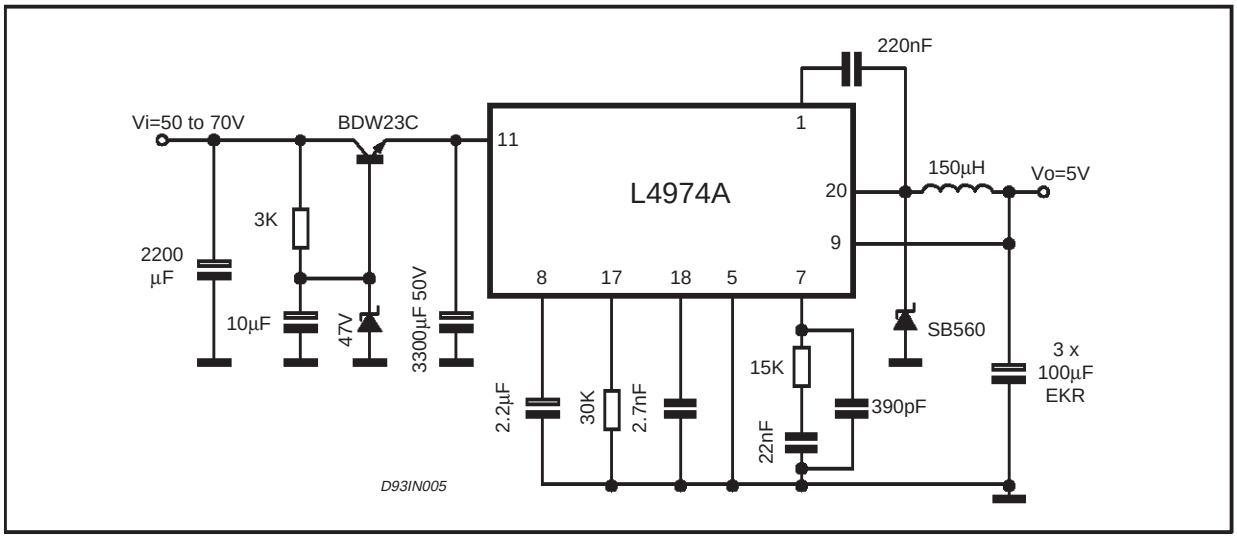


Figure 68.

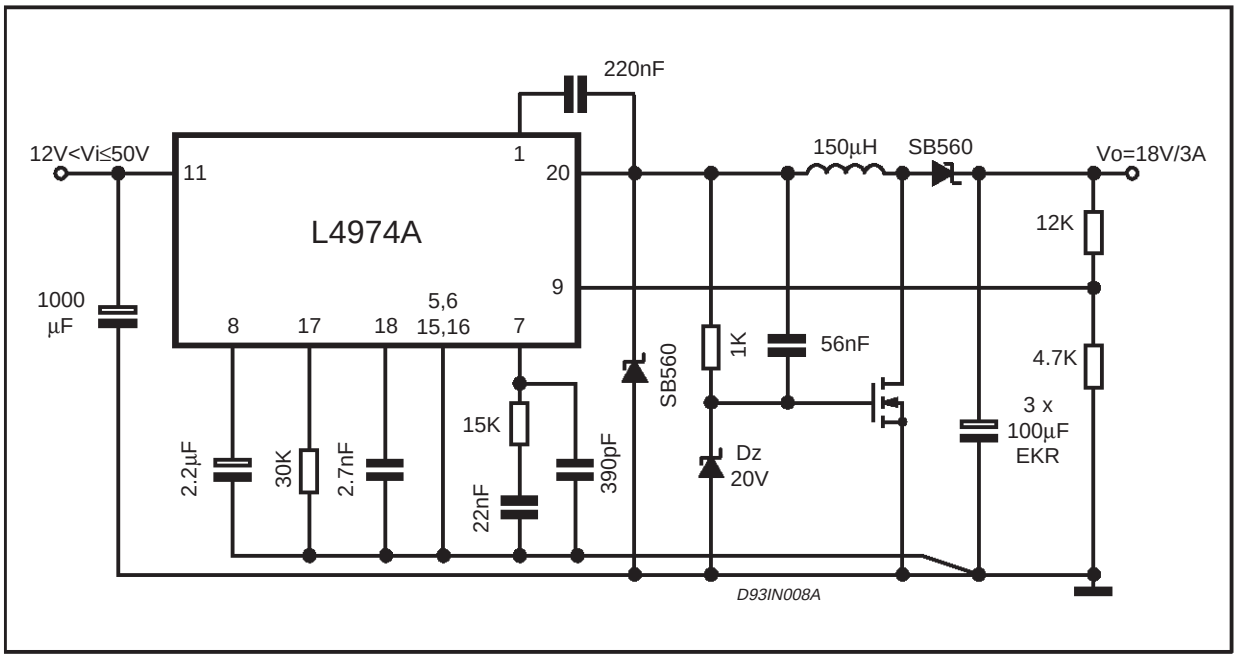
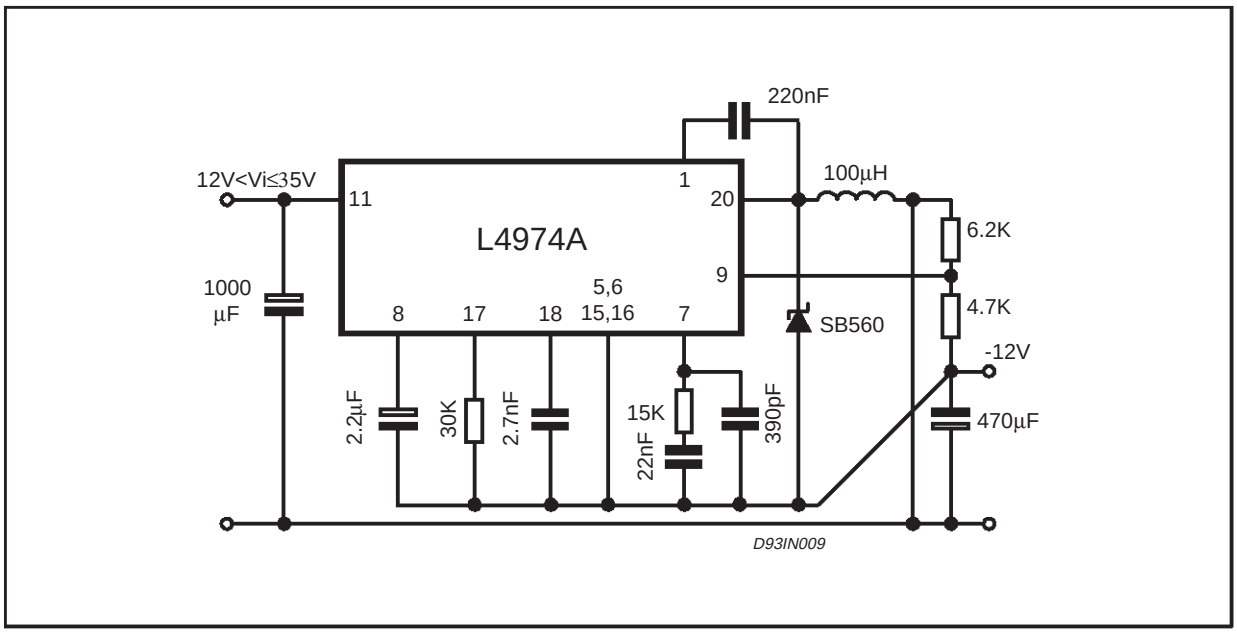


Figure 69: Circuit for negative output voltage



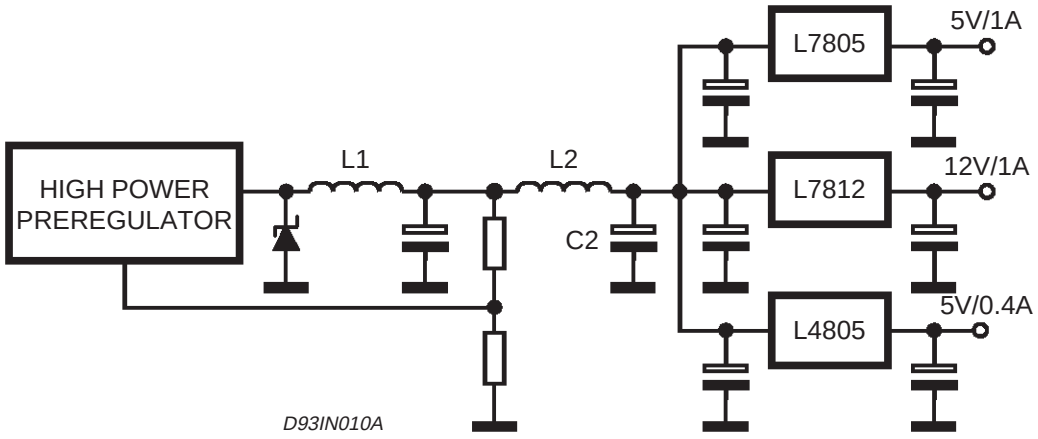
the power trasformer, both at 50Hz and at high frequency.

It's important to remember not to exceed the absolute maximum voltage ratings of the device. In this case the differential voltage applied to the device is the sum of the maximum input voltage (positive) and of that controlled output negative.

Linear low drop post regulation

In some application it becomes necessary to generate stable, precise fixed or adjustable output voltages at high efficiency and with a truly negligible output ripple. Summarizing a regulator that offers the quality of a linear type of control with the efficiency of a switching regulator. The fig. 70 shows the diagram of a swithcing preregulator at high efficiency followed by one or more series regulators of the type very "low drop", or in the case of elevated current, by a discret low drop solution.

Figure 70.



L2 and C2 are necessary to reduce the switching frequency spikes

LAYOUT CONSIDERATIONS

Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path lenght becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to output pin, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig 71 shows the structure of a power device. As demonstrated in thermo-dynamics, a thermal circuit can be considered to be an electrical circuit where R_1, R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 72).

C1, C2	are the thermal capacitance (expressed in °C/W).
I	is the dissipated power.
V	is the temperature difference with respect to the reference (ground).
This circuit can be simplified as shown in fig. 74, where:	
C_C	is the thermal capacitance of the die plus that of the tab.
C_h	is the thermal capacitance of the heatsink
R_{jc}	is the junction case thermal resistance
R_{th}	is the heatsink thermal resistance

Figure 71.

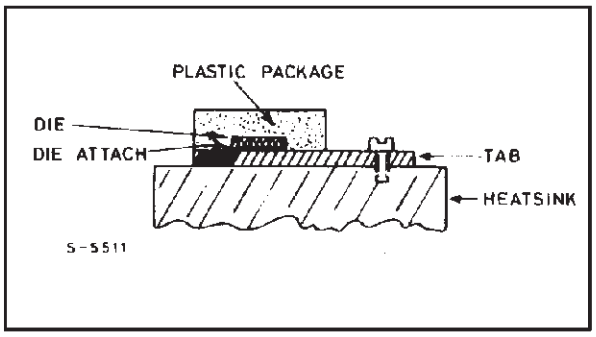


Figure 72.

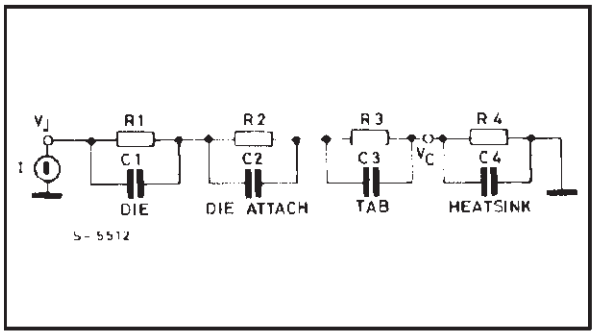
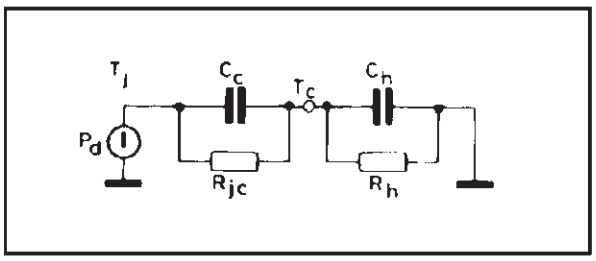
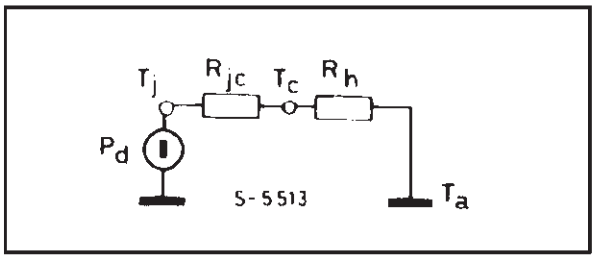


Figure 73.



But since the aim of this section is not that of studing the transistors, the circuit can be further reduced as shown in figure 74.

Figure 74.



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_{th})\, P_d \qquad a)$$

$$R_{th} = \frac{T_j - T_a - R_{jc}\, P_d}{P_d} \qquad b)$$

$$T_C = T_a + R_{th}\, Pd \qquad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5°C/W;; with silicone grease roughly 0.3°C/W and with silicone grease plus a mica insulator about 0.4°C/W. See fig. 75. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperature can be calculated by solving the circuit shown in fig. 75. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig.77 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 77 refers to specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Figure 75.

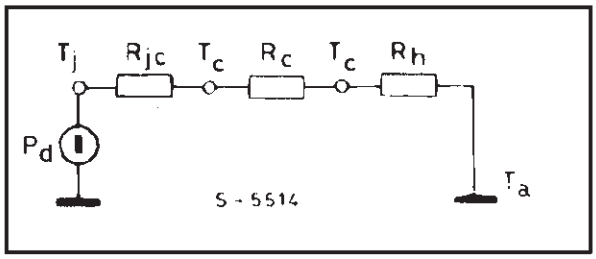


Figure 76.

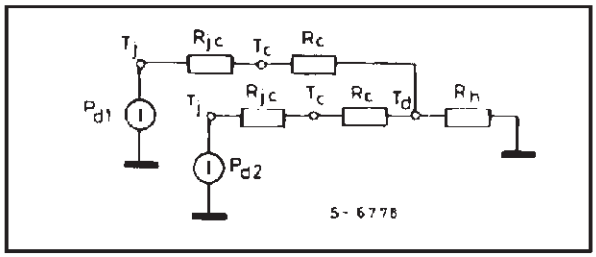


Figure 77.

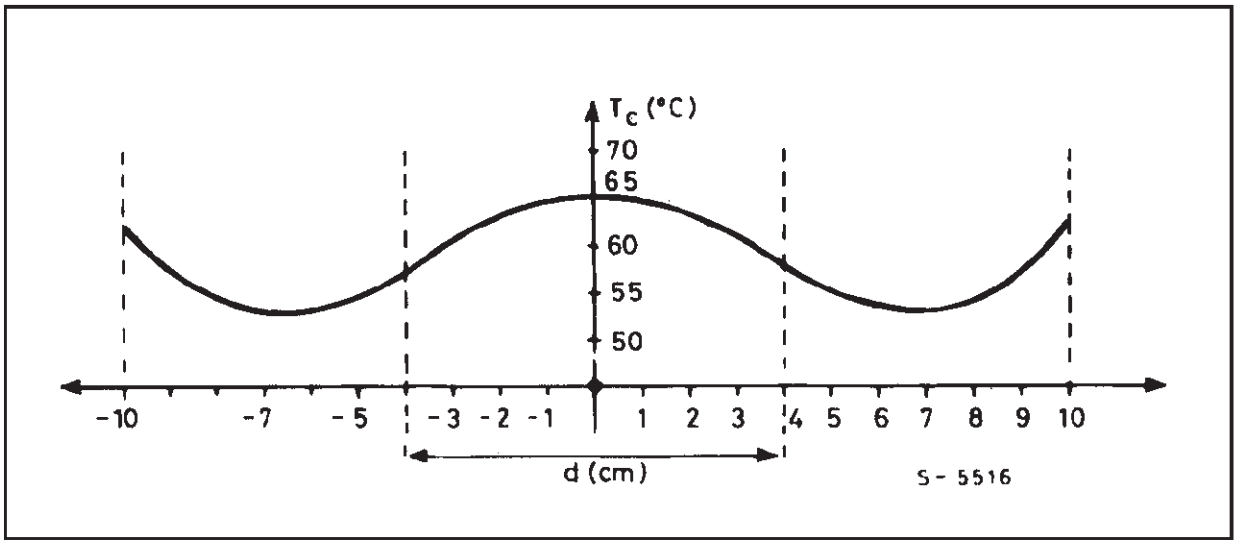


Figure 78.

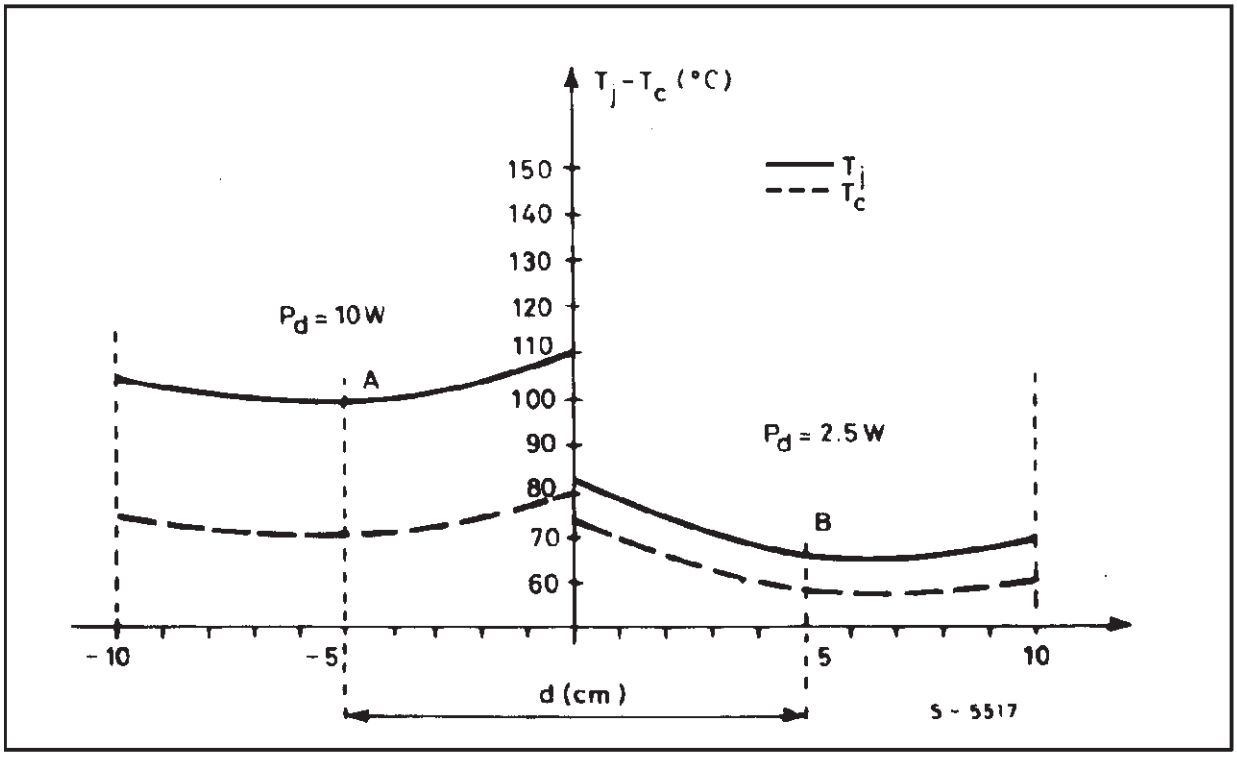


Fig. 78 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in applications with two devices in MTW package are synchronized.

REFERENCES:

1) ***AN244*** *"Designing with the L296 monolithic power switching regulator" (Ref. Designer' Guide to Power Products Application Manual).*

2) ***Table1*** *(see page 31-32/46) – EKR & EKE Roederstein Low Voltage Electrolytic Capacitors.*