



2N70-M

Preliminary

Power MOSFET

2 Amps, 700 Volts N-CHANNEL POWER MOSFET

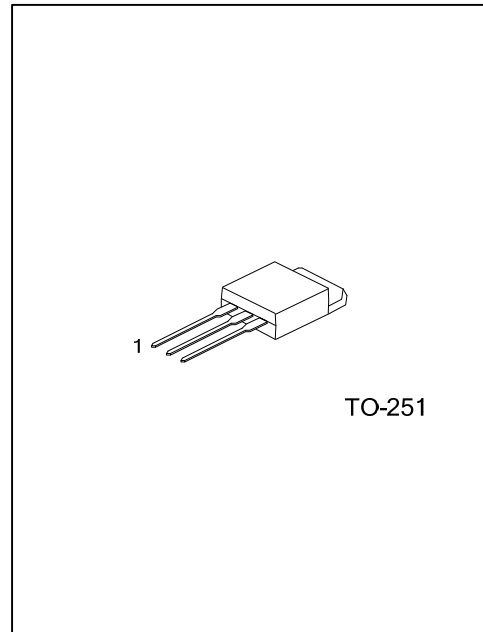
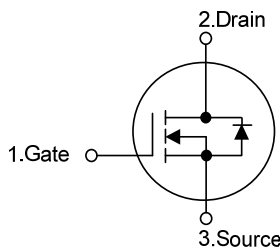
■ DESCRIPTION

The UTC **2N70-M** is a high voltage MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

■ FEATURES

- * $R_{DS(ON)} < 6.3\Omega @ V_{GS} = 10V$
- * Ultra Low gate charge (typical 17.2nC)
- * Low reverse transfer capacitance ($C_{RSS} =$ typical 5.0 pF)
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N70L-TM3-T	2N70G-TM3-T	TO-251	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2N70L-TM3-T</p>	<p>(1) T: Tube</p> <p>(2) TM3: TO-251</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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■ MARKING INFORMATION

PACKAGE	MARKING
TO-251	

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	700	V
Gate-Source Voltage	V_{GSS}	± 30	V
Avalanche Current (Note 2)	I_{AR}	2.0	A
Drain Current	Continuous	I_D	2.0
	Pulsed (Note 2)	I_{DM}	8.0
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	140
	Repetitive (Note 2)	E_{AR}	2.8
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation	P_D	30	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Temperature	T_{OPR}	-55 ~ +150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by T_J

3. $L=64\text{mH}$, $I_{AS}=2\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 2.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.24	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	700			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 700V, V_{GS} = 0V$			10	μA
		$V_{DS} = 560V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			100	μA
Gate-Source Leakage Current	Forward	I_{GSS}				nA
	Reverse					
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D = 250\mu A$, Referenced to 25°C		0.4		$^\circ\text{V}/^\circ\text{C}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 1A$		5.4	6.3	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS} = 25V, V_{GS} = 0V, f = 1\text{MHz}$		270	350	pF
Output Capacitance	C_{OSS}			38	50	pF
Reverse Transfer Capacitance	C_{RSS}			5	7	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 30V, I_D = 0.5A, R_G = 25\Omega$ (Note 1, 2)		35	40	ns
Turn-On Rise Time	t_R			65	70	ns
Turn-Off Delay Time	$t_{D(OFF)}$			105	115	ns
Turn-Off Fall Time	t_F			50	70	ns
Total Gate Charge	Q_G	$V_{DS} = 560V, V_{GS} = 10V, I_D = 2.0A$ (Note 1, 2)		17.2		nC
Gate-Source Charge	Q_{GS}			1.7		nC
Gate-Drain Charge	Q_{GD}			4.4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_{SD} = 2.0A$			1.4	V
Continuous Drain-Source Current	I_{SD}				2.0	A
Pulsed Drain-Source Current	I_{SM}				8.0	A
Reverse Recovery Time	t_{RR}	$V_{GS} = 0V, I_{SD} = 2.0A$		260		ns
Reverse Recovery Charge	Q_{RR}	$di/dt = 100A/\mu s$ (Note1)		1.09		μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

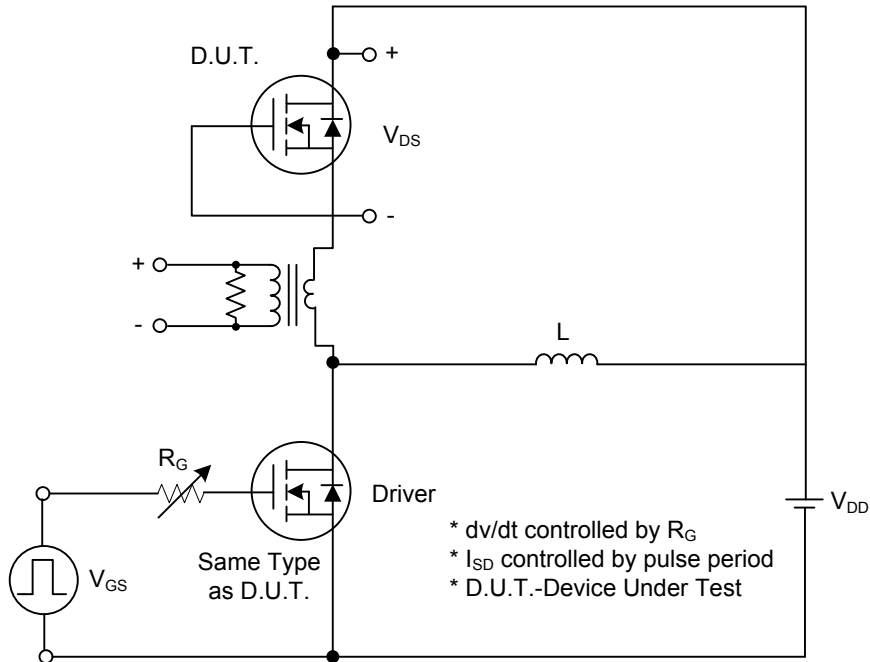


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

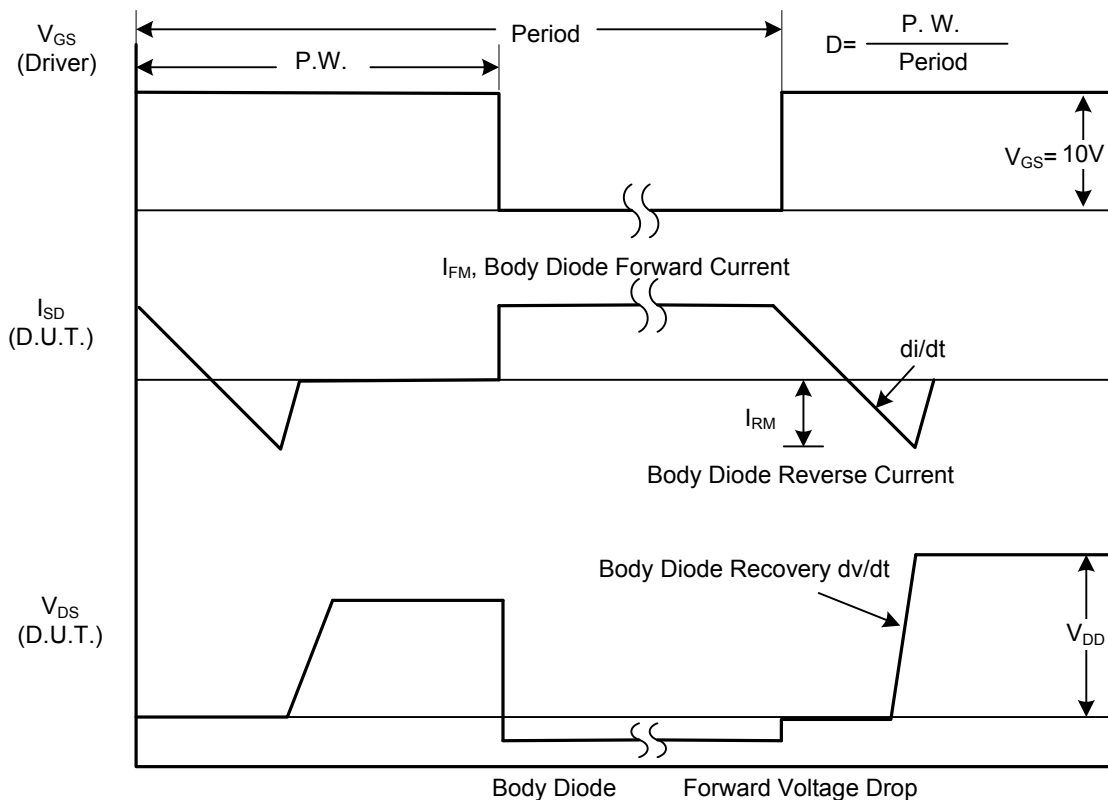


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

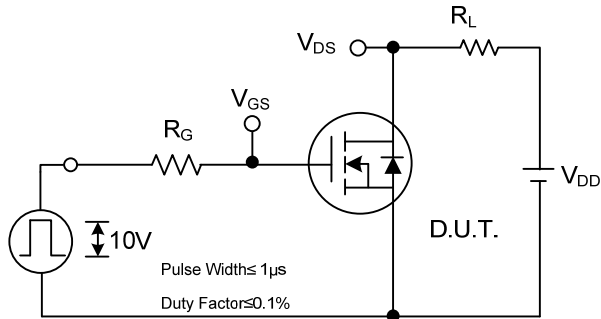


Fig. 2A Switching Test Circuit

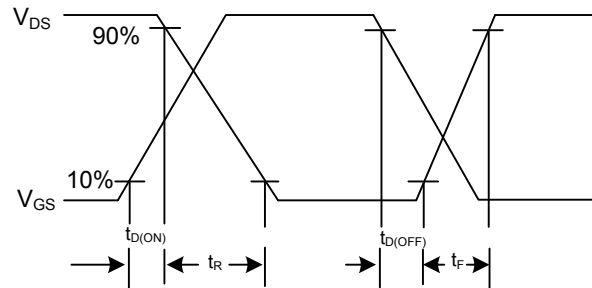


Fig. 2B Switching Waveforms

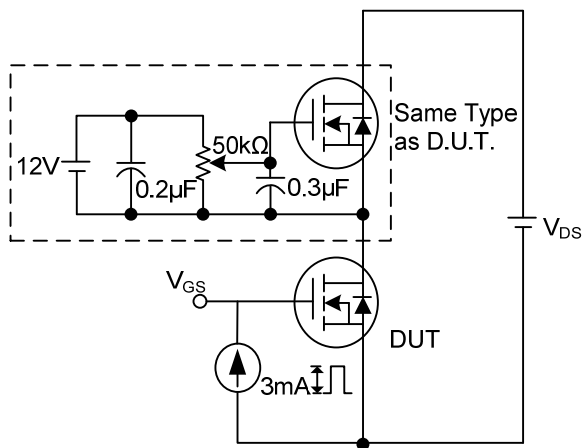


Fig. 3A Gate Charge Test Circuit

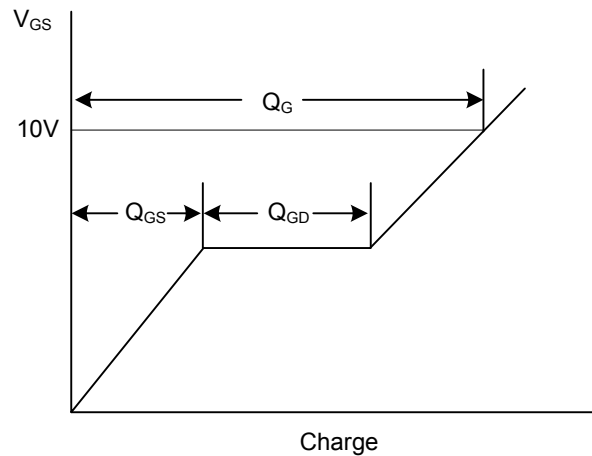


Fig. 3B Gate Charge Waveform

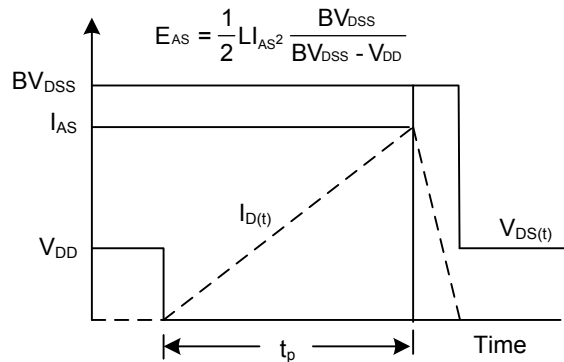
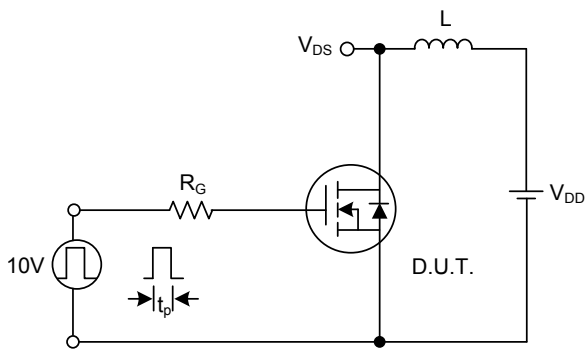


Fig. 4A Unclamped Inductive Switching Test Circuit Fig. 4B Unclamped Inductive Switching Waveforms

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