SCG4540 Synchronous Clock Generators

PLL

CONNOR WINFIELD

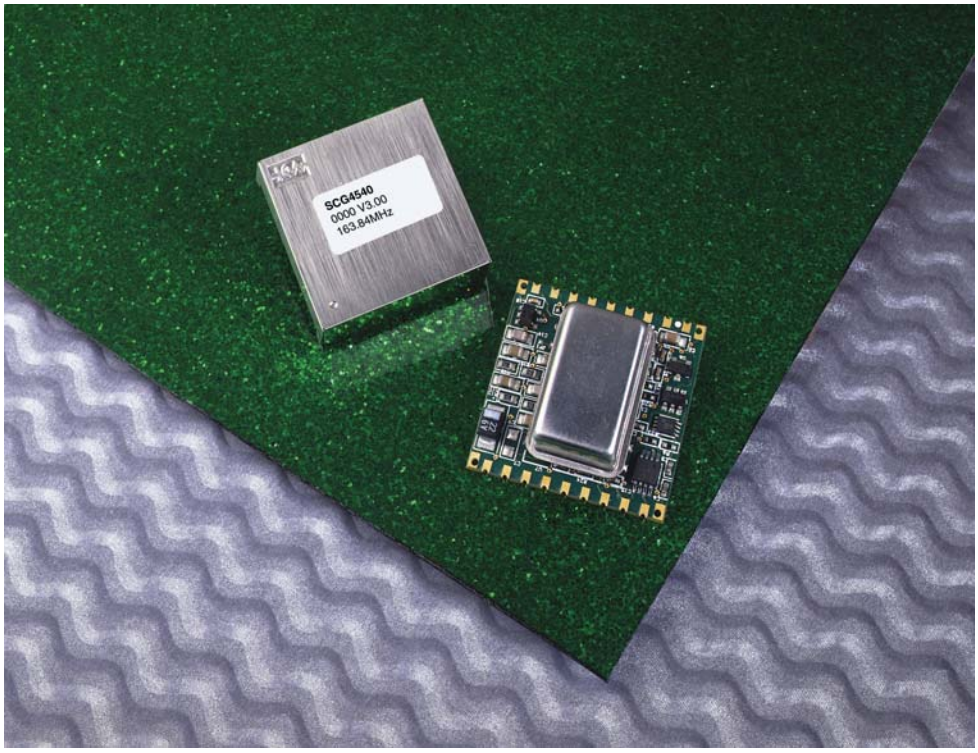
2111 Comprehensive Drive

Aurora, Illinois 60505

Phone: 630-851-4722

Fax: 630-851-5040

www.conwin.com



Features

- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- LVPECL Outputs with Disable Function
- Dual 10 kHz Input References
- LOR & LOL combined alarm output
- Force Free Run Function
- Automatic Free Run operation on loss of both References A & B
- Input Duty Cycle Tolerant
- 3.3V dc Power Supply
- Small Size: 1 Square Inch

Bulletin	**SG053**
Page	**1 of 16**
Revision	**P01**
Date	**5 AUG 02**
Issued By	**MBatts**

General Description

The SCG4540 is a mixed-signal phase locked loop generating LVPECL outputs from an intrinsically low jitter, voltage controlled, crystal oscillator. The LVPECL outputs may be disabled.

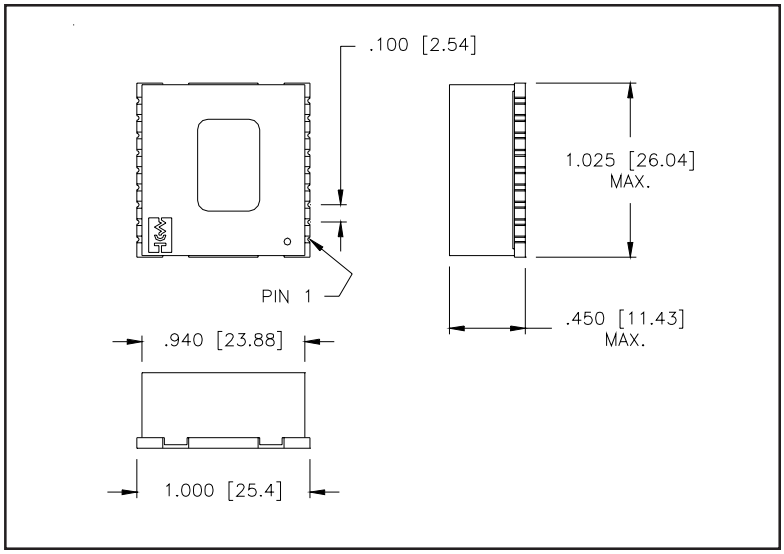
The SCG4540 can lock to one of two 10 kHz, external references, which is selectable using the SEL_{AB} input select pin. The unit has a fast acquisition time of about 1 second and it is tolerant of different reference duty cycles.

The SCG4540 includes an alarm output that indicates deviations from normal operation. If a Loss-of-Reference (LOR) or Loss-of-Lock (LOL) is detected the alarm with indicate the need for a reference rearrangement. If both references A and B are absent the module will enter Free Run operation. The FR_{status} pin will indicate that the module is in Free Run operation. Frequency stability during Free Run operation is guaranteed to ±20 ppm. Additionally the Free Run mode may be entered manually.

The package dimensions are 1" x 1.025" x .45" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloys, 180°C surface mount reflow processes.

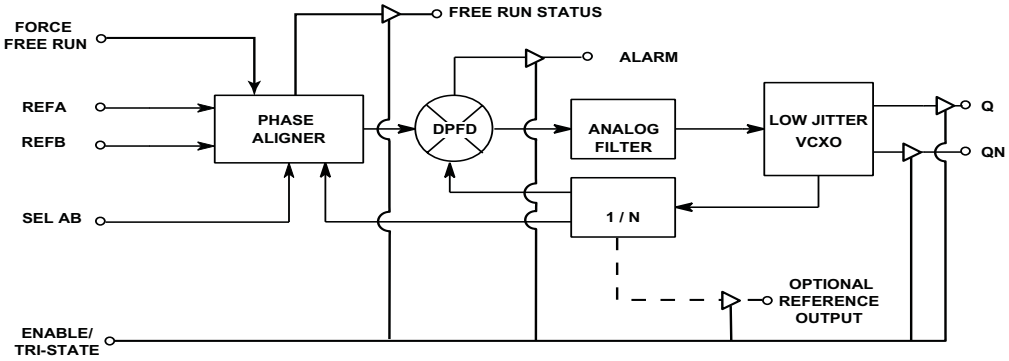
Maximum Dimension Package Outline

Figure 1



Block Diagram

Figure 2



Model Comparison Table

Table 1

Model	Dual Input Ref Freq	Max Duty Cycle	LVPECL Oscillator Output (Pins 16 & 18)	Notes
SCG4500	8 kHz/8 kHz	40/60	77.76 MHz,155.52 MHz,125 MHz	Basic Model
SCG4510	**1.544 MHz/1.544 MHz**	40/60	155.52 MHz	
SCG4520	**19.44 MHz/19.44 MHz**	40/60	77.76 MHz,155.52 MHz	
SCG4540	**10 kHz/10 kHz**	40/60	**163.84 MHz**	

*Features which differentiate a model from the base model (SCG4500) are highlighted in boldface color and in the notes column.

Absolute Maximum Rating

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_i	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+100	°C	1.0

Input and Output Frequencies

Table 3

Parameter	Frequency
Input Reference Frequency	Dual 10 kHz
Available Output Frequencies	163.84 MHz
Optional Reference Output Frequencies	Not Available

Operating Specifications

Table 4

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.135	3.3	3.465	Volts	2.0
I_{cc}	Power Supply Current	170	230	280	mA	5.0
T_o	Temperature Range	0	-	70	°C	
F_{fr}	Free Run Frequency	-20	-	20	ppm	
F_{cap}	Capture/pull-in range	-25	-	25	ppm	
F_{bw}	Jitter Filter Bandwidth	-	-	10	Hz	3.0
T_{jtol}	Input Jitter Tolerance *(Input Jitter Frequencies ≥ 10 Hz)*	1	-	-	µs	
T_{aq}	Acquisition Time	-	1	-	s	4.0
T_{rf}	Output Rise and Fall Time (20% 80%)	100	225	350	ps	5.0
DC	Output Duty Cycle	40	50	60	%	
$MTIE_{sr}$	MTIE at Synchronization Rearrangement		GR-253-CORE.1999 R5-136			6.0, 7.0

Output Jitter Specifications

Table 5

	Jitter BW 10 Hz - 1 MHz		SONET Jitter BW 12 kHz - 20 MHz	
Frequency (MHz)	pS (RMS)	m UI	pS (RMS)	m UI
163.84	10 Typ.	1.638 Typ.	1 Max.	0.164 Max.

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires external regulation and supply decoupling. (22 uF, 330 pF)

3.0 3db loop response.

4.0 From a 20 PPM step in reference frequency at 25°C @ 3.3V

5.0 50-ohm load biased to 1.3 volts.

6.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.

7.0 If the selected reference is removed system response to the ALARM must be less than 100ns.

Input And Output Characteristics

Table 6

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
CMOS Input and Output Characteristics						
V_{ih}	High Level Input Voltage	2.0	-	5.5	V	
V_{il}	Low Level Input Voltage	0.0	-	0.8	V	
T_{io}	I/O to Output Valid	-	-	10	ns	
C_l	Output Capacitance	-	-	10	pF	
V_{oh}	High Level Output Voltage	2.4	-	-	V	
V_{ol}	Low Level Output Voltage	-	-	0.4	V	
T_{ir}	Input Reference Pulse Width	12.5	-	-	ns	
PECL Output Characteristics						
V_{oh}	High Level PECL Voltage	2.27	2.34	2.52	V	
V_{ol}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_l	Output Capacitance	-	-	10	pF	
T_{skew}	Differential Output Skew	-	50	-	ps	

Input Selection / Output Response

Table 7

INPUTS						OUTPUTS				NOTE
RESET	**ENABLE**	**SEL_{AB}**	**REF_A**	**REF_B**	**FR**	**FR_{status}**	**ALARM**	**Q**	**QN**	
1	0	X	X	X	X	1	X	X	X	FR
X	1	X	X	X	X	X	X	0	1	
0	0	X	X	X	1	1	X	X	X	FR
0	0	0	A	A	0	0	0	X	X	RA
0	0	1	A	A	0	0	0	X	X	RB
0	0	0	NA	A	0	0	1	X	X	U
0	0	1	NA	A	0	0	0	X	X	RB
0	0	1	A	NA	0	0	1	X	X	U
0	0	0	A	NA	0	0	0	X	X	RA
0	0	X	NA	NA	0	1	1	X	X	FR

NOTES:

A Active
FR Free Run Mode
NA Not Active
RA Locked to Reference A
RB Locked to Reference B
U Unstable (due to conditions shown, switch to active reference or Free Run)
X Don't care

Pin Description

Table 8

Pin #	Pin Name	Pin Information	Note
1	ENABLE/TRI-STATE	VCXO Enable. (Enable = 0, Disable = 1 = CMOS Outputs Tri-stated)	9.0
2	TCK	No Connection, Internal Factory Programming Input.	8.0
3	TDO	No Connection, Internal Factory Programming Input.	8.0
4	REF_A	10 kHz, TTL/CMOS Reference Frequency Input.	
5	SEL_{AB}	Input Reference Select Pin. (REFA = 0, REFB = 1)	9.0
6	RESET	RESET. (RESET = 1)	9.0
7	REF_B	10 kHz, TTL/ CMOS Reference Frequency Input.	
8	V_{ee}	Ground.	
9	FR_{status}	Free Run Status. (FR = 1)	
10	V_{cc}	Supply Voltage relative to ground.	
11	N/C	No Connection. (Optional Reference Output Available)	8.0, 8.1
12	ALARM	Loss of Reference / Lock alarm. (Alarm = 1)	
13	FR	Force Free Run. (Phase Lock = 0, Free Run = 1)	9.0
14	TDI	No Connection, Internal Factory Programming Input.	8.0
15	TMS	No Connection, Internal Factory Programming Input.	8.0
16	QN	LVPECL Complementary Output.	
17	V_{ee}	Ground.	
18	Q	LVPECL Output.	

NOTES

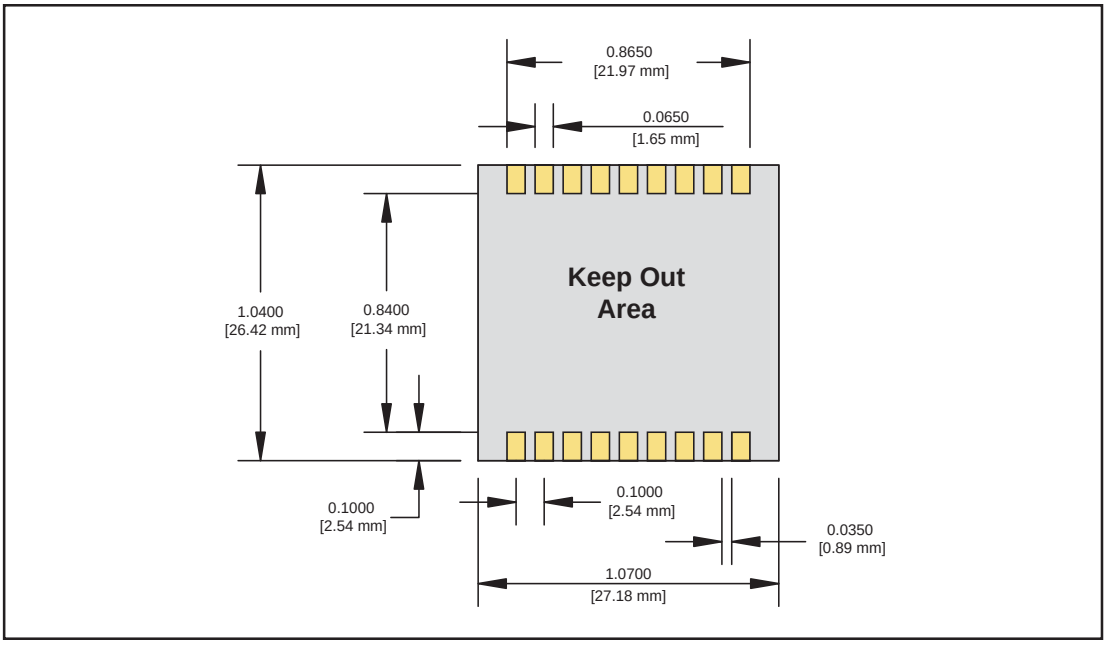
8.0 Do not connect pin

8.1 Contact a Sales Representative for availibilty and use of optional reference output

9.0 Input pulled to ground

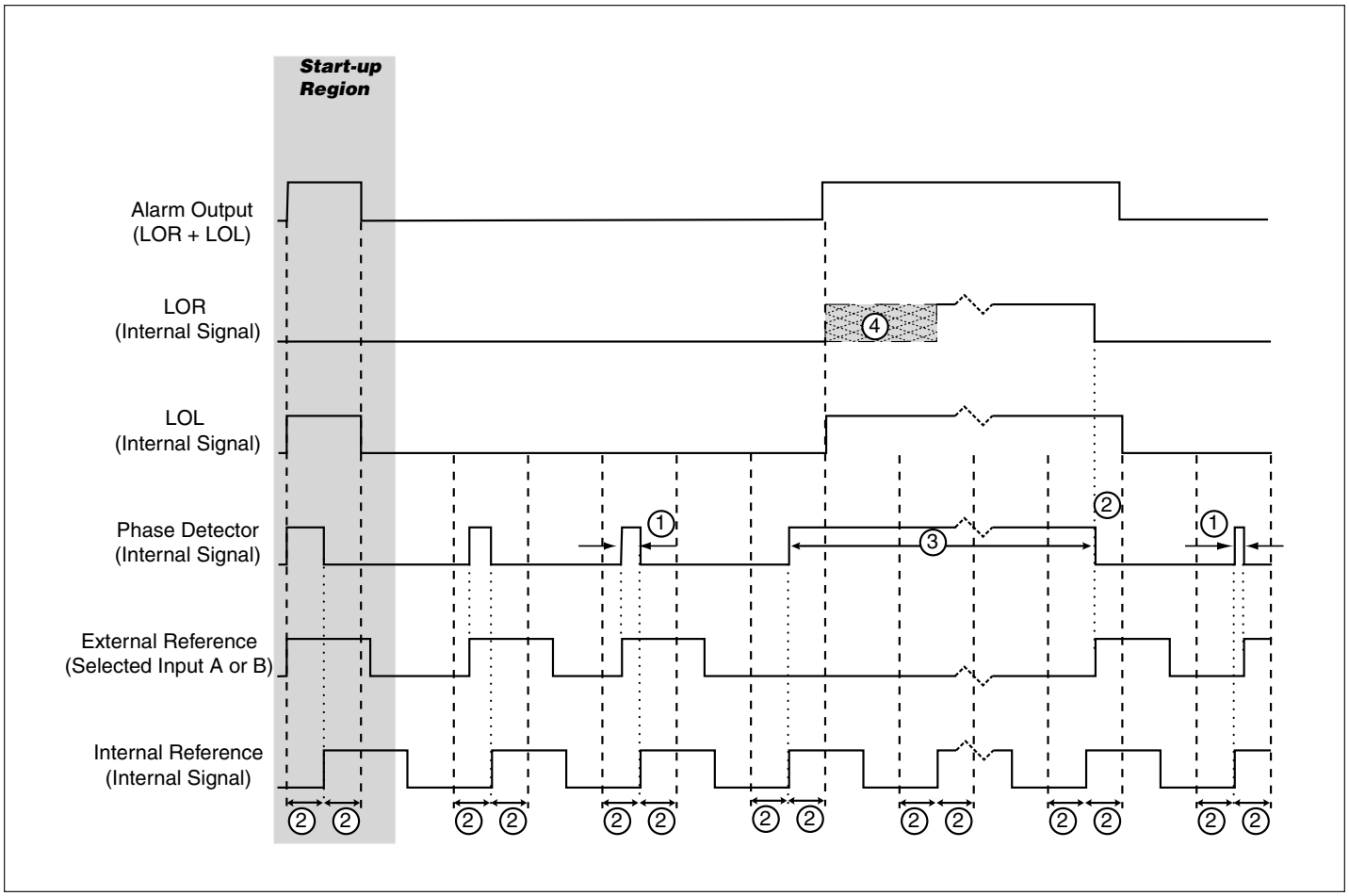
Circuit Board Footprint & Keepout Recommendations

Figure 3



Loss of Reference Condition Alarm Timing

Figure 4



AlarmTiming Legend

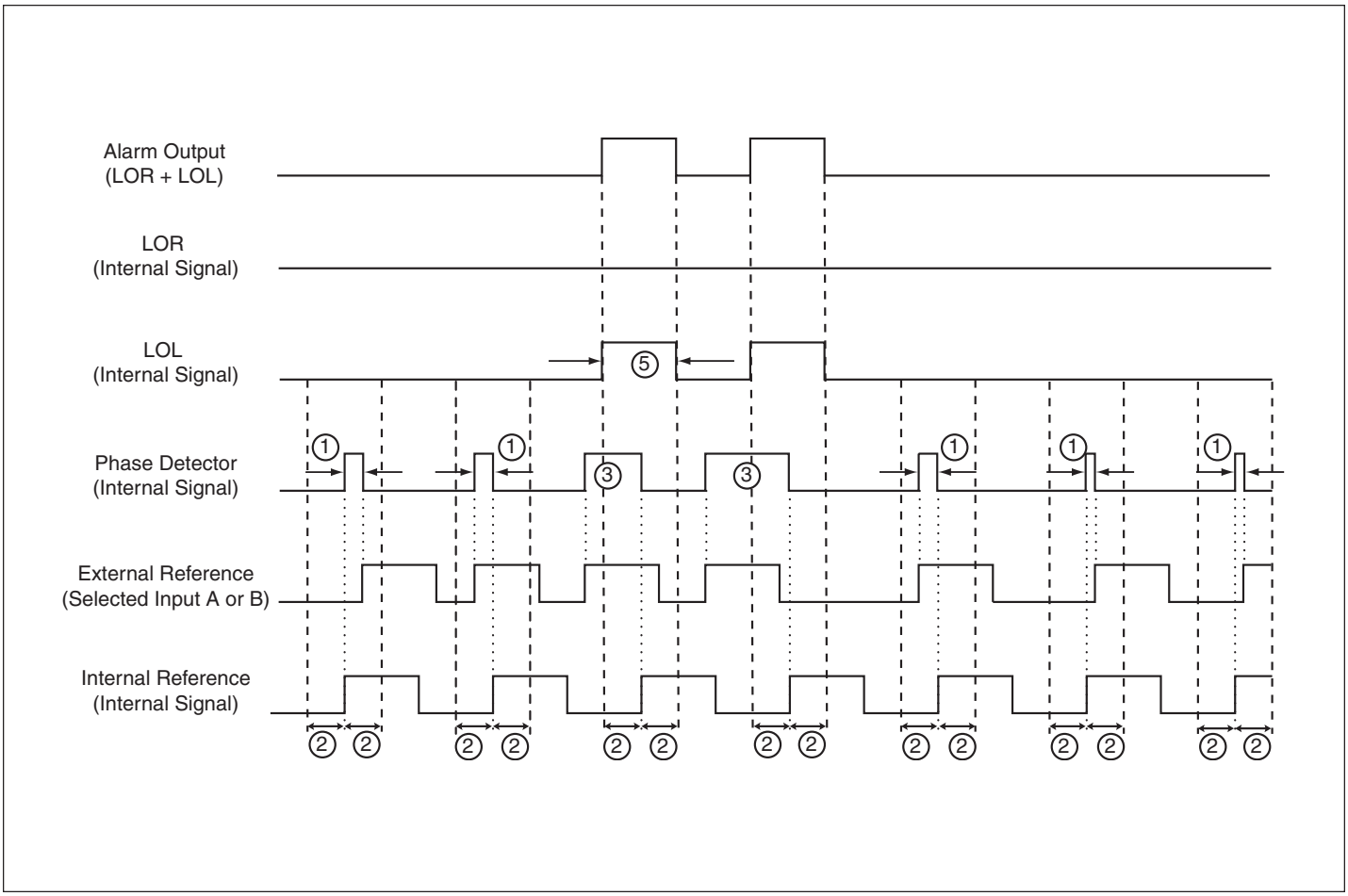
Use for all alarm timing diagrams

Table 9

	10 kHz Reference Input
1	< 1 µsec
2	1 µsec
3	> 1 µsec
4	124 µsec(min) to 374 µsec(max) after LOL
5	Minimum pulse width = 2 µs
Start-up Region	During Start-up, The LOL Alarm will pulse during the few seconds of operation

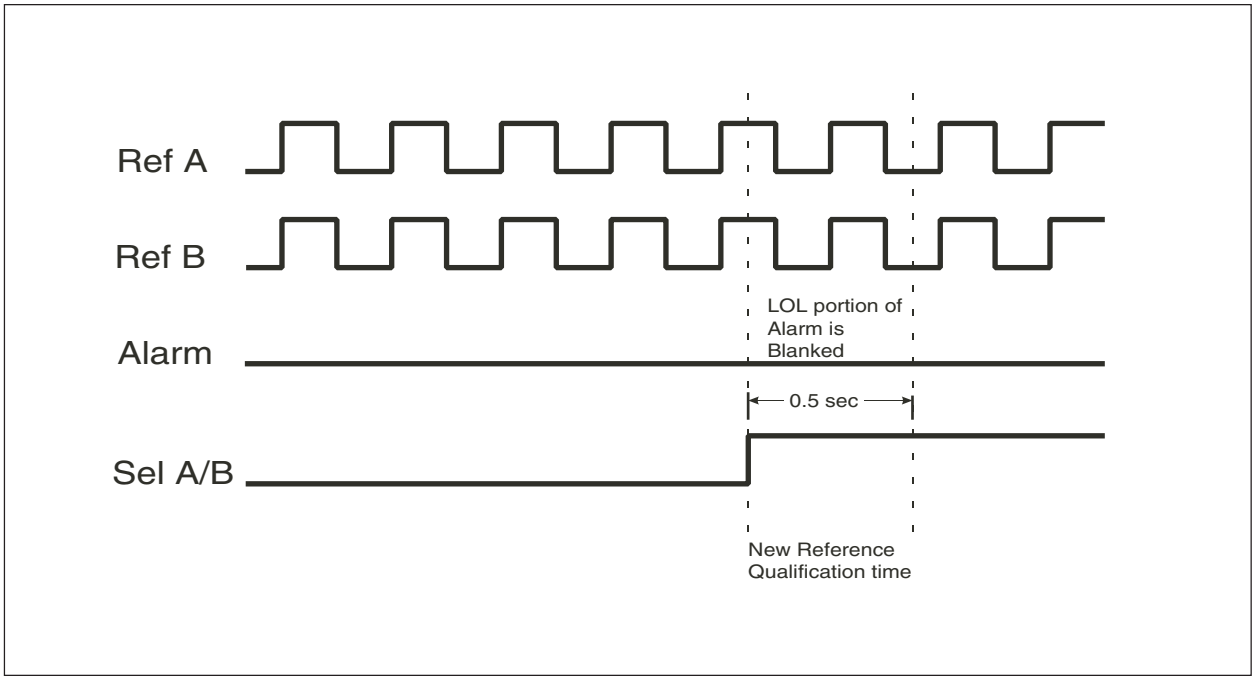
Loss of Lock Condition Alarm Timing

Figure 5



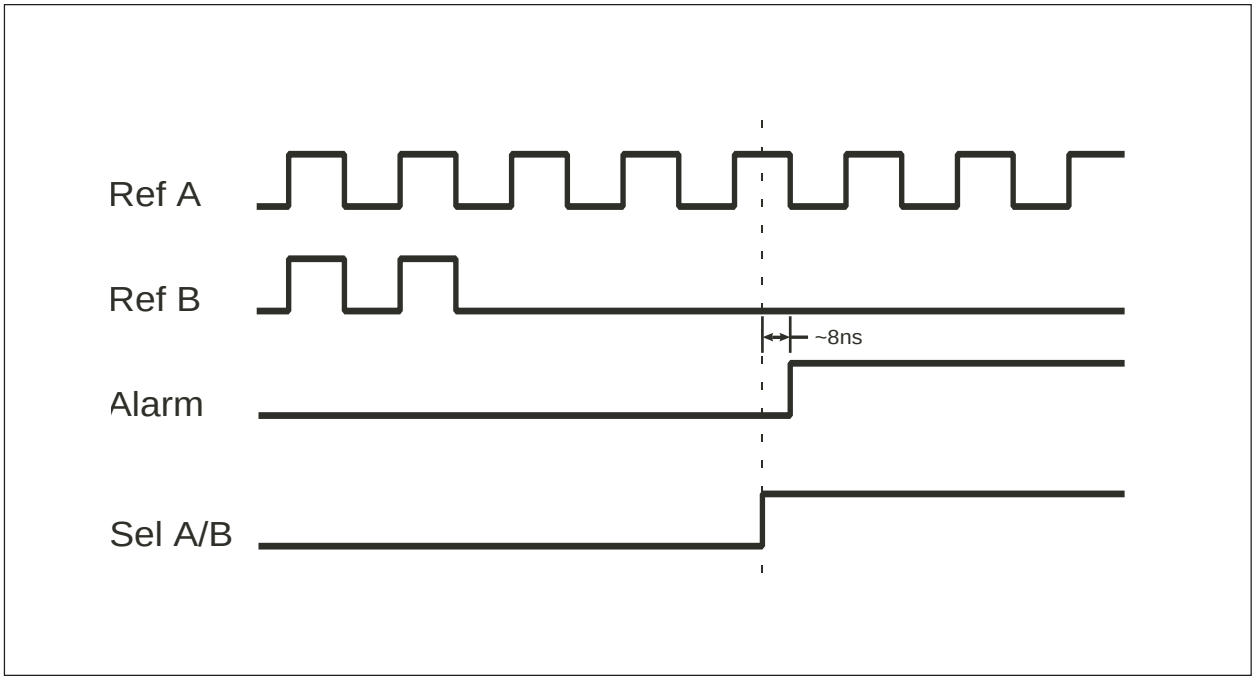
Switch from A to B when both are good signals

Figure 6



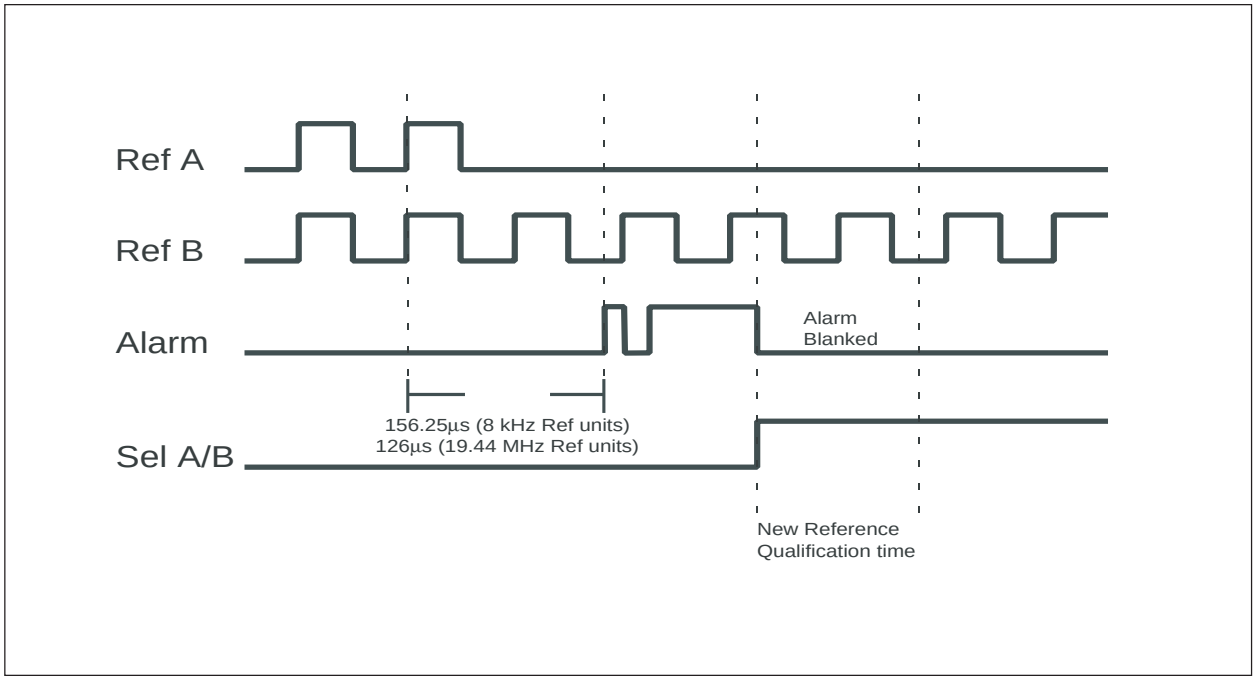
Switch from A to B when Reference B is lost

Figure 7



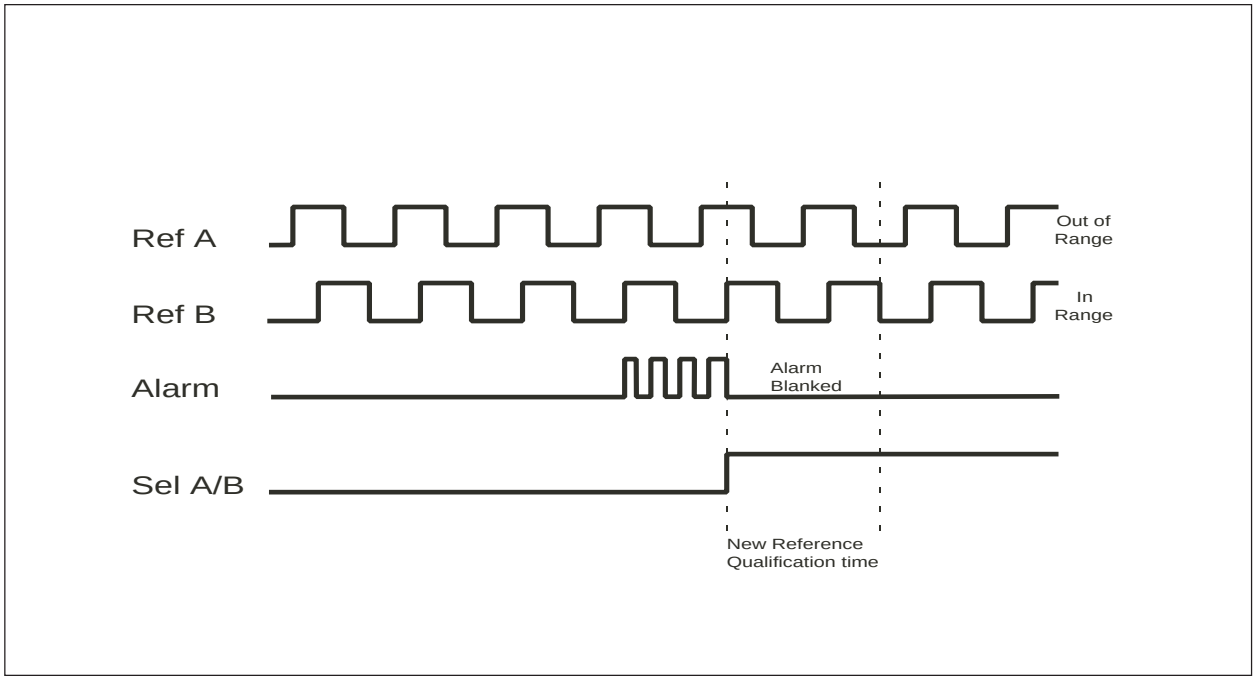
Switch from A to B after Reference A is lost

Figure 8



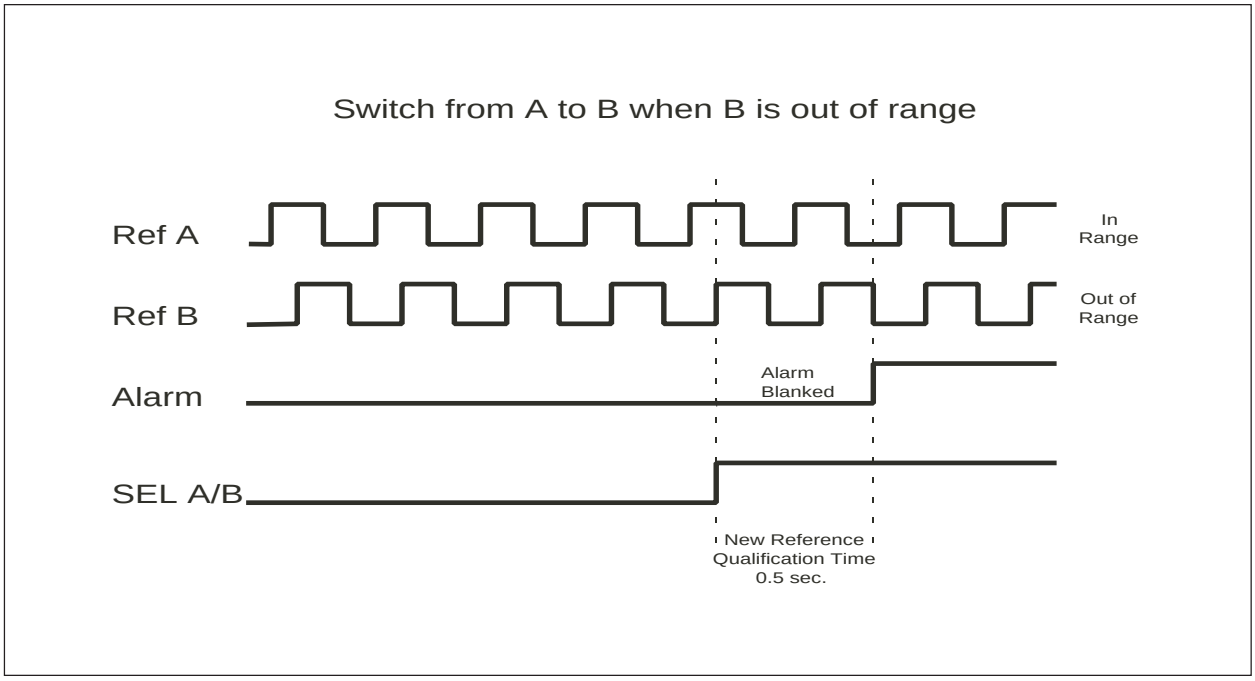
Switch from A to B when A is out of range

Figure 9



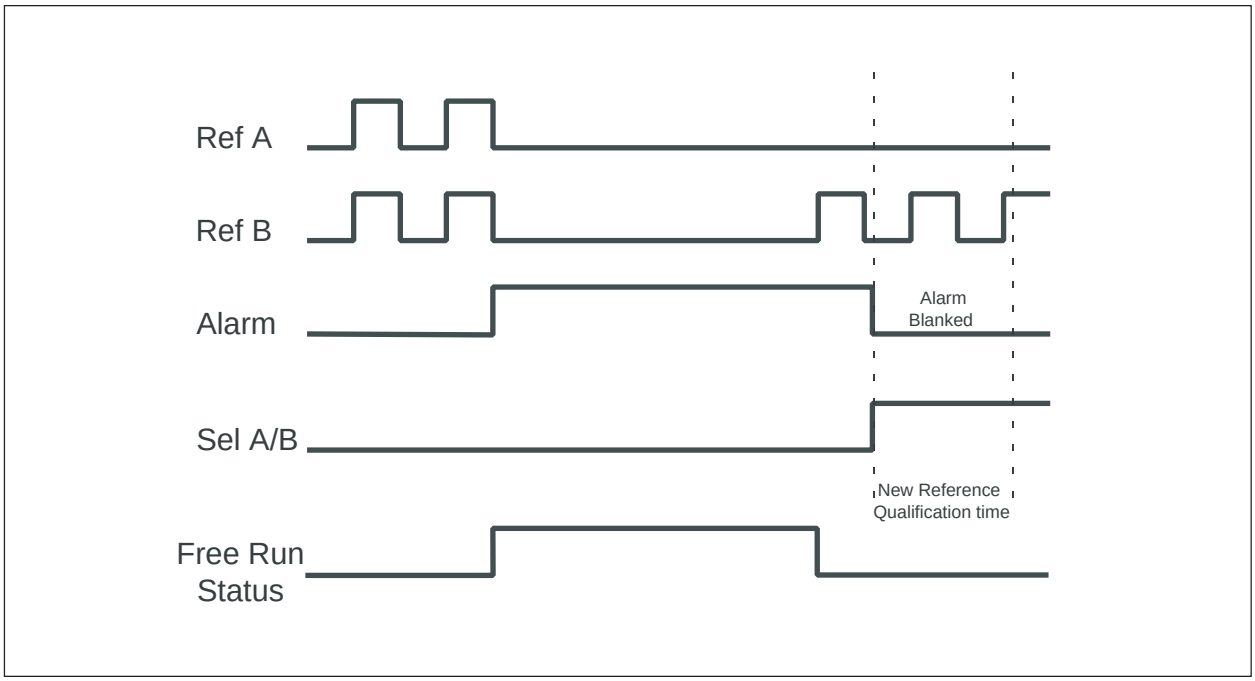
Switch from A to B when B is out of range

Figure 10



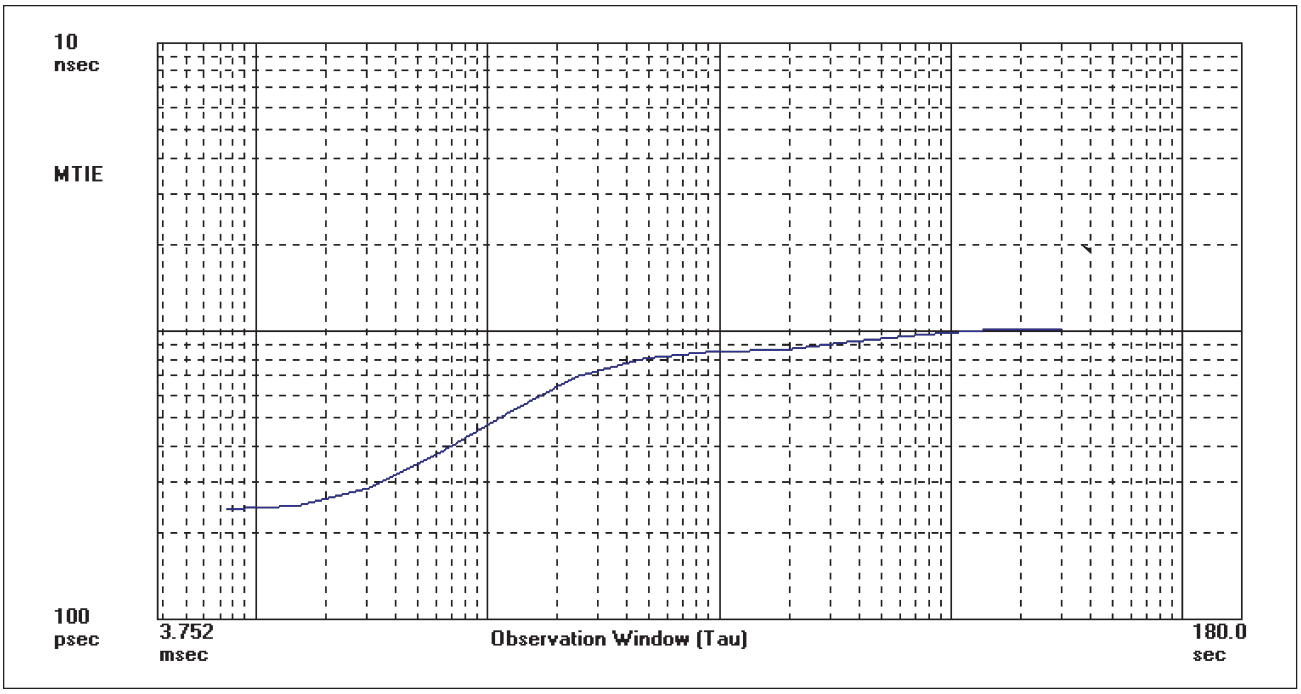
Switch from A to B after auto Free Run due to loss of both references

Figure 11



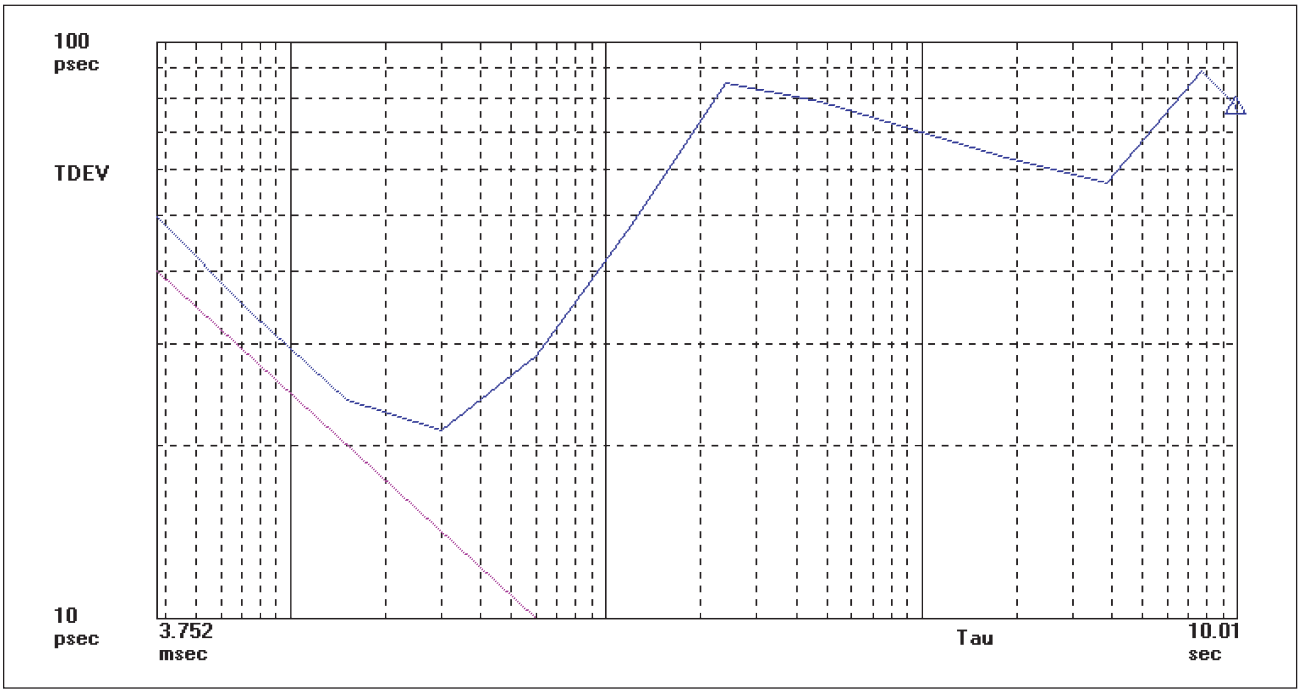
Typical MTIE Measurement

Figure 12



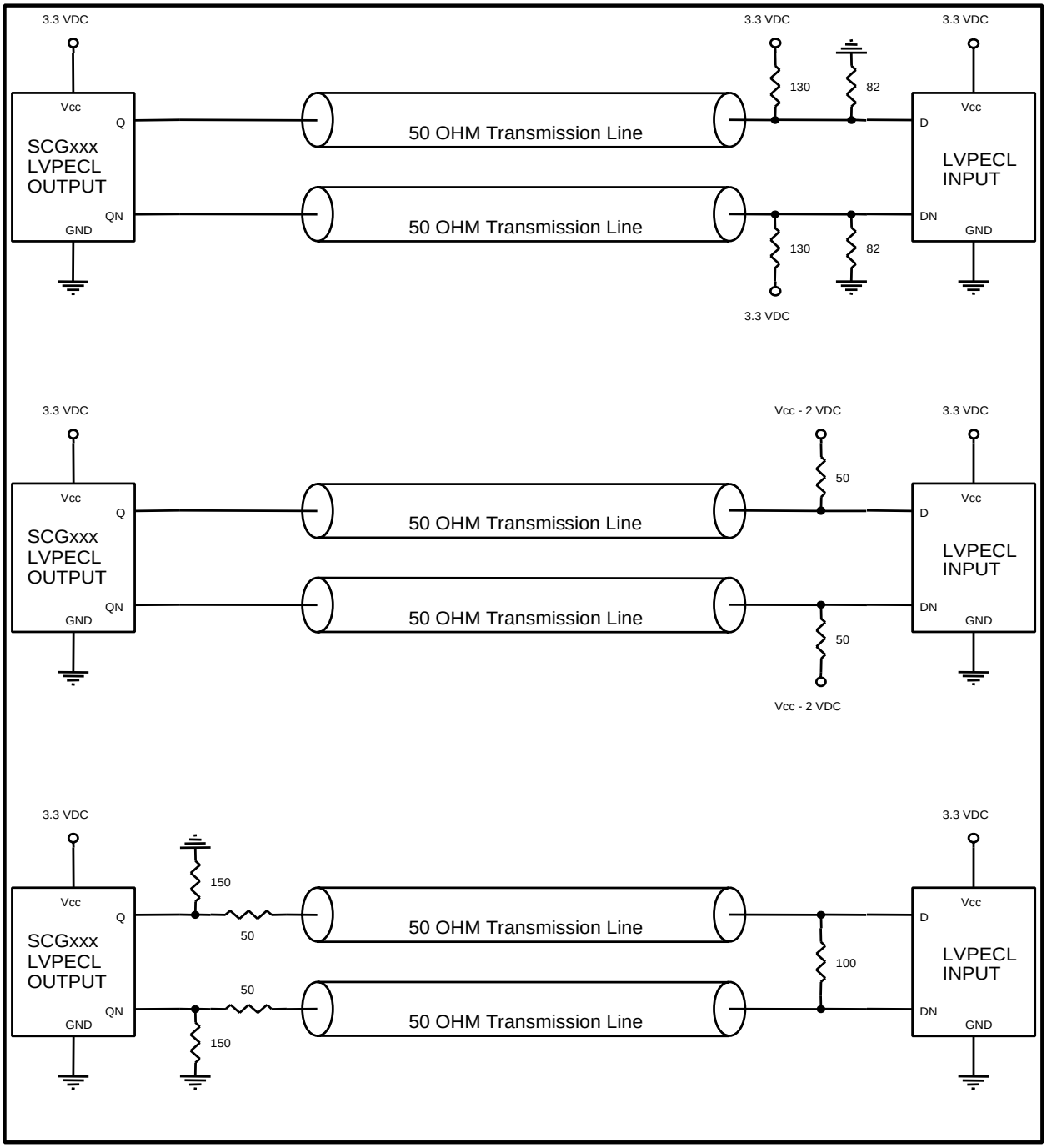
Typical TDEV Measurement

Figure 13



Recommended PECL Termination

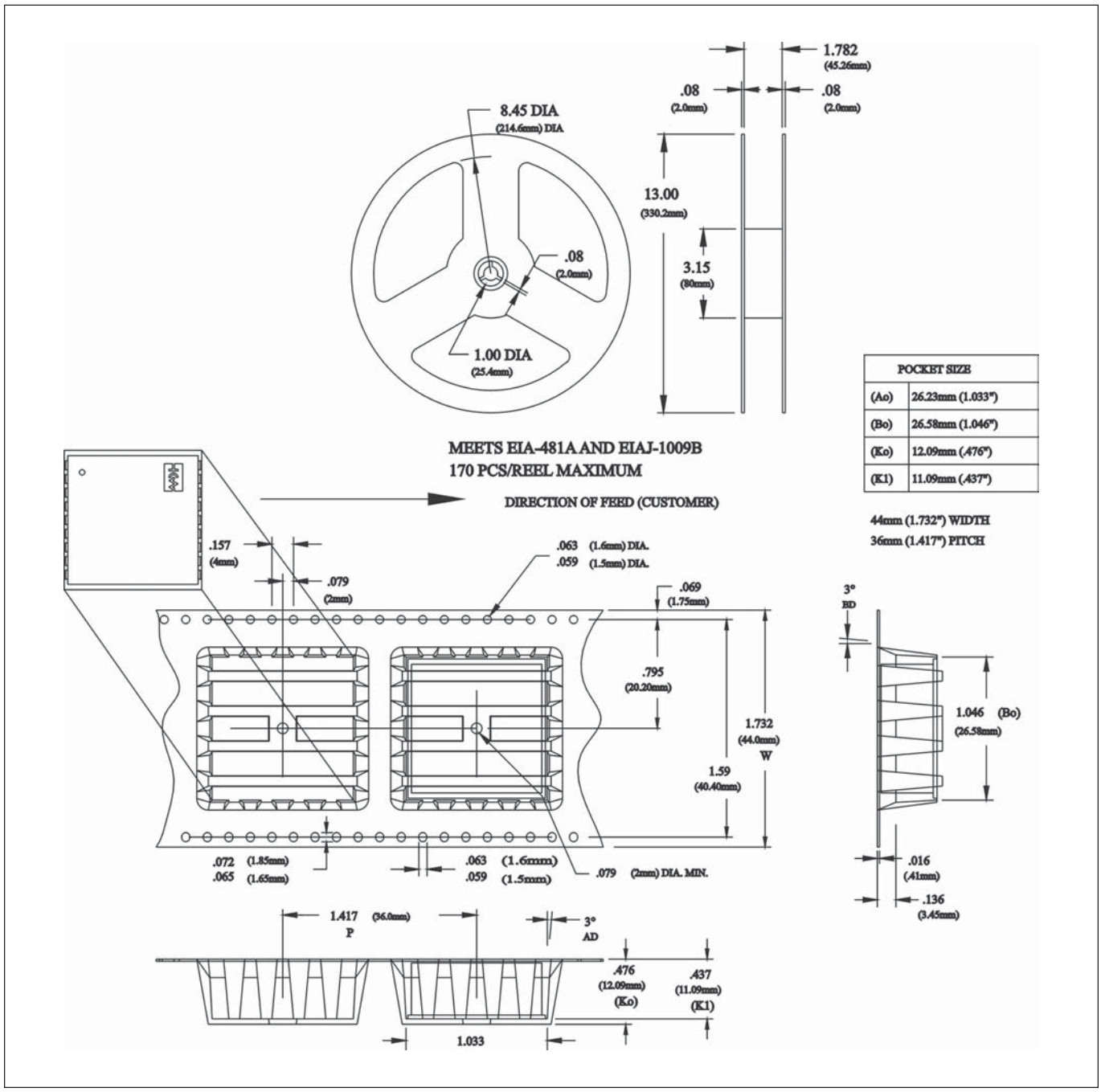
Figure 14



If PECL outputs do not drive a long line (< 0.5”),
a single 150Ω termination resistor to ground may be used for each pin.

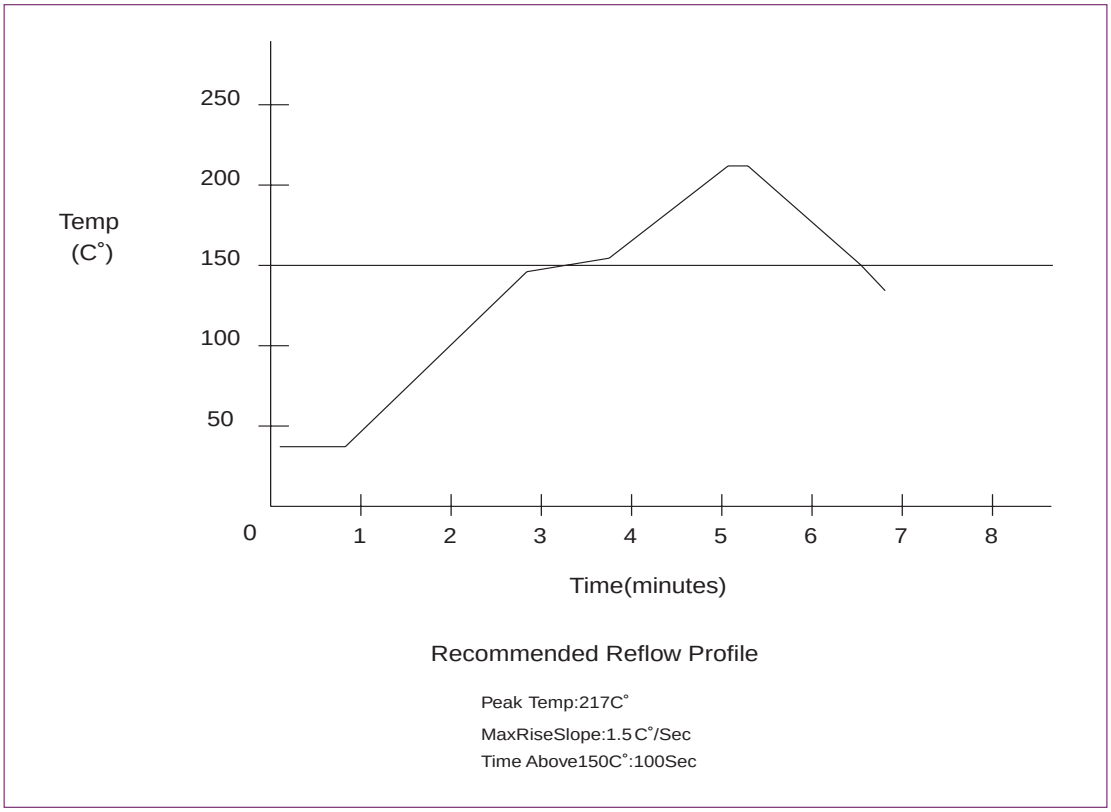
Tape and Reel Packaging

Figure 15



Solder Profile

Figure 16



Ordering Information

SCG{XXXX}-{FFF.FFF}{M}

XXXX equals a specific model (4540)
FFF.FFF equals the Oscillator Output frequency (163.84 MHz)
M equals MHZ and is added to all part numbers

Example: To order an SCG4540 with an Oscillator Output of 163.84 MHz,
Order part number 4540-163.84M

Please contact Connor-Winfield for other frequencies that may be available.

Revision	Revision Date	Note
P00	07/08/02	Preliminary informational release
P01	08/05/02	Advanced to Ver 3