

# P3PSL450A

## Low Voltage, Timing-Safe™ Peak EMI Reduction IC

### Functional Description

P3PSL450A/AH is a versatile low voltage peak EMI reduction IC based on Timing-Safe technology. P3PSL450A/AH accepts one input from an external reference, and locks on to it delivering a 1x Timing-Safe output clock. P3PSL450A/AH has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer *frequency Selection table*. The device has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected at this pin to GND. P3PSL450A/AH has an MR pin for selecting one of the two Modulation Rates. PD# provides the Power Down option.

P3PSL450A is a Low drive part and P3PSL450AH is a High drive part. Refer to *DC/AC Electrical characteristic table*.

P3PSL450A/AH operates over a supply voltage range of 1.8 V ± 0.2 V, and is available in an 8 Pin WDFN (2 mm x 2 mm) Package.

### General Features

- 1x, LVCMOS Timing-Safe Peak EMI Reduction
- Input Clock Frequency: 15 MHz – 60 MHz
- Output Clock Frequency (Timing-Safe): 15 MHz – 60 MHz
- Analog Frequency Deviation Selection
- Two different Modulation Rate Selection Option
- Power Down option for Power Save
- Low and High Drive Parts
- Supply Voltage: 1.8 V ± 0.2 V
- 8 Pin WDFN (2 mm X 2 mm) Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Application

- P3PSL450A/AH is targeted for use in consumer electronic applications like mobile phones, Camera modules, MFP and DPF

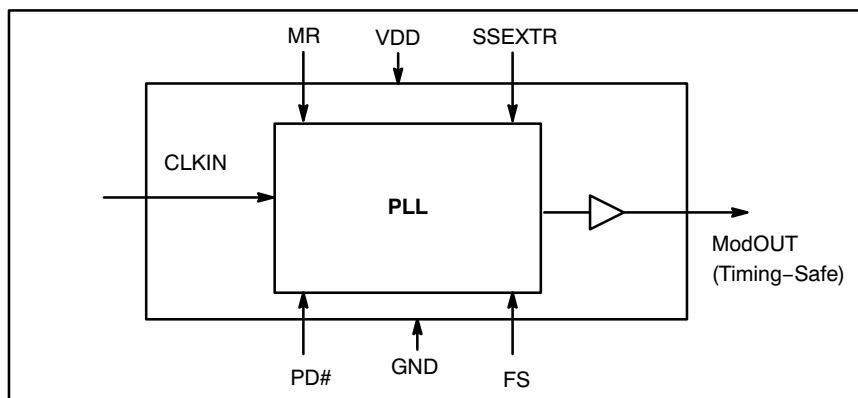
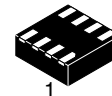


Figure 1. Block Diagram



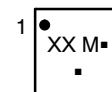
ON Semiconductor®

<http://onsemi.com>



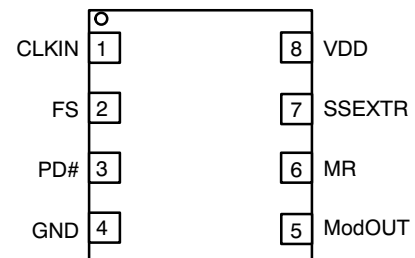
WDFN8  
CASE 511AQ

### MARKING DIAGRAM



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

### PIN CONFIGURATION



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# P3PSL450A

**Table 1. PIN DESCRIPTION**

Pin #	Pin Name	Type	Description
1	CLKIN	I	External reference Clock input.
2	FS	I	Frequency Select. Has an internal pull-down resistor. see <i>Frequency Selection table</i>
3	PD#	I	Power Down. Pull LOW to enable Power Down. Pull HIGH to disable power down. Output Clock will be LOW when power down is enabled. Has an internal pull-up resistor
4	GND	P	Ground
5	ModOUT	O	Buffered modulated Timing-Safe clock output
6	MR	I	Modulation Rate Select. When LOW selects Low Modulation Rate. Selects High Modulation Rate when pulled HIGH. Has an internal pull-up resistor.
7	SSEXTR	I	Analog Frequency Deviation Selection through external resistor to GND.
8	VDD	P	1.8 V Supply Voltage

**Table 2. FREQUENCY SELECTION TABLE**

FS	Frequency (MHz)
0	15-30
1	30-60

**Table 3. ABSOLUTE MAXIMUM RATING**

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.3	+2.7	V
DC Input Voltage(CLKIN)	-0.3	+2.7	V
DC Input Voltage (Except CLKIN)	-0.3	V <sub>DD</sub> + 0.3	V
Storage Temperature	-65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22-A114-B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	1.6	2	V
T <sub>A</sub>	Operating Temperature	-20	+85	°C
C <sub>L</sub>	Load Capacitance		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

## P3PSL450A

**Table 5. DC ELECTRICAL CHARACTERISTICS FOR  $V_{DD} = 1.8\text{ V} \pm 0.2\text{ V}$**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage		1.6	1.8	2	V
V <sub>IH</sub>	Input HIGH Voltage		0.65 * V <sub>DD</sub>			V
V <sub>IL</sub>	Input LOW Voltage				0.35 * V <sub>DD</sub>	V
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>DD</sub>			5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0 V			5	μA
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -8 mA (P3PSL450A)	0.75 * V <sub>DD</sub>			V
		I <sub>OH</sub> = -16 mA (P3PSL450AH)				
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 8 mA (P3PSL450A)			0.25 * V <sub>DD</sub>	V
		I <sub>OL</sub> = 16 mA (P3PSL450AH)				
I <sub>CC</sub>	Static Supply Current	CLKIN & PD# pins pulled to GND			10	μA
I <sub>DD</sub>	Dynamic Supply Current	Unloaded Output	FS = 0, @ 15 MHz	1.7	2.2	mA
			FS = 0, @ 30 MHz	3.0	3.7	
			FS = 1, @ 30 MHz	2.6	3.7	
			FS = 1, @ 60 MHz	4.3	6.4	
Z <sub>o</sub>	Output Impedance	P3PSL450A		23		Ω
		P3PSL450AH		17		

**Table 6. AC ELECTRICAL CHARACTERISTICS FOR  $V_{DD} = 1.8\text{ V} \pm 0.2\text{ V}$**

Parameter	Test Conditions	Min	Typ	Max	Unit	
Input Frequency	FS = 0	15		30	MHz	
	FS = 1	30		60		
ModOUT	FS = 0	15		30		
	FS = 1	30		60		
Duty Cycle (Notes 1 and 2)	Measured at V <sub>DD</sub> / 2	45	50	55	%	
Rise Time (Notes 1 and 2)	Measured between 20% to 80%	P3PSL450A	1.3	2.1	ns	
		P3PSL450AH	1	1.7		
Fall Time (Notes 1 and 2)	Measured between 80% to 20%	P3PSL450A	1.3	2.1	ns	
		P3PSL450AH	1	1.7		
Cycle-to-Cycle Jitter (Note 2)	Unloaded output with SSEXTR pin OPEN	FS = 0	15 MHz	± 150	± 250	ps
			24 MHz	± 100	± 150	
			30 MHz	± 80	± 150	
		FS = 1	30 MHz	± 150	± 250	
			60 MHz	± 100	± 150	
PLL Lock Time <sup>2</sup>	Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High			1	ms	

1. All parameters are specified with 15 pF loaded output.

2. Parameter is guaranteed by design and characterization. Not 100% tested in production

# P3PSL450A

## SWITCHING WAVEFORMS

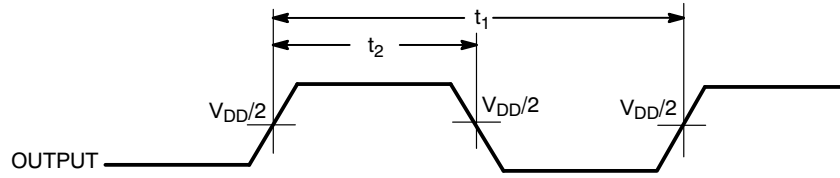


Figure 2. Duty Cycle Timing

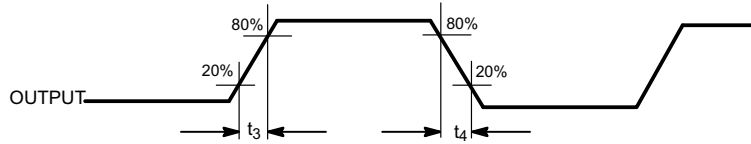
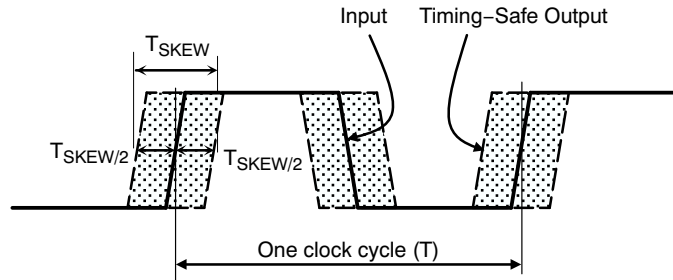


Figure 3. Output Rise/Fall Time



$T_{SKEW}$  represents input-output skew when spread spectrum is ON  
For example,  $T_{SKEW}/2 = \pm 0.20 * T$  for an Input clock of 24 MHz, translates in to  
 $(1/24 \text{ MHz}) * 0.20 = 8.33 \text{ ns}$

Figure 4. Input-Output Skew

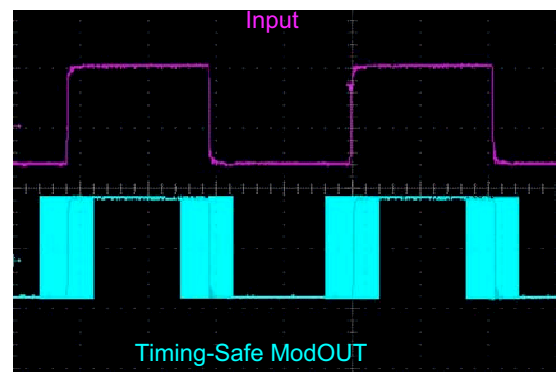
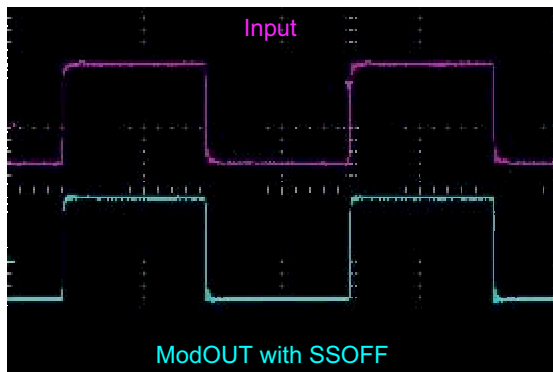


Figure 5. Typical Example of Timing-Safe Waveform

DEVIATION VERSUS SSEXTR RESISTANCE CHARTS

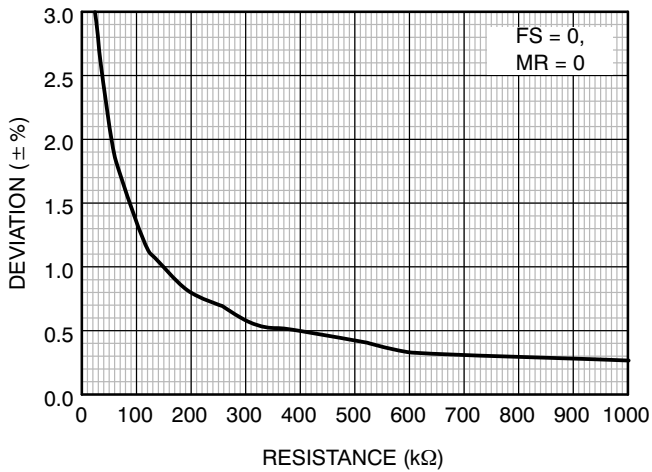


Figure 6. Deviation vs SSEXTR Chart (CLKIN = 15 MHz)

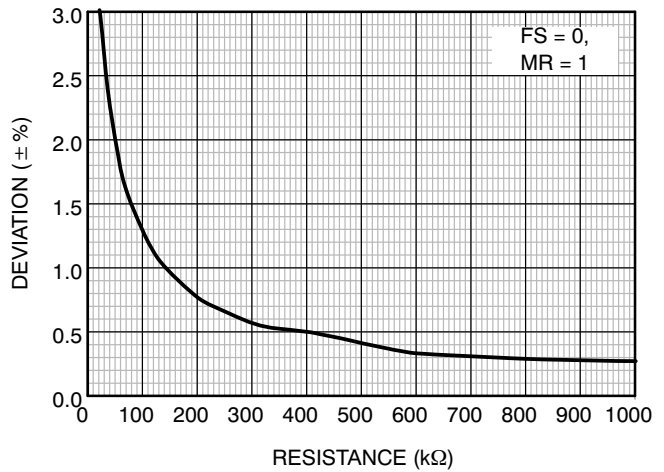


Figure 7. Deviation vs SSEXTR Chart (CLKIN = 15 MHz)

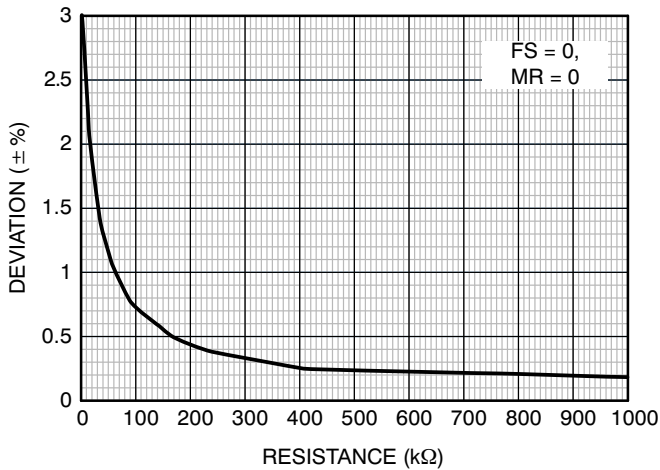


Figure 8. Deviation vs SSEXTR Chart (CLKIN = 24 MHz)

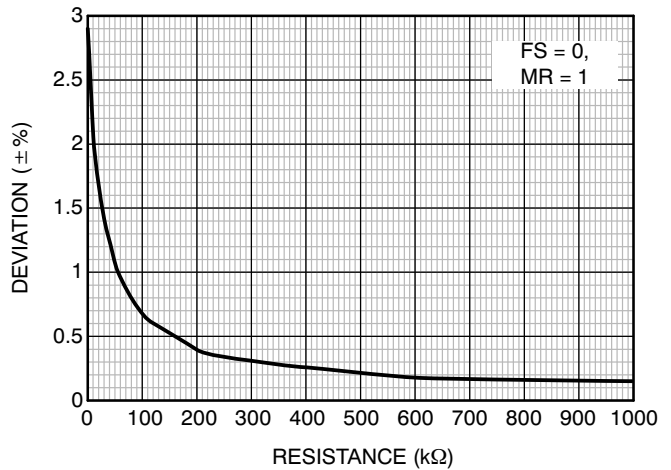


Figure 9. Deviation vs SSEXTR Chart (CLKIN = 24 MHz)

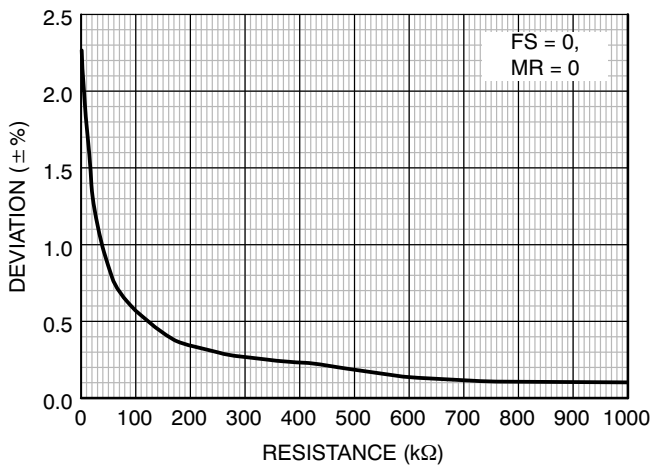


Figure 10. Deviation vs SSEXTR Chart (CLKIN = 30 MHz)

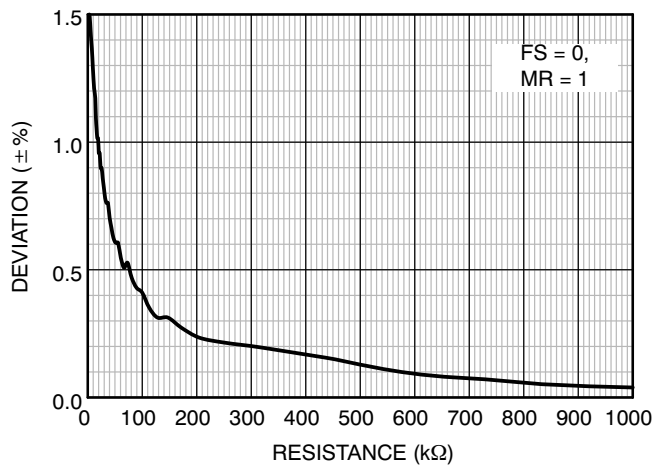


Figure 11. Deviation vs SSEXTR Chart (CLKIN = 30 MHz)

DEVIATION VERSUS SSEXTR RESISTANCE CHARTS

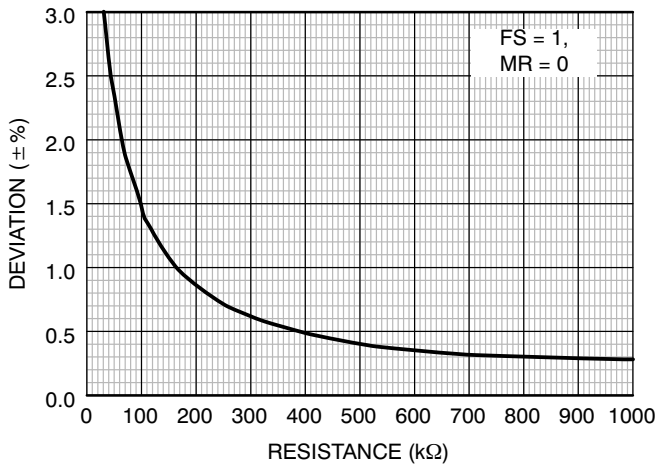


Figure 12. Deviation vs SSEXTR Chart  
(CLKIN = 30 MHz)

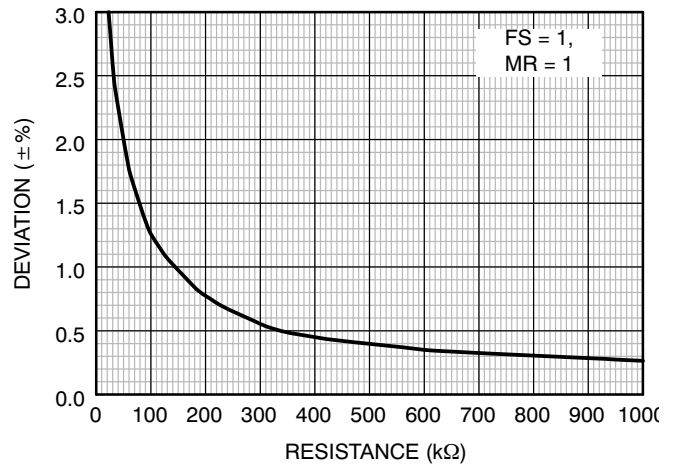


Figure 13. Deviation vs SSEXTR Chart  
(CLKIN = 30 MHz)

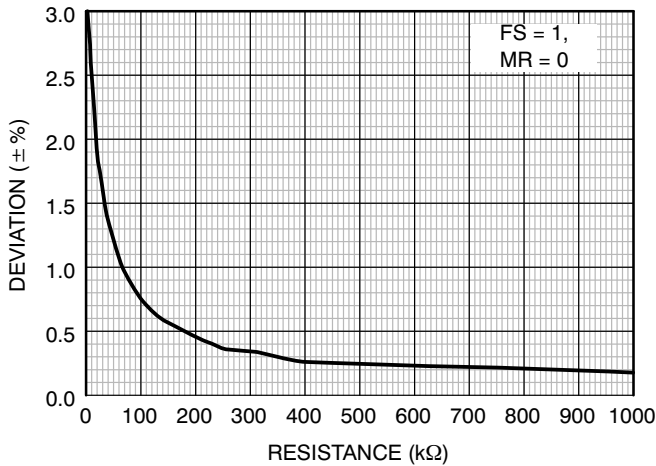


Figure 14. Deviation vs SSEXTR Chart  
(CLKIN = 48 MHz)

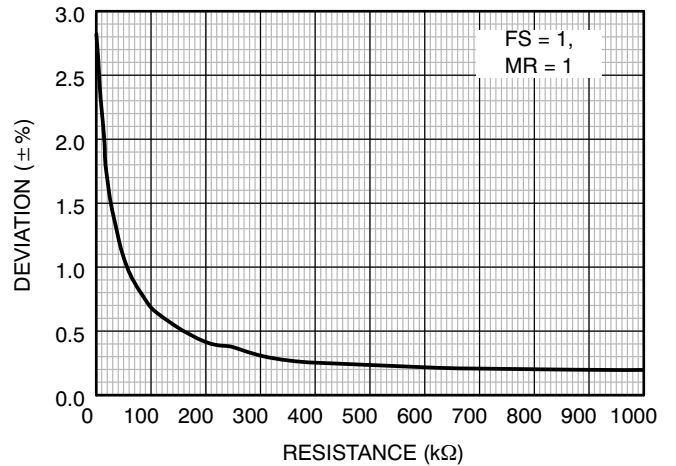


Figure 15. Deviation vs SSEXTR Chart  
(CLKIN = 48 MHz)

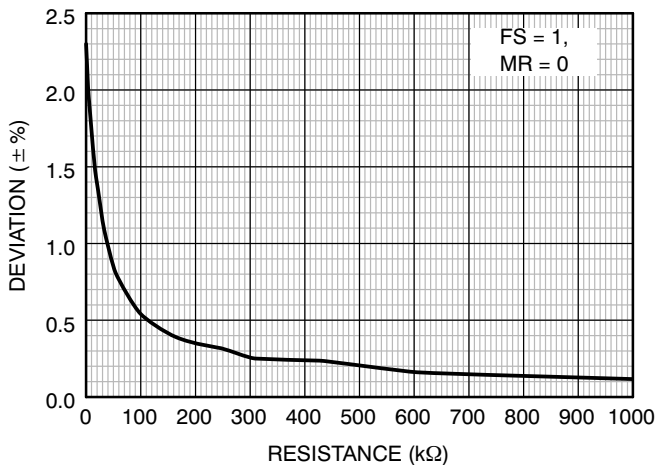


Figure 16. Deviation vs SSEXTR Chart  
(CLKIN = 60 MHz)

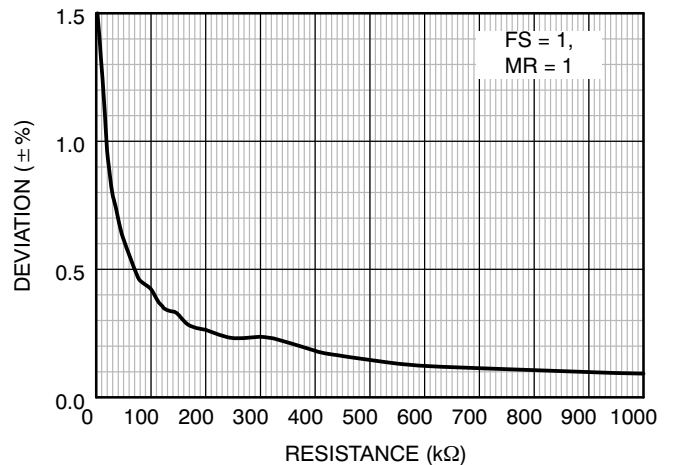
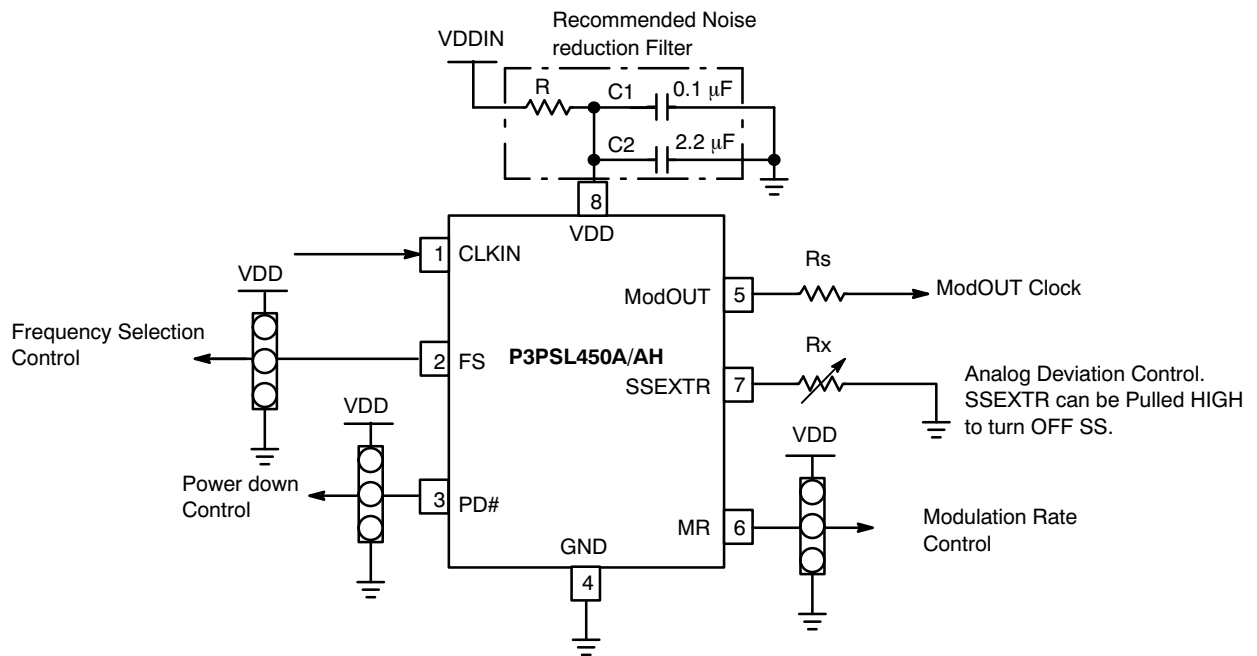


Figure 17. Deviation vs SSEXTR Chart  
(CLKIN = 60 MHz)

# P3PSL450A



NOTE: Refer to Pin Description table for Functionality details

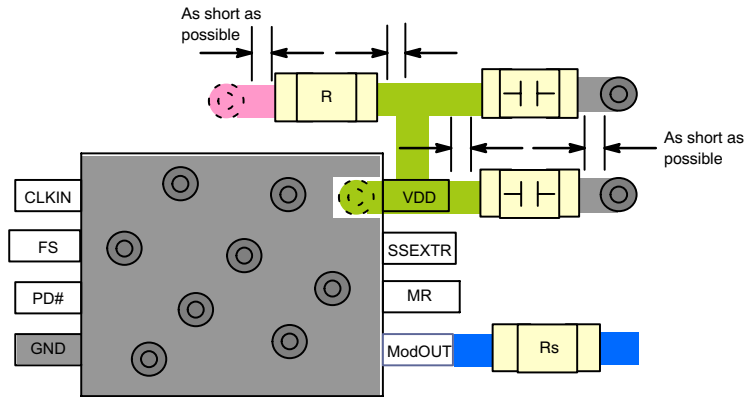
**Figure 18. Typical Application Schematic**

# P3PSL450A

## PCB LAYOUT RECOMMENDATION

For optimum device performance, following guidelines are recommended.

- Dedicated  $V_{DD}$  and GND planes.
- The device must be isolated from system power supply noise. A 0.1  $\mu\text{F}$  and a 2.2  $\mu\text{F}$  decoupling capacitor should be mounted on the component side of the board as close to the  $V_{DD}$  pin as possible. No vias should be used between the decoupling capacitor and  $V_{DD}$  pin. The PCB trace to  $V_{DD}$  pin and the ground via should be kept as short as possible. All the  $V_{DD}$  pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers. A typical layout is shown in the Figure below:



## ORDERING INFORMATION

Ordering Code	Marking	Temperature	Package Type	Shipping <sup>†</sup>
P3PSL450AG-08CR	FA	-20°C to +85°C	8-pin (2 mm x 2 mm) WDFN (Pb-Free)	Tape & Reel
P3PSL450AHG-08CR	FC	-20°C to +85°C	8-pin (2 mm x 2 mm) WDFN (Pb-Free)	Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

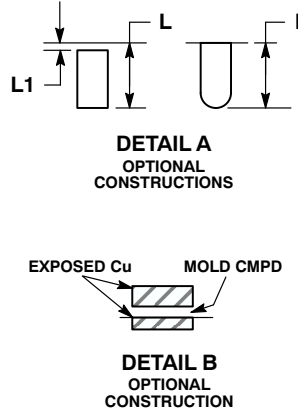
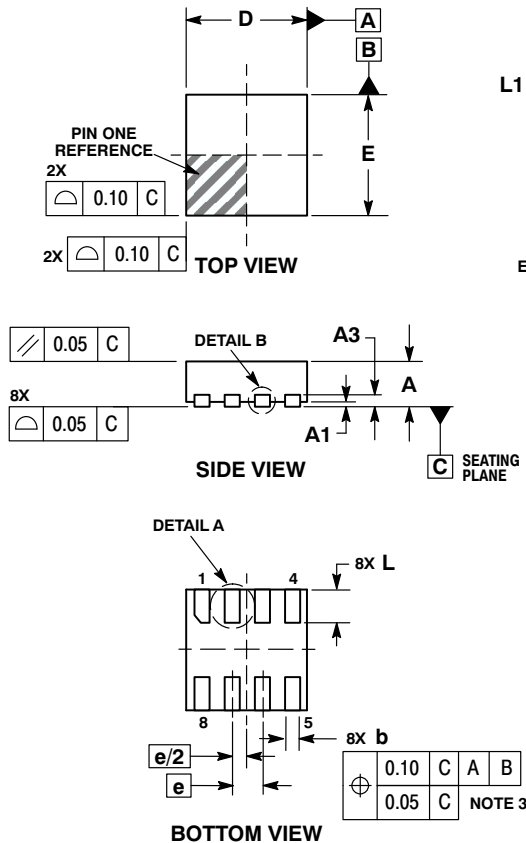
\*A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-Free.



# P3PSL450A

## PACKAGE DIMENSIONS

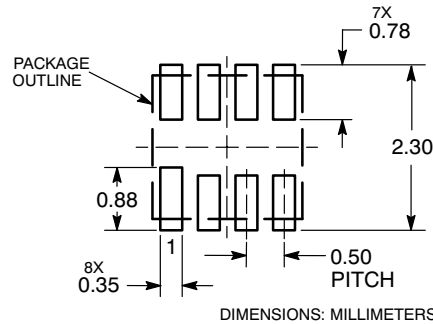
WDFN8 2x2, 0.5P  
CASE 511AQ-01  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Timing-Safe is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative