Ordering number : ENN*7051

CMOS IC

LC35W256GM, GT-70U

256K (32768-words × 8-bit) SRAM with $\overline{OE}$ and $\overline{CE}$ control pins

Preliminary

Overview

The LC35W256GM-70U and LC35W256GT-70U are 32768-words by 8-bit asynchronous silicon gate low supply voltage CMOS SRAMs. These devices adopt a full-CMOS type six-transistor memory cell, and feature ultralow supply voltage operation, a low operating mode current drain, and an ultralow standby mode current drain. These device provide an $\overline{OE}$ pin for high-speed memory access and a $\overline{CE}$ chip select pin for device selection and low power mode control. Thus these devices are optimal for use in systems that require low power and battery backup. They also allow easy expansion of memory capacities. Their ultralow standby mode current drain allows them to be used in capacitor backed up systems.

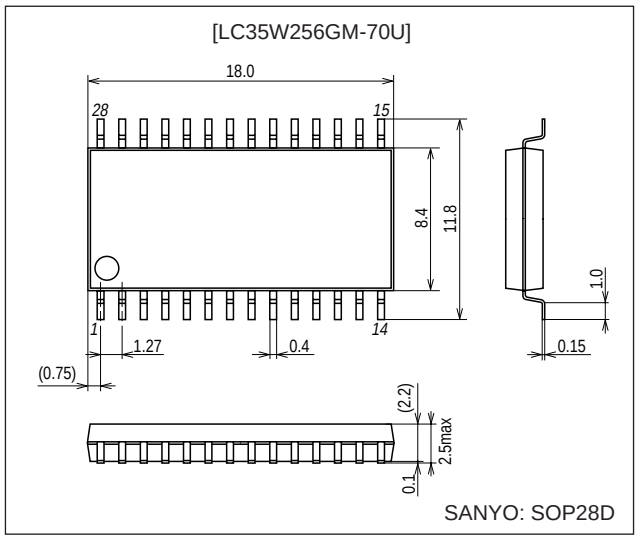
Features

- Supply Voltage : 2.7V to 3.6V
- Access time : 70 ns (max.)
- Standby current : 2.0 µA (Ta ≤ 70°C)
  : 5.0 µA (Ta ≤ 85°C)
- Operating Temperature : –40°C to +85°C
- DATA Retention Voltage : 2.0 V to 3.6 V
- Input Levels : CMOS-Compatible
  [0.2 V_{CC}/0.8 V_{CC}]
- SOP28 (450mil) Plastic Package
- Control Input ($\overline{OE}$, $\overline{CE}$)
- Common Input/Output Pins, Three-state Outputs
- No Clocks or Timing Signals Required

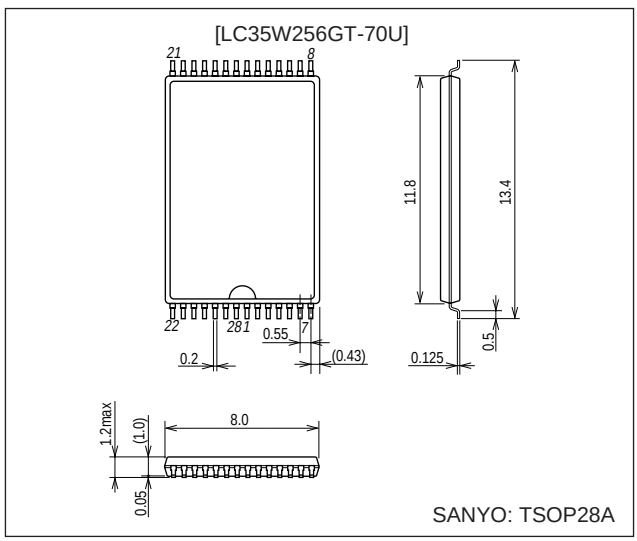
Package Dimensions

unit: mm

3187B-SOP28D



3221-TSOP28A



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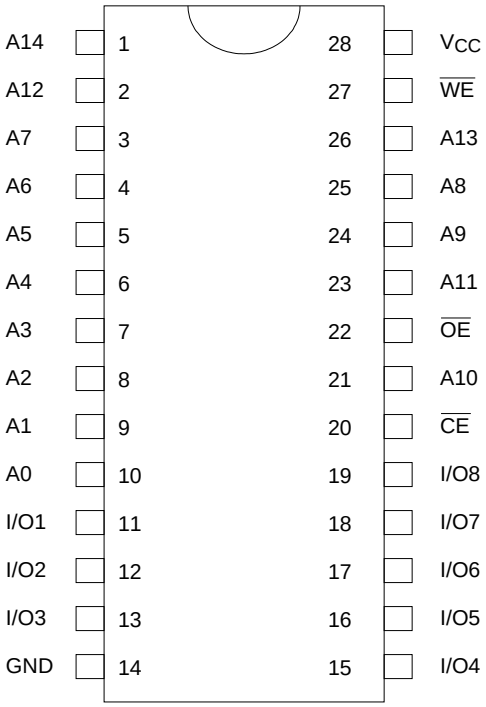
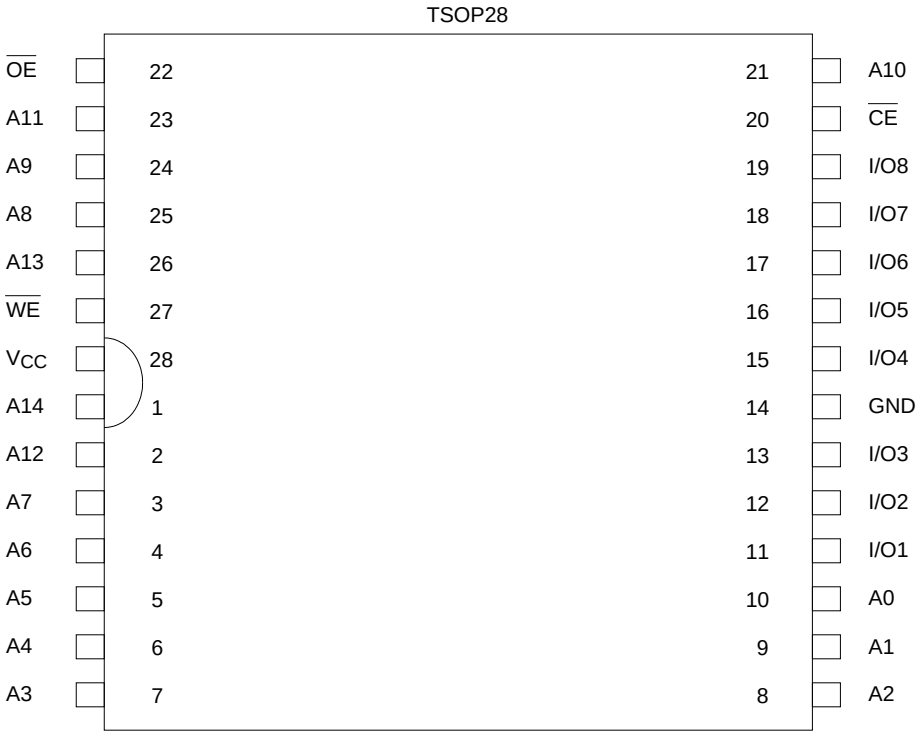
Pin Assignment

SOP28



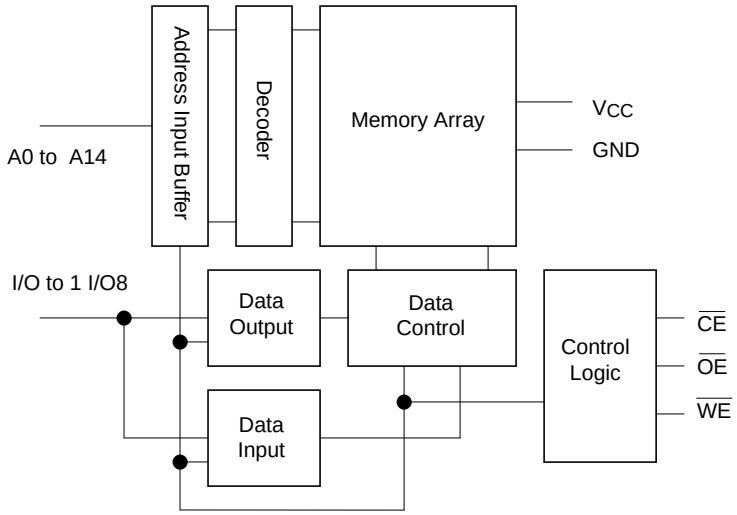
Top view

TSOP28



Top view

Block Diagram



Pin Name

Pin Name	Pin function	Pin Name	Pin function
$\overline{CE}$	Chip Enable Input	V_{CC}	Power
$\overline{OE}$	Output Enable Input	GND	Ground
$\overline{WE}$	Write Enable Input	I/O1 to I/O8	Data Inputs/Outputs
Ao to A14	Address Inputs	NC	No Conect

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Current
Read Cycle	L	L	H	Data Output	I_{CCA}
Write Cycle	L	X	L	Data Input	I_{CCA}
Output Disable	L	H	H	High Impedance	I_{CCA}
Unselected	H	X	X	High Impedance	I_{CCS}

X: Arbitrary H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Max Supply Voltage	V_{CC} max		+4.6	V
Input Voltage	V_{IN}		–0.3* to V_{CC} +0.3	V
I/O Voltage	$V_{I/O}$		–0.3 to V_{CC} +0.3	V
Operating Temperature Range	Topr		–40 to +85	°C
Storage Temperature Range	Tstg		–55 to +125	°C

Note*: The inputs may undershoot to –2.0V(min.)for periods less than 30ns.

I/O Capacitances at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		6	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0 V		6	10	pF

Note*: This parameter is sampled and not 100% tested.

Recommended DC Operating at Ta = –40°C to +85°C, V_{CC} = 2.7 V to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply Voltage	V_{CC}		2.7	3.0	3.6	V
Input Voltage	V_{IH}		0.8 × V_{CC}		V_{CC} + 0.3	V
	V_{IL}		–0.3*		0.2 × V_{CC}	V

Note*: The inputs may undershoot to –2.0V(min.)for periods less than 30ns.

DC Characteristics at Ta = –40°C to +85°C, V_{CC} = 2.7 V to 3.6 V

Parameter		Symbol	Conditions		Ratings			Unit
					min	typ	max	
Input Leakage Current		I_{LI}	V_{IN} = 0 to V_{CC}		–1.0		+1.0	µA
I/O Leakage Current		I_{LO}	$V_{\overline{CE}}$ = V_{IH} or $V_{\overline{CE}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, $V_{I/O}$ = 0 to V_{CC}		–1.0		+1.0	µA
Output High Level Voltage		V_{OH1}	I_{OH1} = –2.0 mA		V_{CC} – 0.4			V
		V_{OH2}	I_{OH2} = –100 µA		V_{CC} – 0.1			V
Output Low Level Voltage		V_{OL1}	I_{OL1} = 2.0 mA				0.4	V
		V_{OL2}	I_{OL2} = 100 µA				0.1	V
Operating Current	CMOS Input	I_{CCA2}	$V_{\overline{CE}}$ = V_{IL}, $I_{I/O}$ = 0 mA, V_{IN} = V_{IH} or V_{IL}				1.2	mA
		I_{CCA3}	V_{CE} = V_{IL}, $I_{I/O}$ = 0 mA, V_{IN} = V_{IH} or V_{IL}, duty = 100%	70 ns cycle		20	25	mA
				100 ns cycle		15	18	mA
				1 µs cycle		1.5	2.5	mA
Standby Current	V_{CC}-0.2 V/0.2 V Input	I_{CCS1}	V_{CE} ≥ V_{CC} – 0.2 V, V_{IN} = 0 to V_{CC}	Ta ≤ 25°C		0.01		µA
				Ta ≤ 70°C			2.0	µA
				Ta ≤ 85°C			5.0	µA
	CMOS Input	I_{CCS2}	V_{CE} = V_{IH}, V_{IN} = 0 to V_{CC}				0.4	mA

Note*: Reference value at V_{CC} = 3.0 V, Ta = +25°C

AC Characteristics at Ta = –40°C to +85°C, V_{CC} = 2.7V to 3.6V

AC Test Conditions

Input Pulse Level : $V_{IL} = 0.2 \times V_{CC}$, $V_{IH} = 0.8 \times V_{CC}$

Input Rise and Fall Time : 5 ns

Input and Output Timing Reference Levels : $0.5 \times V_{CC}$

Output Load : 30 pF (Including scope and jig)

READ CYCLE

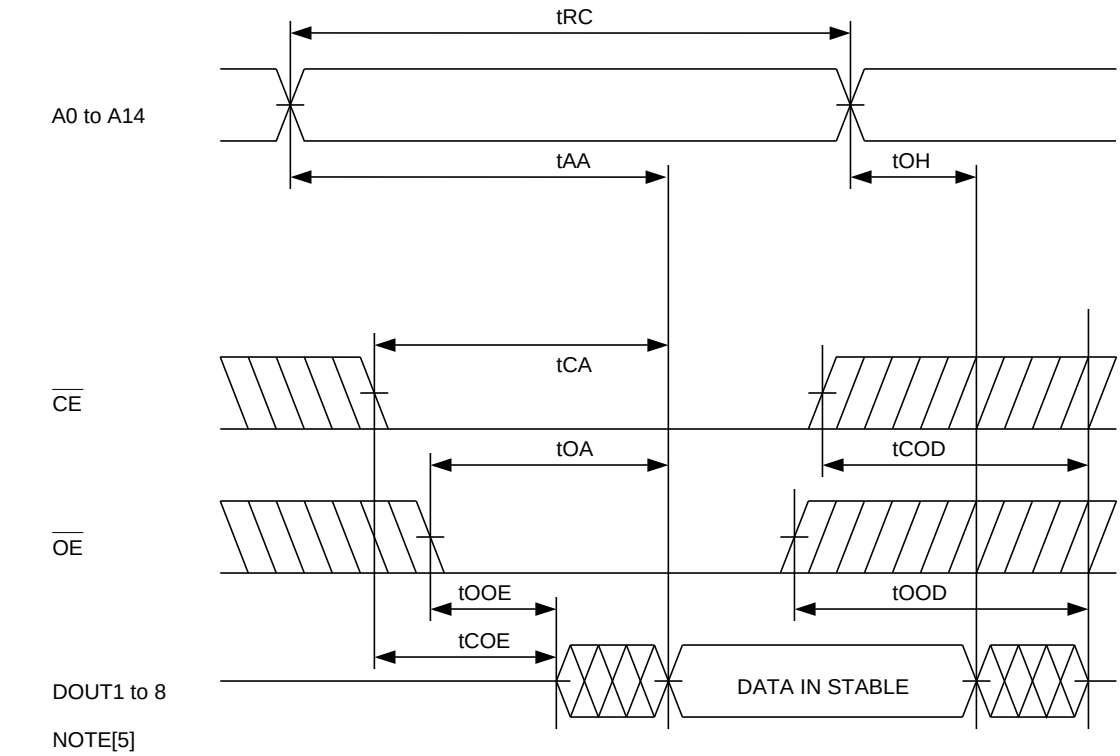
Parameter	Symbol	LC35W256GM, GT-70U		Unit
		min	max	
Read Cycle Time	tRC	70		ns
Address Access Time	tAA		70	ns
$\overline{CE}$ Access Time	tCA		70	ns
$\overline{OE}$ Access Time	tOA		35	ns
Output Hold Time	tOH	10		ns
$\overline{CE}$ Output Enable Time	tCOE	10		ns
$\overline{OE}$ Output Enable Time	tOOE	5		ns
$\overline{CE}$ Output Disable Time	tCOD		30	ns
$\overline{OE}$ Output Disable Time	tOOD		25	ns

WRITE CYCLE

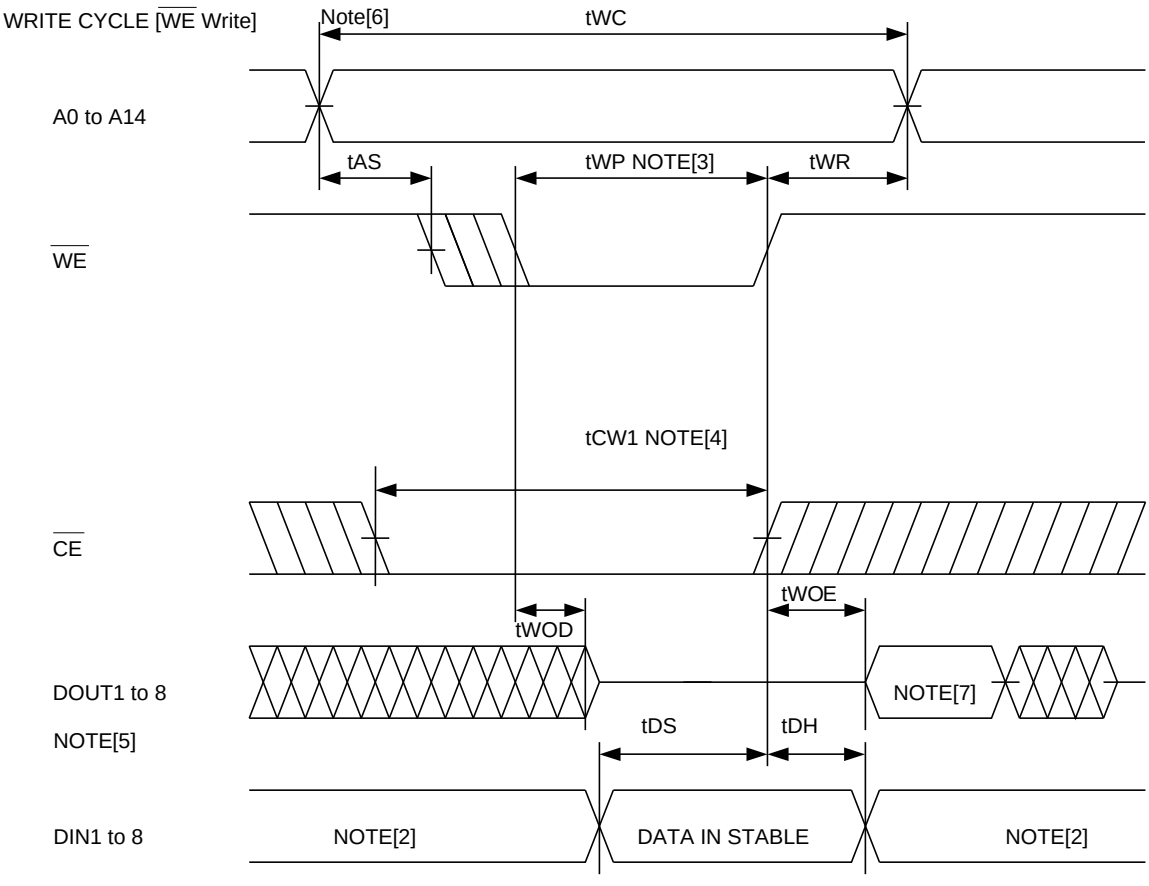
Parameter	Symbol	LC35W256GM, GT-70U		Unit
		min	max	
Write Cycle Time	tWC	70		ns
Address Setup Time	tAS	0		ns
Write Pulse Width	tWP	50		ns
$\overline{CE}$ Setup Time	tCW	60		ns
Write Recovery Time	tWR	0		ns
$\overline{CE}$ Recovery Time	tWR1	0		ns
Data Setup Time	tDS	40		ns
Data Hold Time	tDH	0		ns
$\overline{CE}$ Data Hold Time	tDH1	0		ns
$\overline{WE}$ Output Enable Time	tWOE	5		ns
$\overline{WE}$ Output Disable Time	tWOD		30	ns

Timing Waveform

READ CYCLE Note[1]

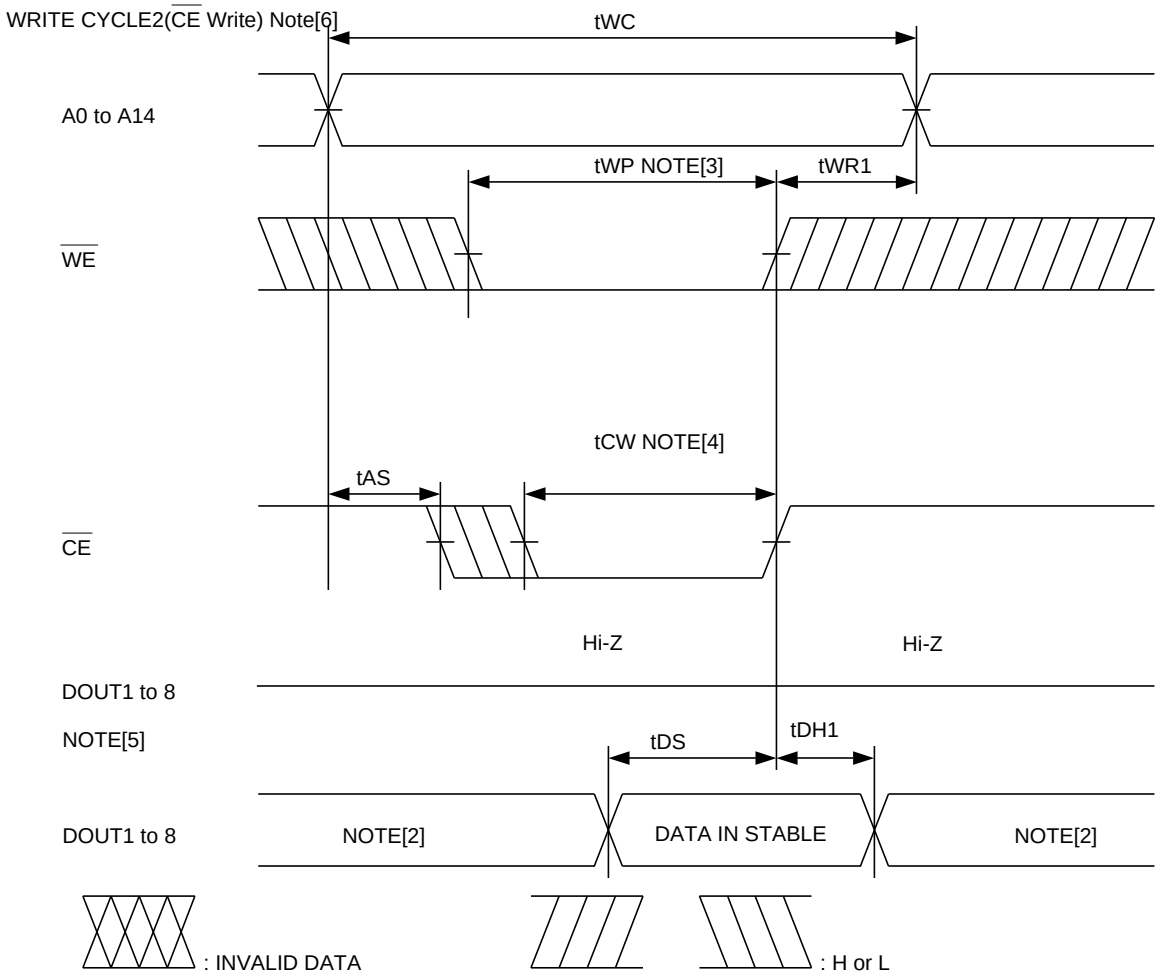


WRITE CYCLE [WE Write]



: INVALID DATA : H or L

WRITE CYCLE2 ($\overline{CE}$ Write) Note[6]



Notes:

(1) In read cycle, $\overline{WE}$ should be high.

(2) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

(3) The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. tWP is measured from the falling edge of $\overline{WE}$ to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

(4) The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. tCW is measured from the falling edge of $\overline{CE}$ to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

(5) If one of these conditions[$\overline{OE}$ is high, $\overline{CE}$ is high, $\overline{WE}$ is low] at least is satisfied, DOUT goes to high impedance state.

(6) In write cycle, $\overline{OE}$ =V_{IH} or V_{IL}.

(7) DOUT is in the same phase of written data of this cycle.

- Functional operation of the device at any conditions beyond “absolute maximum ratings” is not implied.
- CMOS-LSI input pins must be high or low to prevent them from floating or the level which neither V_{IH} nor V_{IL}.

Circuit Design Notes

When designing an actual application circuit, consider each of the following aspects and assure that none of the maximum ratings are ever exceeded.

- Supply voltage fluctuations
- Sample-to-sample variations in electrical characteristics of the electrical components used, including semiconductor devices, resistors, and capacitors.
- The ambient temperature
- Fluctuations in the input and clock signals
- Possible application of abnormal pulses

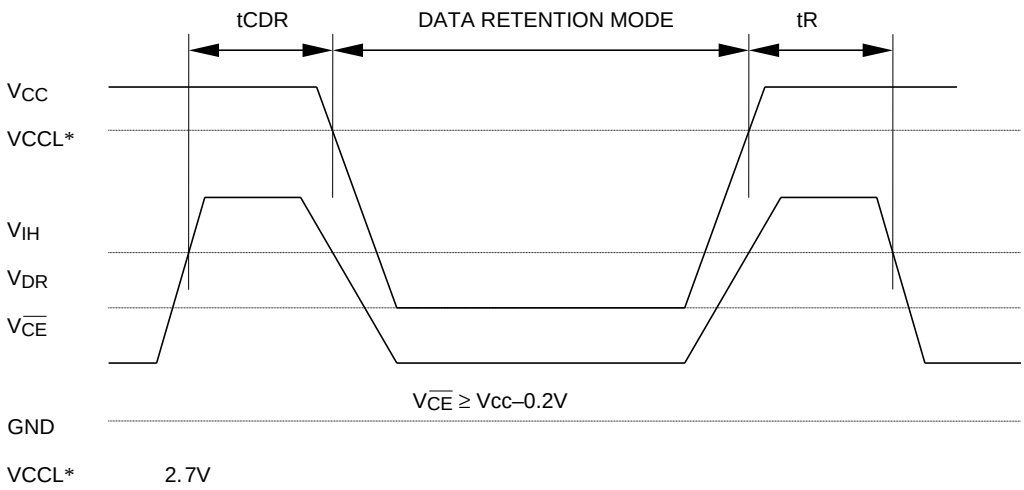
Also, these ICs must be operated within the allowable operating ranges. If any of the input pins on this CMOS IC are left open, intermediate potentials may be generated leading to incorrect operation due to through currents or other phenomenon. Unused input pins must be handled as stipulated.

Data Retention Characteristics at Ta = –40°C to +85°C

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Data Retention Power Supply Voltage	V_{DR}	$V_{CE} \geq V_{CC} - 0.2$ V		2.0		3.6	V
Data Retention Current	I_{CCDR}	V_{CC} = 3 V, $V_{CE} \geq V_{CC} - 0.2$ V	Ta ≤ 85°C			2.0	µA
			Ta ≤ 70°C			1.5	µA
			Ta ≤ 25°C		0.01		µA
Chip Enable Setup Time	tCDR			0			ns
Chip Enable Hold Time	tR			tRC*			ns

Note*: Read Cycle Time

Data Retention Waveform [1]



This catalog provides information as of January, 2003. Specifications and information herein are subject to change without notice.