L5300AH7

5 V low drop voltage regulator

Features

Max DC supply voltage	V_s	40 V
Max output voltage tolerance	ΔV_0	+/-2 %
Max dropout voltage	V_{dp}	500 mV
Output current	I_0	300 mA
Quiescent current	I_{qn}	5 µA(1) 55 µA(2)

1. Typical value with regulator disabled
2. Typical value with regulator enabled

- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- 300 mA current capability
- Low quiescent current
- Very low consumption mode
- Precision output voltage 5 V +/-2%
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range (T_j = -40°C to 150°C)
- Enable input for enabling / disabling the voltage regulator

HPAK

Description

L5300AH7 is a low dropout linear regulator with microprocessor control functions such as power on reset, low voltage reset, ON/OFF control. In addition, only low value ceramic capacitor is required for stability (above or equal 220 nF).

Typical quiescent current is 60 µA at output current equal to 0 and enable high. It drops to 10 µA in “not enabled” mode.

On chip trimming results in high output voltage accuracy (2%). Accuracy is kept over wide temperature range, line and load variation.

The maximum input voltage is 40 V. The max output current is internally limited. Internal temperature protection disables the voltage regulator output.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
HPAK	L5300AH7	L5300AH7TR

Contents

List of tables

List of figures

1 Block diagram and pins description

Figure 1. Block diagram

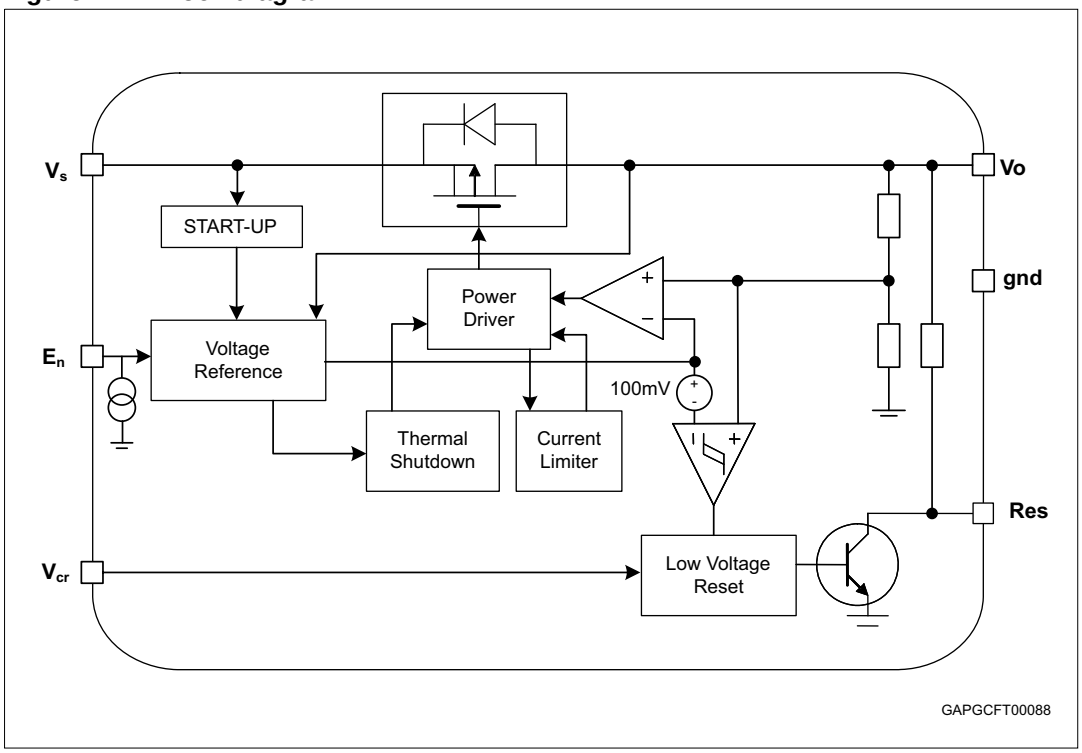


Figure 2. Configuration diagram (top view)

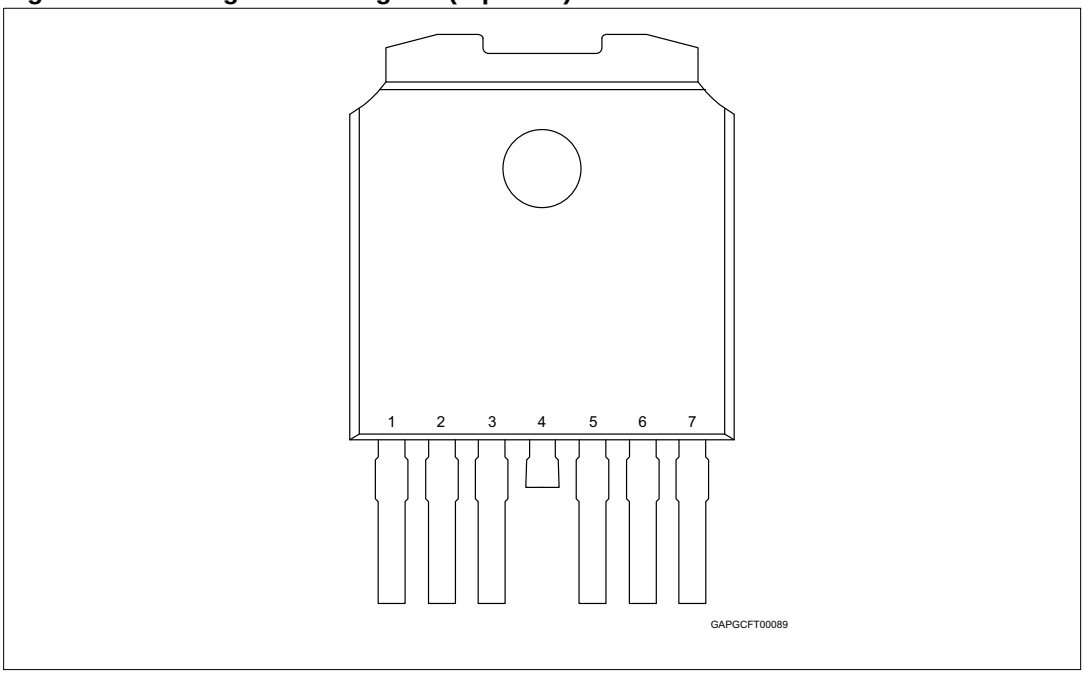


Table 2. Pins description

N°	Name	Function
1	V_S	Supply voltage, block directly to GND on the I_C with a capacitor.
2	E_n	Enable input. A high signal switches the regulator ON. Connect to V_S if not needed.
3	R_{es}	Reset output. Internally connected to V_o through a 20 KΩ pull up resistor. This pin is pulled low when $V_o < V_{o\_th}$. Keep open if not needed.
4	GND	Ground reference.
5	V_{cr}	Reset delay. Connect an external capacitor between V_{cr} pin and ground to adjust the reset delay time. Keep open if not needed.
6	V_{os}	Output voltage sensing: this pin must be connected to V_o.
7	V_o	5 V regulated output. Block to GND with a ceramic capacitor (≥ 220 nF for regulator stability).

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{sdc}	DC supply voltage	-0.3 to 40	V
I_{sdc}	Input current	Internally limited	
V_{odc}	DC output voltage	-0.3 to 6	V
I_{odc}	DC output current	Internally limited	
$V_{od\ Res}$	Open drain output voltage R_{es}	-0.3 to V_{Vodc} + 0.3	V
$I_{od\ Res}$	Open drain output current R_{es}	Internally limited	
V_{cr}	V_{cr} voltage	-0.3 to V_{Vo} + 0.3	V
V_{En}	Enable input	-0.3 to 40	V
T_j	Junction temperature	-40 to 150	°C
$V_{ESD\ HBM}$	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
$V_{ESD\ CDM}$	ESD CDM voltage level (CDM AEC-Q100-011)	+/- 750	V

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case	4.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient	45(1)	K/W

1. The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, double layer with thermal vias (one copper heatsink layer, thickness 0.070 mm, area 8 cm^2).

2.3 Electrical characteristics

Values specified in this section are for V_S = 5.6 V to 31 V, T_j = -40 °C to 150 °C, unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_o	V_{o_ref}	Output voltage	V_S = 8 to 18 V I_O = 8 to 300 mA	4.9	5.0	5.1	V
V_o	V_{o_ref}	Output voltage	V_S = 5.6 to 31 V I_O = 8 to 300 mA	4.85	5.0	5.15	V
V_o	V_{o_ref}	Output voltage	V_S = 5.6 to 31 V I_O = 0.1 mA to 8 mA	4.75	5.0	5.25	V
V_o	I_{short}	Short circuit current	V_S = 13.5 V	0.8	1.8	2.6	A
V_o	I_{lim}	Output current limitation(1)	V_S = 13.5 V	0.6	1.6	2.5	A
V_S, V_o	V_{line}	Line regulation voltage	V_S = 6 V to 28 V I_O = 50 mA			40	mV
V_o	V_{load}	Load regulation voltage	V_S = 13.5 V I_O = 8 mA to 300 mA T_j = 25 °C			40	mV
			V_S = 8 V to 18 V I_O = 8 mA to 300 mA			55	mV
V_S, V_o	V_{dp}	Drop voltage(2)	I_O = 300 mA			500	mV
V_S, V_o	SVR	Ripple rejection	f_r = 100 Hz(3)		60		dB
V_o	I_{oth_H}	Normal consumption mode output current		8			mA
V_o	I_{oth_L}	Very low consumption mode output current				1.1	mA
V_o	I_{oth_Hyst}	Output current switching threshold hysteresis	V_S = 13.5 V, T_j = 25 °C		0.8		mA
V_S, V_o	I_{qs}	Current consumption with regulator disabled $I_{qs} = I_{Vs} - I_O$	V_S = 13.5 V, E_n = low		5	10	µA
V_S, V_o	I_{qn_1}	Current consumption with regulator enabled $I_{qn\_1} = I_{Vs} - I_O$	V_S = 13.5 V, I_O < 1 mA, E_n = high		55	80	µA
V_S, V_o	I_{qn_300}	Current consumption with regulator enabled $I_{qn\_300} = I_{Vs} - I_O$	V_S = 13.5 V, I_O = 300 mA, E_n = high		3	4.2	mA
—	T_w	Thermal protection temperature		150		190	°C
—	T_{w_hy}	Thermal protection temperature hysteresis			10		°C

1. Measured output current when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and I_o = 75 mA.

2. V_S - V_o measured dropout when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and I_o = 75 mA.
3. Guaranteed by design

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R_{es}	V_{Res_l}	Reset output low voltage	R_{ext} = 5 kΩ V_o > 1 V			0.4	V
R_{es}	I_{Res_lkg}	Reset output high leakage current	$V_{Res} = V_o$			1	µA
R_{es}	R_{Res}	Pull up internal resistance	Versus V_o	10	20	40	kΩ
R_{es}	V_{o_th}	V_o out of regulation threshold	V_o decreasing	6%	8%	10%	Below V_{o_ref}
V_{cr}	V_{Rlth}	Reset timing low threshold	V_S = 13.5 V	16%	19%	22%	V_{o_ref}
V_{cr}	V_{Rhth}	Reset timing high threshold	V_S =13.5 V	47%	50%	53%	V_{o_ref}
V_{cr}	I_{cr}	Charge current	V_S = 13.5 V	10	20	30	µA
V_{cr}	I_{dr}	Discharge current	V_S = 13.5 V	10	20	30	µA
R_{es}	T_{rr}	Reset reaction time	$V_o = V_{o\_th}$ - 100 mV			2	µs
R_{es}	T_{rd}	Reset delay time	V_S = 13.5 V, C_{tr} = 1 nF	2	4	6	ms

Table 7. Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_n	V_{En_low}	E_n input low voltage				1	V
E_n	V_{En_high}	E_n input high voltage		3			V
E_n	V_{En_hyst}	E_n input hysteresis			500		mV
E_n	$I_{\_leak}$	Pull down current	V_{En} = 5 V		3	10	µA

2.4 Electrical characteristics curves

Figure 3. Output voltage vs T_j

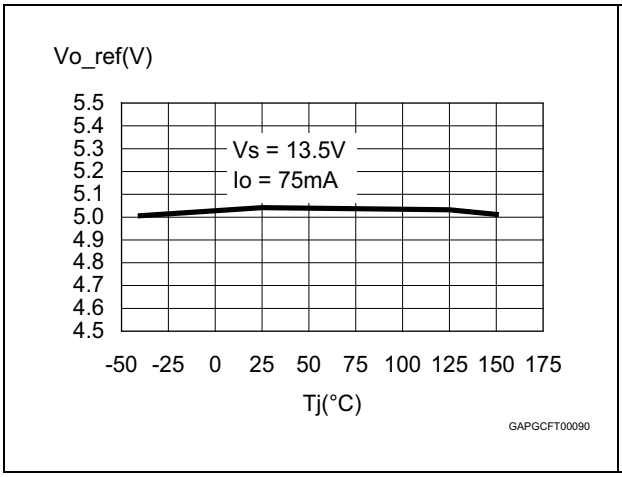


Figure 4. Output voltage vs V_S

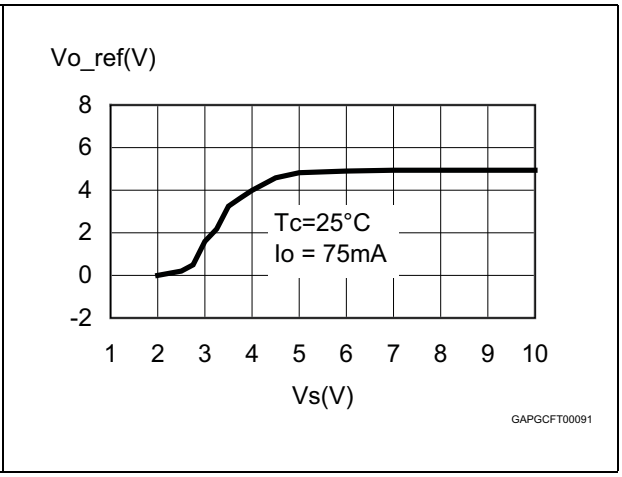


Figure 5. Output voltage vs V_{En}

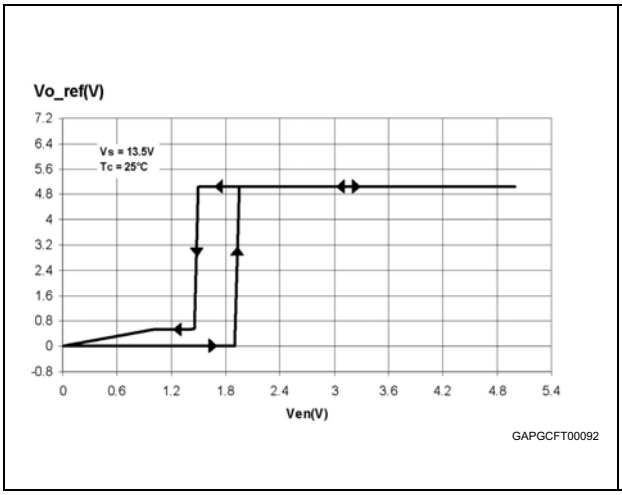


Figure 6. Drop voltage vs output current

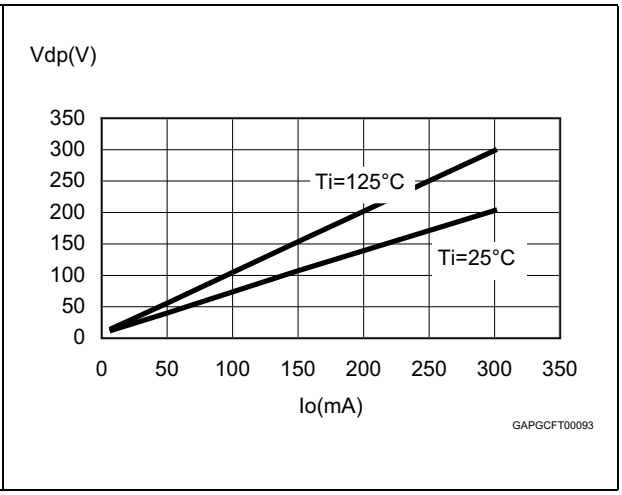


Figure 7. Current consumption vs output current

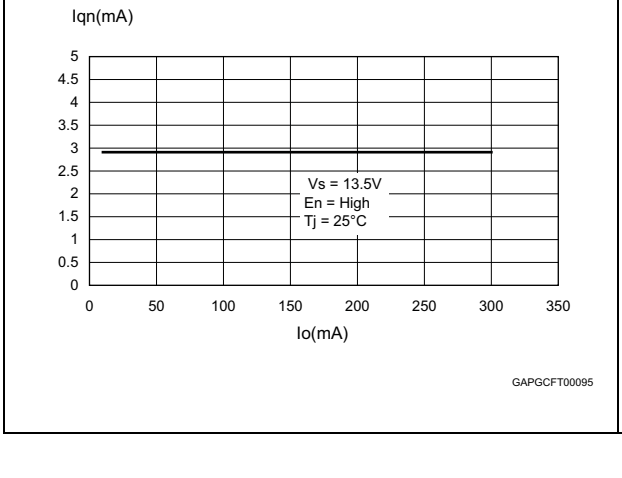


Figure 8. Current consumption vs output current (at light load condition)

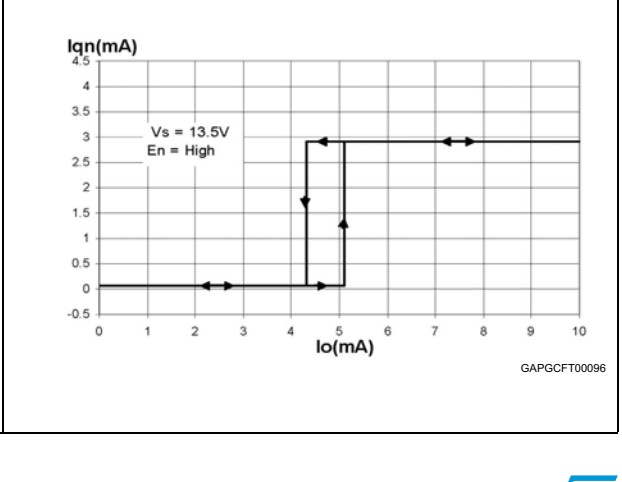


Figure 9. Current consumption vs input voltage (I_O = 0.1 mA)

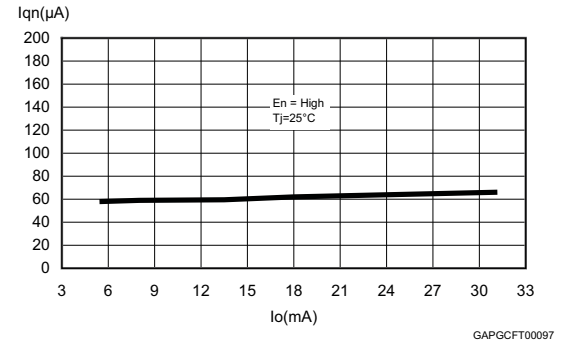


Figure 10. Current consumption vs input voltage (I_O = 100 mA)

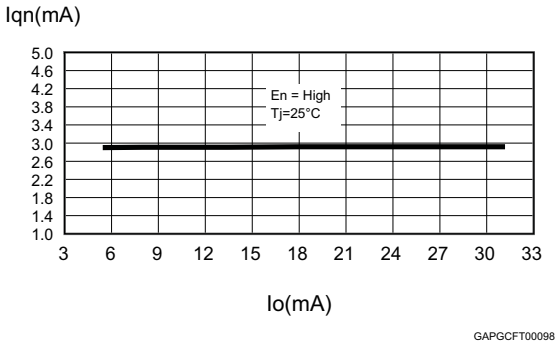


Figure 11. Current limitation vs T_j

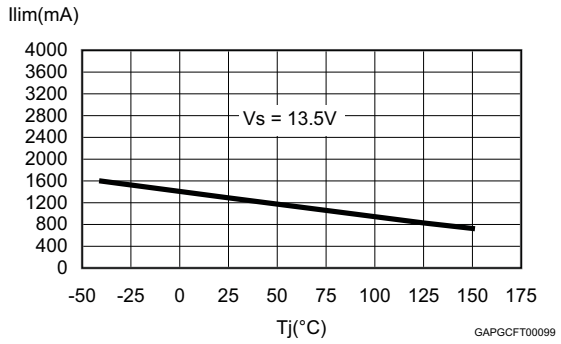


Figure 12. Current limitation vs input voltage

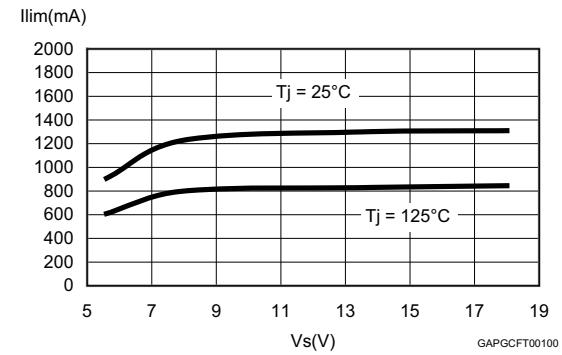


Figure 13. Short-circuit current vs T_j

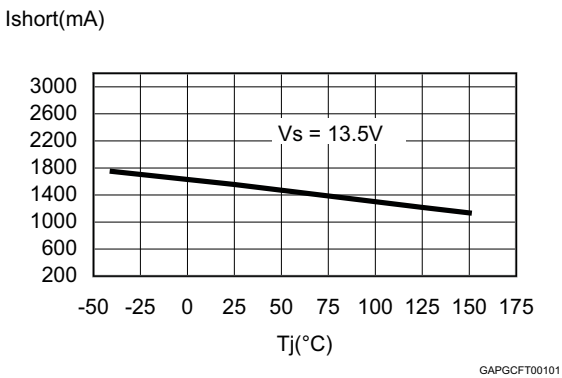


Figure 14. Short-circuit current vs input voltage

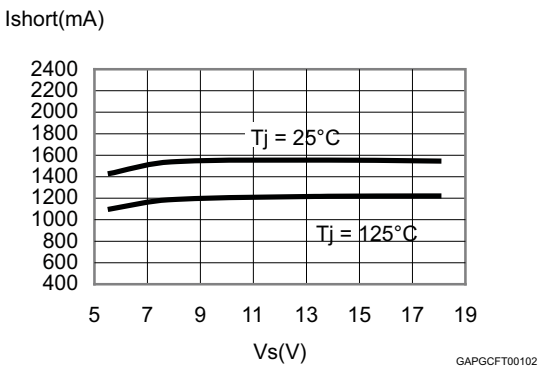


Figure 15. V_{En_high} vs T_j

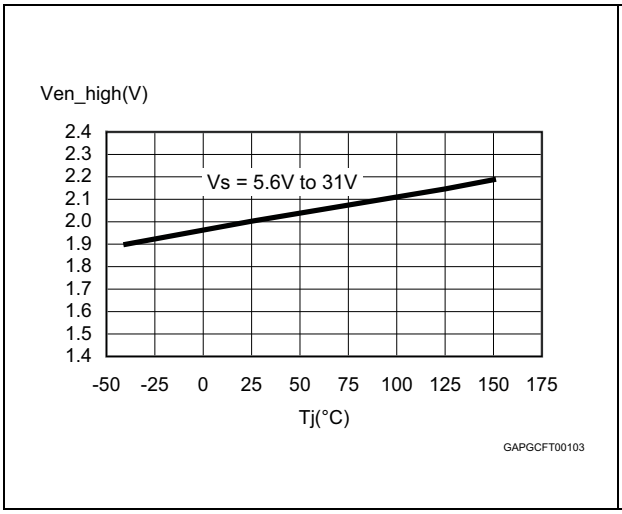


Figure 16. V_{En_low} vs T_j

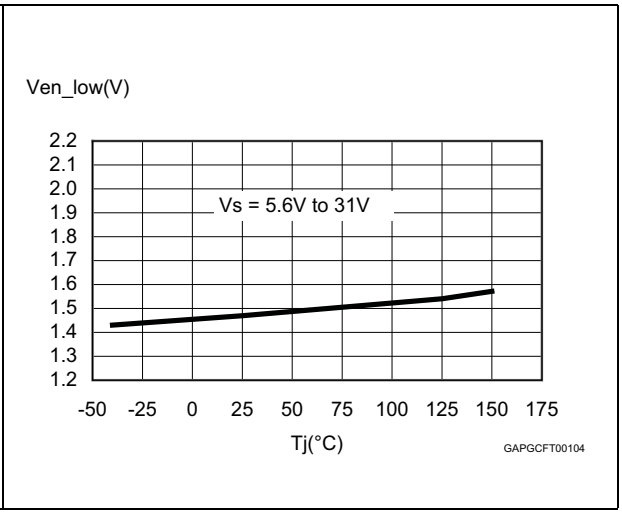


Figure 17. V_{Rhth} vs T_j

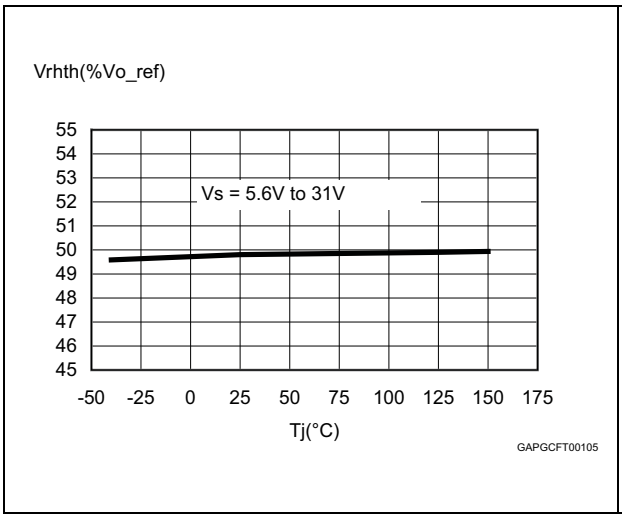


Figure 18. V_{Rlth} vs T_j

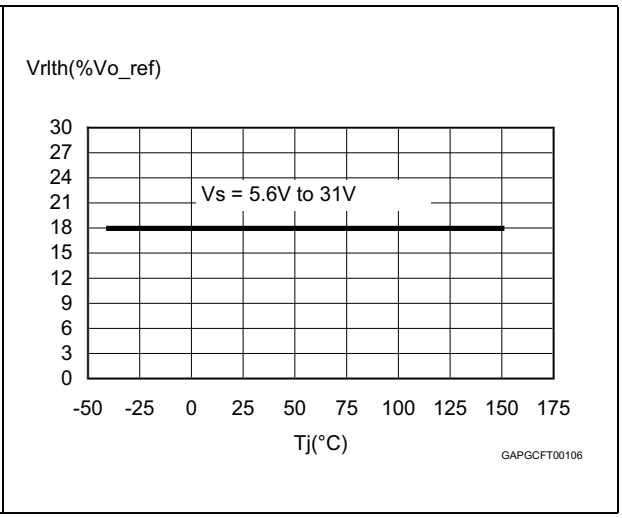


Figure 19. I_{cr} vs T_j

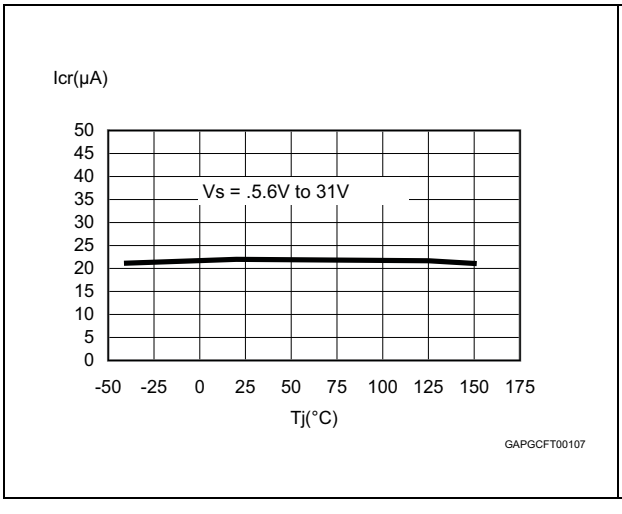
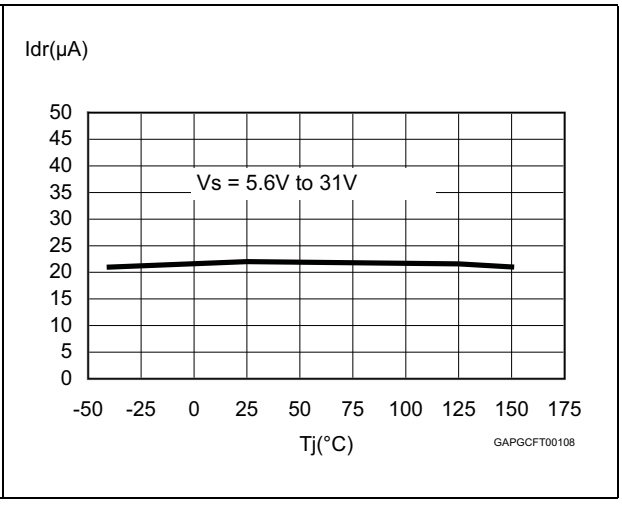


Figure 20. I_{dr} vs T_j

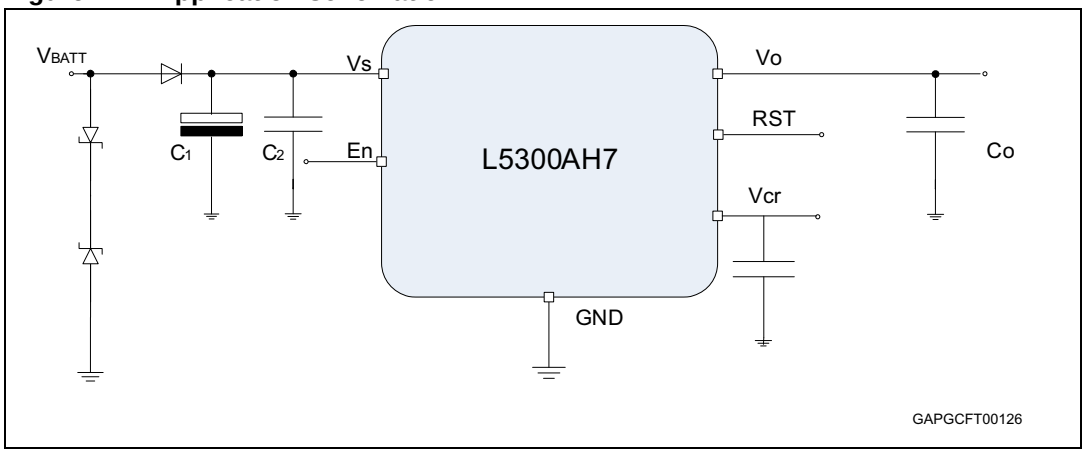


3 Application information

3.1 Voltage regulator

The voltage regulator uses a P-channel MOS transistor as a regulating element. With this structure a very low dropout voltage at current up to 300 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage (2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to 55 µA only (low consumption mode). This procedure features a certain hysteresis on the output current (see *Figure 8*). Short-circuit protection to GND and a thermal shutdown are provided.

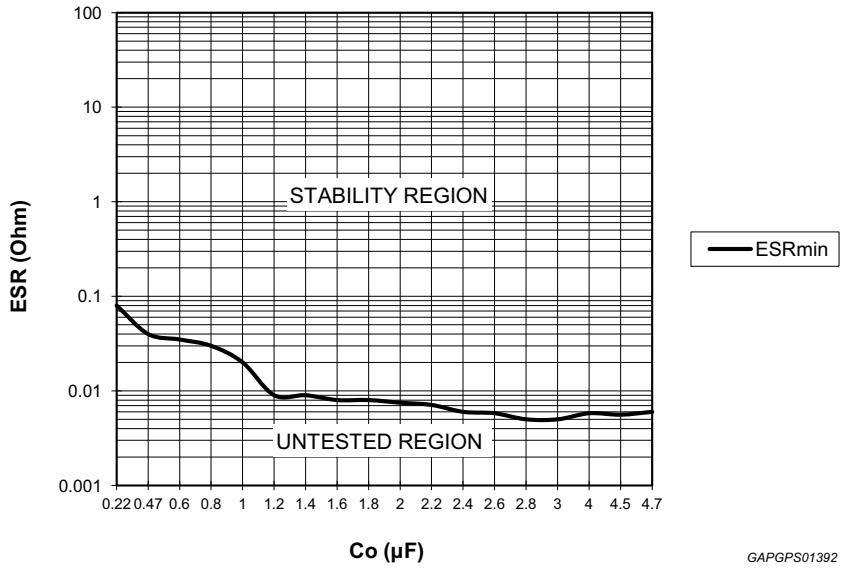
Figure 21. Application schematic



The input capacitor $C_1 \geq 100$ µF is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor $C_2 \geq 220$ nF is needed when the C_1 is too distant from the V_S pin and it compensates smooth line disturbances. The C_0 ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is $C_0 = 220$ nF?with ESR ≥ 100 mΩ.

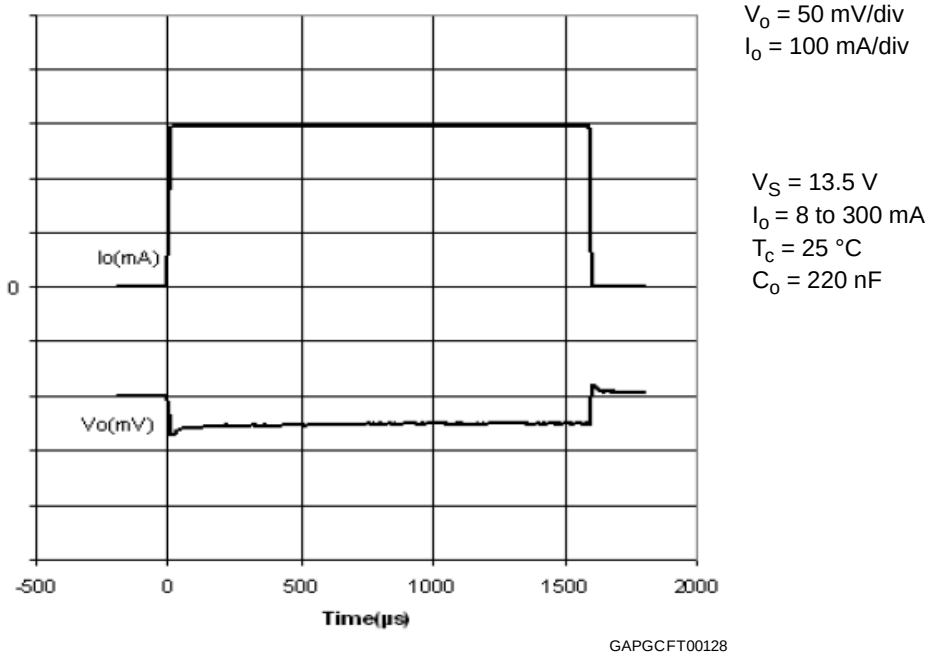
Stability region is reported in *Figure 22*.

Figure 22. Stability region



Note:
The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

Figure 23. Maximum load variation response



3.2 Reset

The reset circuit monitors the output voltage V_o. If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a delay time (t_{rr}). When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay time T_{rd}. This delay is obtained by 512 periods of oscillator. The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth}-V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth}-V_{Rlth}) \times C_{tr}] / I_{dr}$$

and reset pulse delay T_{rd} is given by:

Equation 2

$$t_{rd} = 32 \times T_{osc}$$

Where:

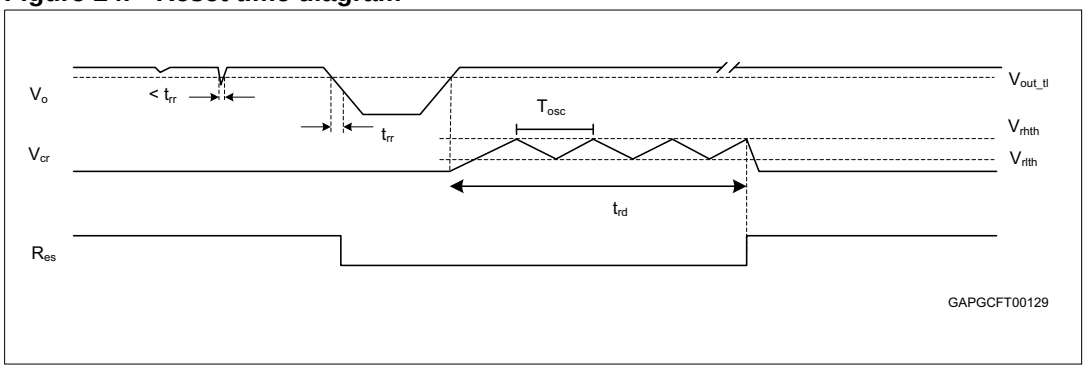
I_{cr} = 20 µA is an internally generated charge current,

I_{dr} = 20 µA is an internally generated discharge current,

V_{Rhth} = 2.5V (typ) and V_{Rlth} = 0.95V (typ) are two voltage thresholds,

C_{tr} is an external capacitor put between V_{cr} pin and GND.

Figure 24. Reset time diagram



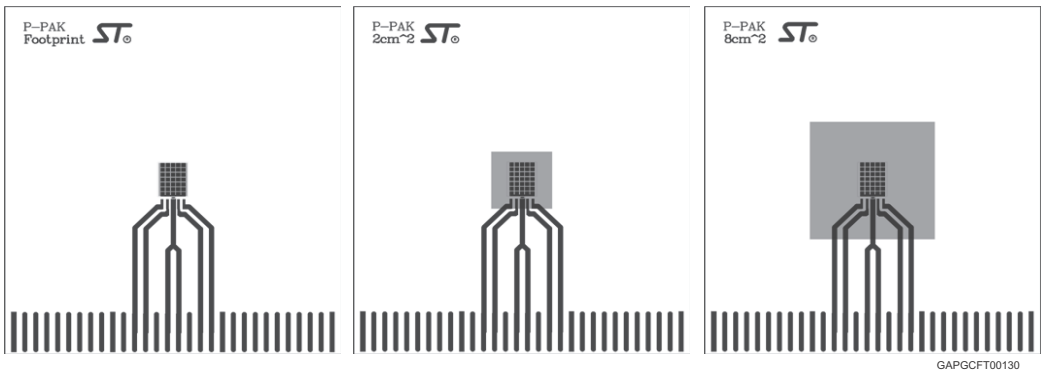
3.3 Enable

L5300AH7 is also provided by an enable input, a high signal switches the regulator ON. In standby mode the output is disabled and the current consumption of the device (quiescent current) is less than 10 µA.

4 Package and PC board thermal data

4.1 HPAK thermal data

Figure 25. PC board



Note:
Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10 %; Board double layer; Board dimension 78 mm x 86 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 6.4 mm x 7 mm).

Figure 26. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

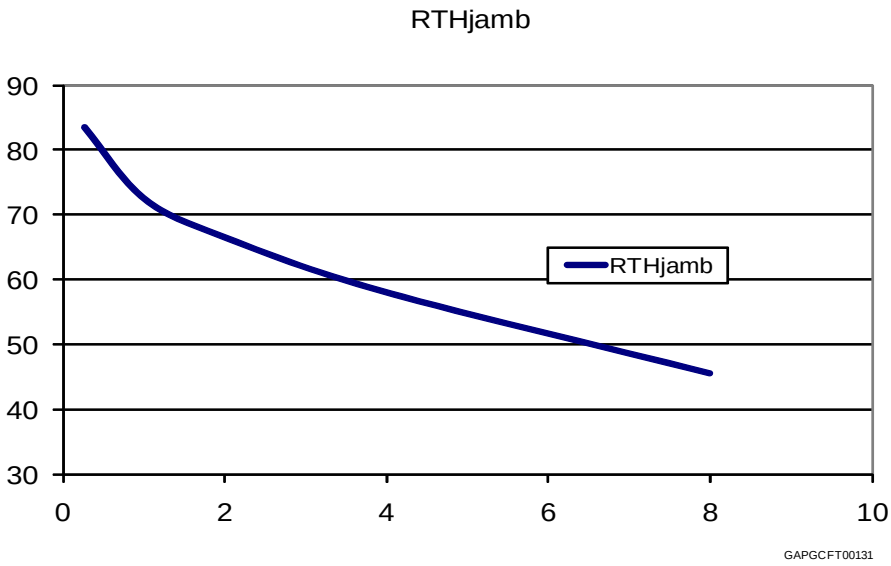


Figure 27. HPAK thermal impedance junction ambient single pulse

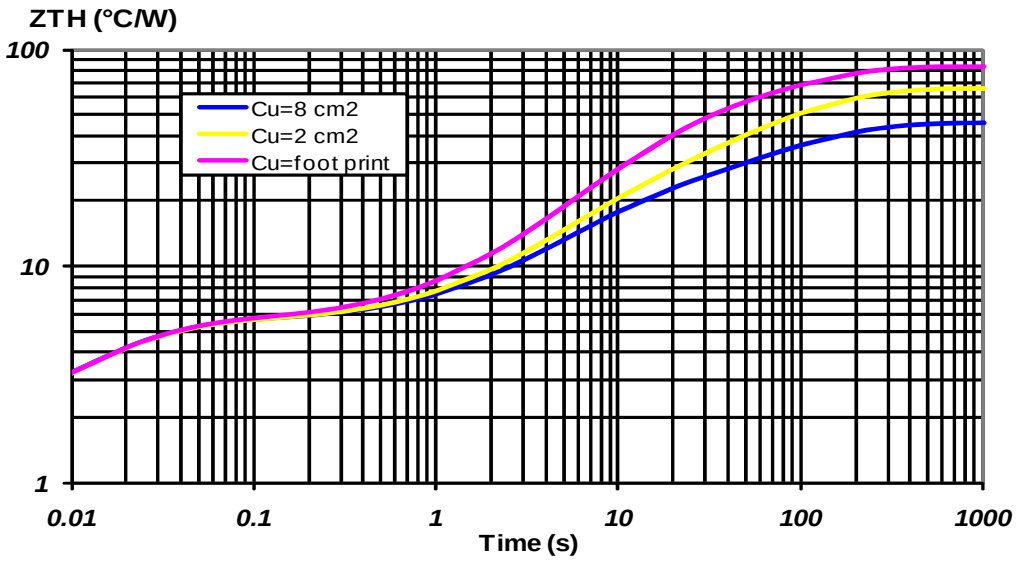
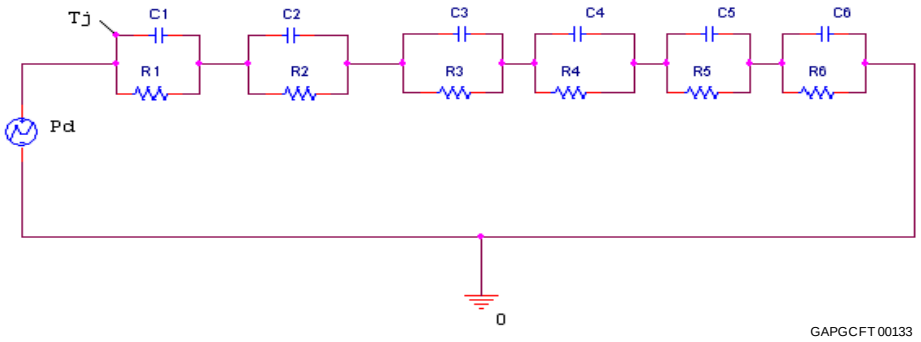


Figure 28. Thermal fitting model of a single-channel HSD in HPAK



Note:
The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Table 8. Thermal parameter

Area/island (cm^2)	Footprint	4	8
R1 (°C/W)	3		
R2 (°C/W)	4		
R3 (°C/W)	6		
R4 (°C/W)	7		
R5 (°C/W)	28	18.5	11
R6 (°C/W)	31	22	14
C1 (W.s/°C)	0.0005		
C2 (W.s/°C)	0.001		
C3 (W.s/°C)	0.005		
C4 (W.s/°C)	0.05		
C5 (W.s/°C)	0.8	2	3
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 HPAK mechanical data

Figure 29. HPAK dimension

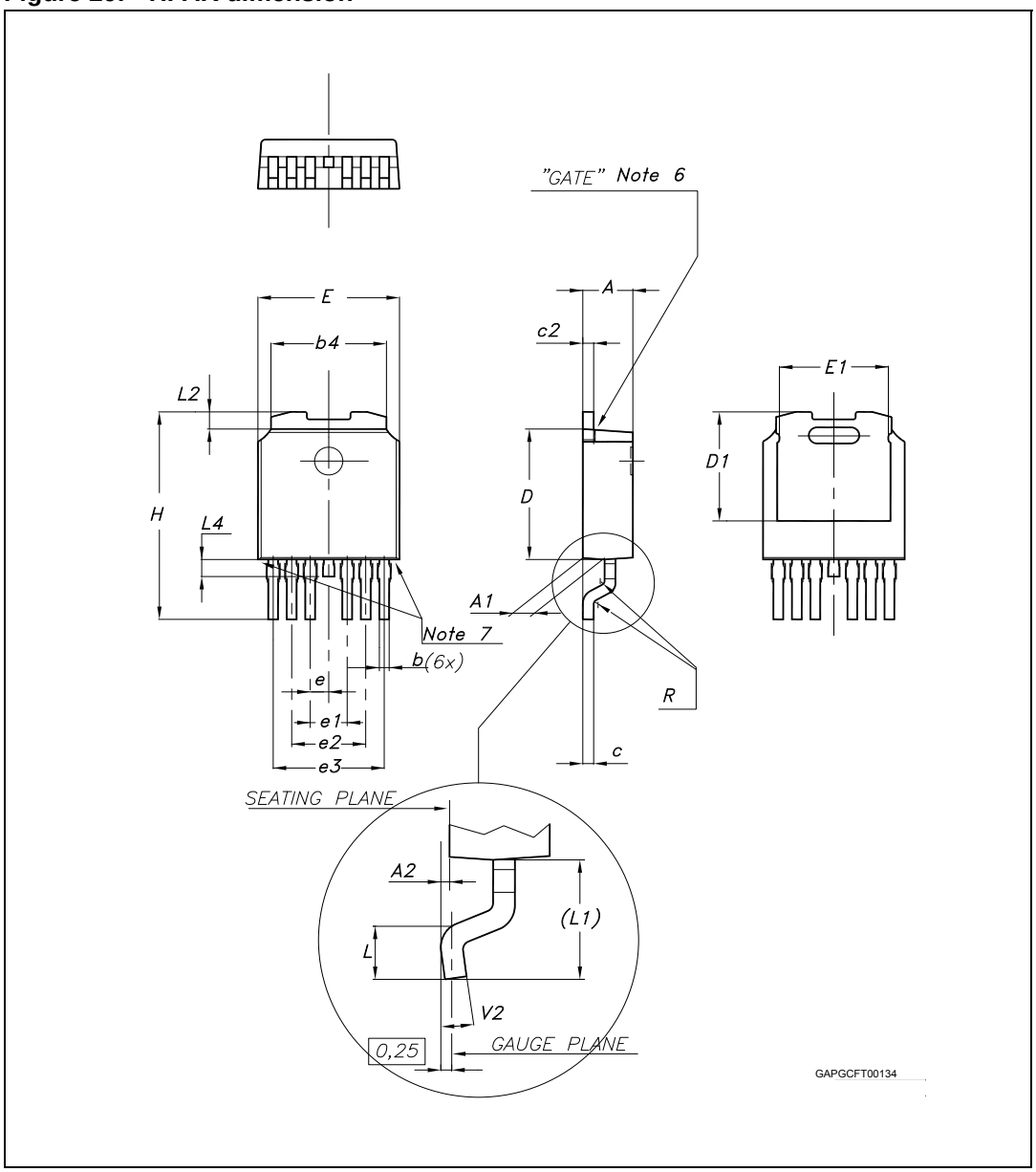


Table 9. HPAK mechanical data

Dim	Millimeter		
	Nom	Min	Max
A		2.20	2.40
A1		0.90	1.10
A1		0.03	0.23
b		0.45	0.60
b4		5.20	5.40
c		0.45	0.60
c2		0.48	0.60
D		6.00	6.20
D1	5.10		
E		6.40	6.60
E1	5.20		
e	0.85		
e1		1.60	1.80
e2		3.30	3.50
e3		5.00	5.20
H		9.35	10.10
L		1	
(L1)	2.80		
L2	0.80		
L4		0.60	1.00
R	0.20		
V2		0°	8°

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Aug-2007	1	Initial release.
15-Oct-2007	2	Changed features table on the cover page: - quiescent current with regulator disabled changed from 10 to 5 µA. - quiescent current with regulator enabled changed from 60 to 55 µA. *Table 5: General* - Added typical value of I_{qs} and I_{qn_1} parameters.
12-Mar-2009	3	Changed features table on the cover page *Table 5: General* – V_{o_ref}: deleted row and added 3 new rows *Table 6: Reset* – I_{Res_lkg}: deleted Test condition – V_{o_th}: deleted I_O = 1 to 300 mA and V_S = 5.6 to 31V, added "V_o decreasing" for test condition – V_{Rlth}: changed min/typ/max values – T_{rd}: changed min/typ/max values Updated *Table 7: Enable* *Section 3.2: Reset* – t_{rd}: changed coefficient – V_{Rlth}: changed coefficient
23-Jul-2010	4	Changed status from target specification to preliminary data. Updated following tables: – *Table 4: Thermal data* – *Table 5: General* Added *Section 2.4: Electrical characteristics curves*. Added *Chapter 4: Package and PC board thermal data*
02-Sep-2010	5	Updated *Figure 27: HPAK thermal impedance junction ambient single pulse*
15-Sep-2010	6	Updated *Table 4: Thermal data*
12-Oct-2010	7	Updated *Section 3.1: Voltage regulator*

Table 10. Document revision history (continued)

Date	Revision	Changes
09-Mar-2011	8	Updated following tables: *Table 2: Pins description*: – Updated pins sequence *Table 3: Absolute maximum ratings*: – I_{sdc}: changed symbol from I_{Vsdc} – I_{odc}: changed symbol from I_{Vodc} *Table 5: General*: – I_{short}: changed min/typ/max value – I_{lim}: changed min/typ/max value, changed parameter – V_{line}: changed test condition – I_{qn_300}: changed typ value – Updated tablefootnote *Table 6: Reset*: – V_{Res_l}: changed test condition – V_{Res_lkg}: added test condition *Table 7: Enable*: – I_{leak}: changed typ value Updated *Section 3.2: Reset*
18-Nov-2011	9	*Table 9: HPAK mechanical data*: – b: updated values
26-Jan-2012	10	Updated *Figure 22: Stability region on page 14*.
07-Feb-2012	11	Modified *Figure 22: Stability region on page 14*.
13-Sep-2013	12	Updated disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com