FEATURES

- **12-Bit SAR ADC**
- **125kSPS sampling rate**
- **Single supply single channel**
- **Low power dissipation 1.9mW**
- **Shutdown feature**
- **Flexible serial interface**
- **Supply voltage of 2.7V to 5.5V**
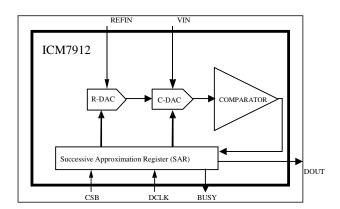- **Temperature range: −40°C to +85°C**
- **8-lead TSSOP**

OVERVIEW

The ICM7912 is a 12-bit 125kSPS through put rate Analog-to-Digital Converter with a unipolar, single-ended input. It has successive approximation register (SAR) architecture and can sample the analog input. It has a flexible serial interface.

APPLICATIONS

- PDA's
- Touch screen monitors
- Hand held devices
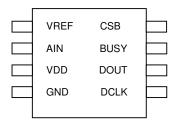- Instrumentation and control systems
- Data Acquisition Systems
- Automotive

BLOCK DIAGRAM

PACKAGE

8-Pin TSSOP

VREF	CSB
AIN	BUSY
VDD	DOUT
GND	DCLK

PIN DESCRIPTION

Pin No	Symbol	Description
1	VREF	Reference input
2	AIN	Analog Input
3	VDD	Power Supply Input. Range is from 2.7V to 5.5V
4	GND	Ground
5	DCLK	External CLK Input
6	DOUT	Serial Data output, clocked out on falling edge of CLK
7	BUSY	BUSY output
8	CSB	Chip Select input Active Low. Initiates conversion and enables serial data.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 6.0	V
I_{IN}	Input Current	+/- 100.0	mA
$V_{IN\_}$	Digital Input Voltage	-0.3 to 6.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 6.0	V
T_{STG}	Storage Temperature	-65 to +150	^{o}C
T_{SOL}	Soldering Temperature	300	^{o}C

Note: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Temperature Range	Package
ICM7912	-40°C to 85°C	8-Pin TSSOP

DC ELECTRICAL CHARACTERISTICS

(VDD= 3.5V, Maximum Sample Rate, REF= 2.5V; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
		DC PERFORMANCE				
N	Resolution	(Note 1)		12		Bits
No Missing Codes		(Note 1)		12		Bits
INL	Integral Nonlinearity	(Note 1)			0.25	% of FSR
GE	Gain Error	(Note 1)			1	% of FS
OE	Offset Error	(Note 1)			30	mV
		POWER REQUIREMENTS				
VDD	Supply Voltage	(Note 2)	2.7		5.5	V
I_{VDD}	Supply Current	(Note 1)		600		µA
$I_{SHTDOWN}$	Supply Current	(Note 1)		40		µA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
		LOGICINPUT/OUTPUT CHARACTERISTICS (VDD = 2.5V)				
VIH			2.4			V
VIL					0.4	V
VOH	IOH = 50 µA	(Note 1)	2.4			V
VOL	IOL = 50 µA	(Note 1)			0.4	V
		SWITCHING SPECIFICATIONS (CLK INPUT)				
Fsample	Maximum Conversion Rate	(Note 2)			125	kSPS
	Minimum Conversion Rate	(Note 2)	0.5			kSPS
TCLK	CLK Period	(Note 2)	500			ns
	Pulse-width High	(Note 2)	250			ns
	Pulse-width Low	(Note 2)	250			ns
T_{Delay}	Data out Delay	(Note 2)		5		ns
	Wake-up Time	(Note 2)		20		ms
		REFERENCE				
R_{IN}	Reference Input Resistance	(Note 1)		32		kΩ
	Reference Input Span				VDD	V
I_{REF}	Reference Input Current			80		µA

Note 1:   100 % Production Tested at 25 C; guaranteed by design and characterization testing for temperature range.
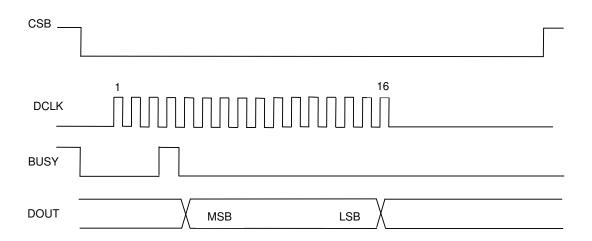Note 2:   Guaranteed by design& characterization testing.
Note 3:   See Applications Information.
Note 4:   12 Monotonicity only guaranteed at REFIN MAX of VDD-1. Reference Input can swing to a higher value till VDD, with some degradation in DC performance and monotonicity could degrade to only 11 bits at high reference input.

ICmic™
IC MICROSYSTEMS

TIMING DIAGRAM

DETAILED DESCRIPTION

The ICM7912 is a SAR architecture 12-Bit ADC. It operates on a 2.7V to 5.5V single supply and consumes about 600µA supply current when operating on a 2MHz external clock. The output throughput rate is a maximum of 125 kSPS when the DCLK is running at at the maximum frequency of 2MHz.

The ADC is composed of a high performance capacitive DAC and a comparator along with SAR control logic and resistor string segment. The reference input drives the resistor string directly and has an input resistance of around 32 kΩ.

The ICM7912 comes complete with a high performance CMOS sample and hold amplifier made up by the capacitive DAC.

There is shutdown capability which is active between conversions when CSB is high. The converter will shut down to under 40 µA of supply current.

APPLICATIONS INFORMATION

The IC7912 has a single ended analog input which can swing from GND to VDD. The reference input has a range from GND to VDD and can be tied to VDD for largest input range.

The ICM7912uses the DCLK as the external clock and this controls all the transfer of information to and from the ADC.

One complete conversion cycle of the ICM7912 will take 16 clock cycles. As CSB is pulled low the ADC powers up and initiates a sampling/conversion cycle. Data is clocked out MSB first on the falling edge of the DCLK input. The analog input is sampled on the first three clock pulses and then conversion process begins. The DOUT is available from the falling edge of the 4th DCLK pulse MSB first and the LSB is available on the falling edge of the 15th DCLK pulse. Since there is some propagation delay the DOUT should be sampled on the rising edge of the following clock pulse. So this implies the MSB can be safely sampled on the 5th DCLK rising edge and the LSB can be sampled on the 16th DCLK rising edge.

PACKAGE INFORMATION

8 LEAD TSSOP STANDARD PACKAGE

173 MIL TSSOP
Thin Shrink Small Outline Package (TSSOP)

PACKAGE INFORMATION

NOTES

1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE
   OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES
   AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. ALL DIMENSIONS ARE GIVEN IN INCHES.
5. LEAD COPLANARITY IS 0.003 INCH MAX.

JEDEC#	MO−153AA	
TYPE	08 LEAD	
SYMBOL	Min	Max
A	0.034	0.047
A1	0.002	0.006
B	0.007	0.012
C	0.004	0.008
D	0.114	0.122
E	0.169	0.177
e	0.0256 BSC	
H	0.252 BSC	
L	0.020	0.030
α°	0°	8°