



### DMN2005LP4K

#### N-CHANNEL ENHANCEMENT MODE MOSFET

### **Features**

- Low On-Resistance
- Very Low Gate Threshold Voltage, 0.9V Max.
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- ESD Protected Gate
- Ultra Low Profile Package
- Qualified to AEC-Q101 Standards for High Reliability

### **Mechanical Data**

- Case: X2-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 (A)
- Weight: 0.001 grams

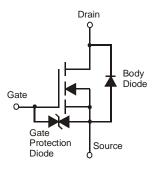




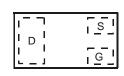


X2-DFN1006-3

Bottom View



**Equivalent Circuit** 



Top View Pin-Out

# **Ordering Information** (Note 4)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMN2005LP4K-7	DN	7	8	3000
DMN2005LP4K-7B	DN	7	8	10,000

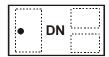
#### Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and
- 3. Halogen- and Antimony-tree "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com.

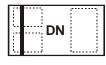
# **Marking Information**

DMN2005LP4K-7



Top View Dot Denotes Drain Side

DMN2005LP4K-7B



Top View Bar Denotes Gate and Source Side

DN = Product Type Marking Code



## **Maximum Ratings** (@T<sub>A</sub> = 25°C unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage		$V_{DSS}$	20	V
Gate-Source Voltage		$V_{GSS}$	±10	V
Drain Current per element (Note 5)	Continuous Pulsed (Note 6)	I <sub>D</sub>	300 350	mA

### **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	400	mW
Thermal Resistance, Junction to Ambient	$R_{ hetaJA}$	280	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to +150	°C

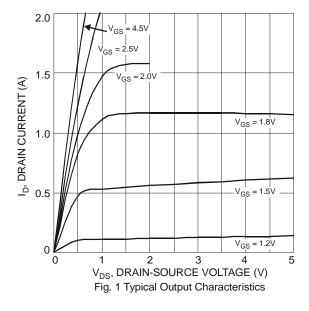
## **Electrical Characteristics** (@T<sub>A</sub> = 25°C unless otherwise specified.)

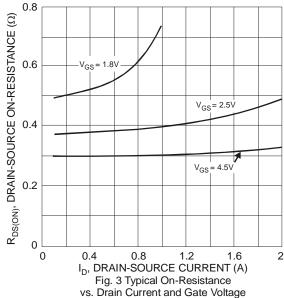
Characteristic		Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (per element) (Note 7)								
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	20	_	_	V	$V_{GS} = 0V, I_D = 100\mu A$	
Zero Gate Voltage Drain Current		I <sub>DSS</sub>	_	_	10	μΑ	$V_{DS} = 17V$ , $V_{GS} = 0V$	
Gate-Source Leakage		I <sub>GSS</sub>	_	_	±5	μΑ	$V_{GS} = \pm 8V, V_{DS} = 0V$	
ON CHARACTERISTICS (per element	ON CHARACTERISTICS (per element) (Note 7)							
Gate Threshold Voltage		V <sub>GS(th)</sub>	0.53		0.9	V	$V_{DS} = V_{GS}$ , $I_D = 100\mu A$	
Static Drain-Source On-Resistance		R <sub>DS</sub> (ON)		0.35 0.4 0.45 0.55 0.65	1.5 1.7 1.7 3.5 3.5	Ω	$\begin{split} &V_{GS} = 4V,  I_D = 10 \text{mA} \\ &V_{GS} = 2.7V,  I_D = 200 \text{mA} \\ &V_{GS} = 2.5V,  I_D = 10 \text{mA} \\ &V_{GS} = 1.8V,  I_D = 200 \text{mA} \\ &V_{GS} = 1.5V,  I_D = 1 \text{mA} \end{split}$	
Forward Transfer Admittance		Y <sub>fs</sub>	40	_	_	mS	$V_{DS} = 3V, I_{D} = 10mA$	
DYNAMIC CHARACTERISTICS								
Input Capacitance		C <sub>iss</sub>	_	37.1	—	pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V f = 1.0MHz	
Output Capacitance		Coss	_	6.5	_	pF		
Reverse Transfer Capacitance		C <sub>rss</sub>	_	4.8	_	pF	I = 1.0ivii iz	
Switching Time	Turn-on Time	t <sub>on</sub>	_	4.06	_	nS	$V_{DD} = 10V$ , $R_I = 47\Omega$ , $V_{GEN} = 4.5V$ ,	
gg	Turn-off Time	t <sub>off</sub>	_	13.7			$R_{GEN} = 10\Omega$ .	

Notes: 5. Device mounted on FR-4 PCB.

6. Pulse width ≤10μS, Duty Cycle ≤1%.
7. Short duration pulse test used to minimize self-heating effect.







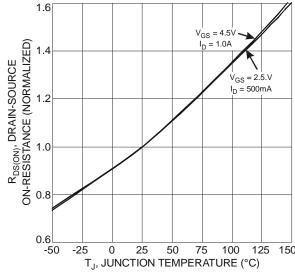
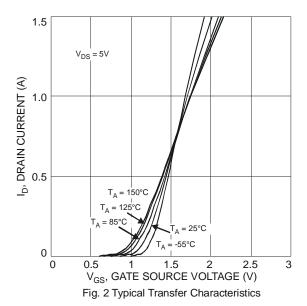


Fig. 5 On-Resistance Variation with Temperature



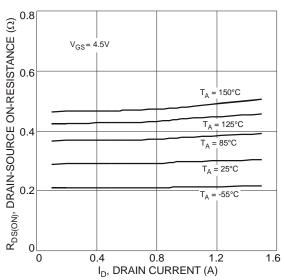


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

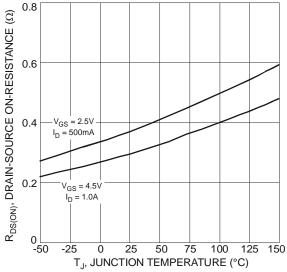


Fig. 6 On-Resistance Variation with Temperature



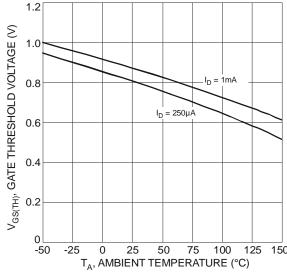
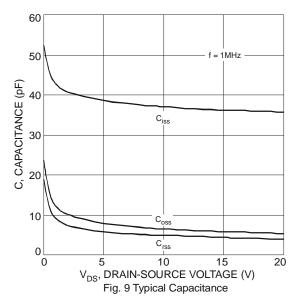
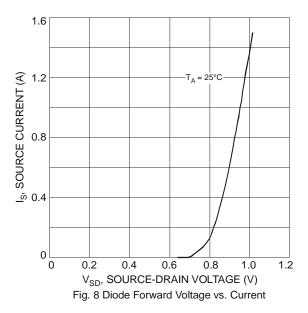


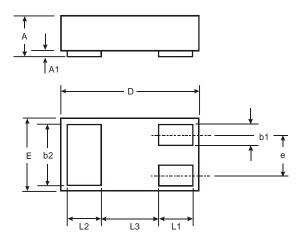
Fig. 7 Gate Threshold Variation vs. Ambient Temperature





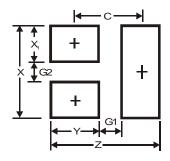


# **Package Outline Dimensions**



X2-DFN1006-3					
Dim	Min	Max	Тур		
Α		0.40			
A1	0	0.05	0.03		
b1	0.10	0.20	0.15		
b2	0.45	0.55	0.50		
D	0.95	1.05	1.00		
Е	0.55	0.65	0.60		
е			0.35		
L1	0.20	0.30	0.25		
L2	0.20	0.30	0.25		
L3	_	_	0.40		
All Dimensions in mm					

# **Suggested Pad Layout**



Dimensions	Value (in mm)
Z	1.1
G1	0.3
G2	0.2
Х	0.7
X1	0.25
Y	0.4
С	0.7



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