Dual Synchronous Buck PWM Controllers

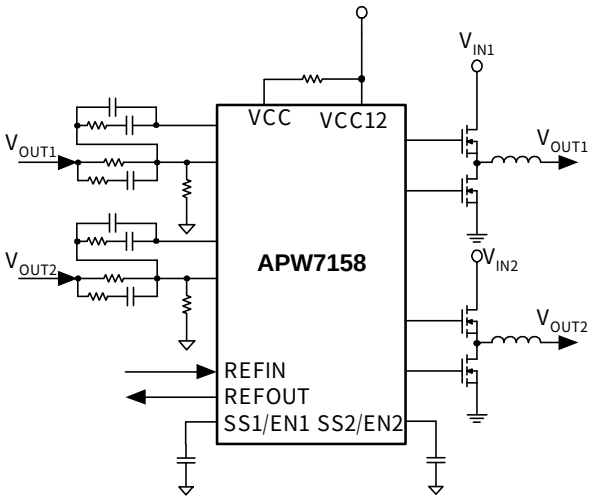
Features

- Two Synchronous Buck Converters(OUT1,OUT2)
- Converter Input Voltage Range up to 12V
- 0.6V Reference for OUT1 with 0.8% Accuracy
- 3.3V Reference for OUT2 with 0.8% Accuracy
- Both Outputs have Independent Soft-Start and Enable Functions
- Internal 300kHz Oscillator and Programmable Frequency Range from 70 kHz to 800kHz
- 180 Degrees Phase Shift etween OUT1 and OUT2
- Short-Circuit Protection
- Thermally Enhanced SOP-20 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Graphic Cards
- Low-Voltage Distributed Power Supplies
- SMPS Application

Simplified Application Circuit



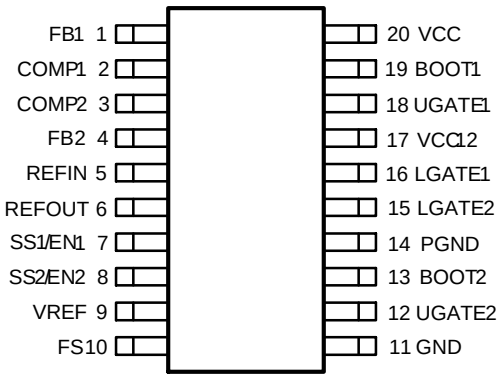
General Description

The APW7158 has two synchronous buck PWM controllers with high precision internal references voltage to offer accurate outputs. The PWM controllers are designed to drive two N-channel MOSFETs in synchronous buck topology. The device requires 12V and 5V power supplies. If the 5V supply is not available, the device can offer an optional shunt regulator 5.8V for 5V supply.

Both outputs have independent soft-start and enable functions combined on the SS/EN pin. Connecting a capacitor from each SS/EN pin to the ground for setting the soft-start time, and pulling the SS/EN pin voltage below 1V to disable regulator. The device also offers 180° phase shift function between OUT1 and OUT2.

The default switching frequency is 300kHz (keep the FS pin open or short to GND), and the device also provides the programmable switching frequency function to adjust the switching frequency from 70kHz to 800kHz. Connecting a resistor from FS pin to GND increases the switching frequency. Conversely, connecting a resistor from FS pin to VCC12 decreases the switching frequency. There is no current sensing or under-voltage sensing on the APW7158. However, it provides a simple short-circuit protection by monitoring the COMP1 pin and COMP2 pin for over-voltage. When any of two pins exceed their trip point and the condition keeps for 1-2 internal clock cycles (3-6us at 300kHz), all regulators are latched off.

Pin Configuration



Ordering and Marking Information

APW7158 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-20 Operating Ambient Temperature Range E : -20 to 70 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7158 K: 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC12}	VCC12 to GND Voltage	-0.3 to 20	V
V_{CC}, Separate Supply	VCC, Separate Supply to GND Voltage	-0.3 to 5.5	V
V_{UGATE1}, V_{UGATE2}, V_{BOOT1}, V_{BOOT2}	UGATE1, UGATE2, BOOT1, BOOT2 to PGND Voltage	-0.3 to 30	V
V_{LGATE1}, V_{LGATE2}	LGATE1, LGATE2 to GND Voltage	-0.3 to 20	V
V_{FS}	FS to GND Voltage	-0.3 to 20	V
V_{REFIN}, V_{REFOUT}, V_{REF}	REFIN, REFOUT, VREF to GND Voltage	-0.3 to V_{CC}	V
V_{FB1}, V_{COMP1}, V_{FB2}, V_{COMP2}	FB1, COMP1, FB2, COMP2 to GND Voltage	-0.3 to V_{CC}	V
$V_{SS1/EN1}$, $V_{SS2/EN2}$	SS1/EN1, SS2/EN2, to GND Voltage	-0.3 to V_{CC}	V
	PGND to GND Voltage	-0.3 to +0.3	V
T_A	Operating Temperature Range	-20 to +70	°C
T_J	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOP-20	75	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3) SOP-20	20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
Note 3: The case temperature is measured at the center of the exposed pad on the underside of the SOP-20 package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CC12}	VCC12 Supply Voltage	10.8 to 13.2	V
V_{CC}	VCC Supply Voltage	4.5 to 5.5	V
V_{IN}	Converter Input Voltage	2.2 to 13.2	V
V_{OUT}	Converter Output Voltage	0.6 to 5	V
I_{OUT}	Converter Output Current	0 to 20	A
T_A	Ambient Temperature Range	-20 to 70	°C
T_J	Junction Temperature Range	-20 to 125	°C

Note 4: Refer to the typical application circuit

Electrical Characteristics

Operating Conditions: V_{CC} = 5V, V_{CC12} = 12V, T_A = -20 to 70°C. Typical values are at T_A =25°C. Unless Otherwise Specified.

Symbol	Parameter	Test Conditions	APW7158			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY POWER						
I_{VCC}	VCC Input Supply Current	OUT1 and OUT2 disabled	-	4	-	mA
		UGATEs, LGATEs C_L = 1nF, 300kHz	-	7	-	mA
I_{VCC12}	VCC12 Input Supply Current	OUT1 and OUT2 disabled	-	6	-	mA
		UGATEs, LGATEs C_L = 1nF, 300kHz	-	50	-	mA
	Shunt Regulator Output Voltage	20mA current; Equivalent to 300Ω resistor from VCC to VCC12	5.6	5.8	6.0	V
	Maximum Shunt Regulator Current		-	-	60	mA
	Power-On-Reset Threshold Voltage	V_{CC} Rising	4.15	4.23	4.4	V
		V_{CC} Falling	3.9	4.0	4.15	V
		V_{CC12} Rising	7.55	7.8	8	V
		V_{CC12} Falling	7.1	7.3	7.55	V
SYSTEM ACCURACY						
	OUT1 Reference Voltage		-	0.6	-	V
	OUT1 System Accuracy		-0.8	-	0.8	%
OSCILLATOR						
	Oscillator Accuracy		-20	-	20	%
F_S	Oscillator Frequency	FS pin is open	240	300	360	kHz
	Oscillator Adjustment Range	FS pin: resistor to GND; resistor to VCC12	70	-	800	kHz
	Oscillator Sawtooth Amplitude		-	2.1	-	V
	Oscillator Duty-Cycle Range		0	-	85	%
ERROR AMPLIFIER (OUT1 AND OUT2)						
	Open-Loop Gain	R_L = 10kΩ to ground	-	85	-	dB
	Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground	-	15	-	MHz
	Slew Rate	C_L = 100pF, R_L = 10kΩ to ground	-	4	-	V/μS
	ERROR AMPLIFIER Offset Voltage	COMP1/2 to FB1/2; compare to internal VREF/REFIN	-	2	-	mV

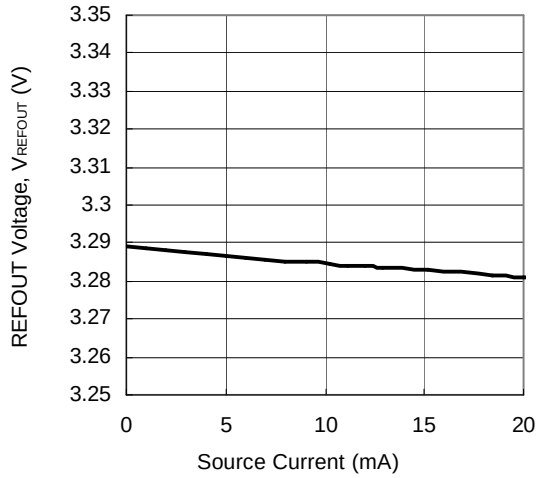
Electrical Characteristics (Cont.)

Operating Conditions: V_{CC} = 5V, V_{CC12} = 12V, T_A = -20 to 70°C. Typical values are at T_A =25°C. Unless Otherwise Specified.

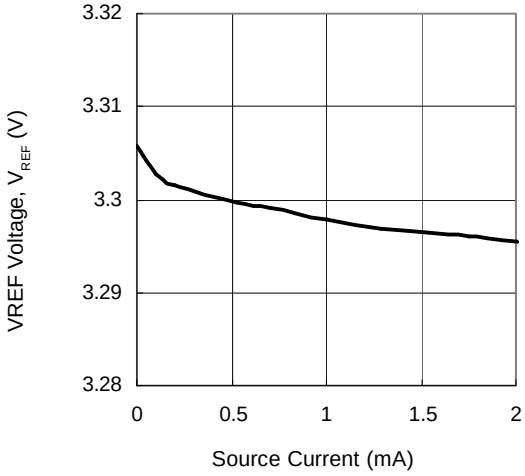
Symbol	Parameter	Test Conditions	APW7158			Unit
			Min.	Typ.	Max.	
ERROR AMPLIFIER (OUT1 AND OUT2) (CONT.)						
	Maximum COMP High Voltage	COMP1/2, R_L = 10kΩ to ground; (may trip short-circuit)	-	V_{CC}	-	V
	COMP Source Current	COMP1/2, V_{COMP}=2V	-	-50	-	mA
	COMP Sink Current	COMP1/2, V_{COMP}=2V	-	45	-	mA
PROTECTION AND MONITOR						
	Short-Circuit Protection Threshold	V_{COMP1} and V_{COMP2} rising	-	3.3	-	V
	Short-Circuit Protection Filter Time	Based on internal oscillator clock frequency (nominal 300kHz = 3.3µs clock period)	1	-	2	Clock pulses
VREF						
V_{REF}	VREF Output Voltage		-	3.3	-	V
	VREF Output Accuracy		-0.8	-	0.8	%
	VREF Source Current		-	-	2.0	mA
REFOUT						
V_{REFOUT}	REFOUT Output Voltage	Determined by REFIN voltage	0.6	-	3.3	V
	REFOUT Offset Voltage		-10	-	10	mV
	REFOUT Source Current		-	-	20	mA
	REFOUT Sink Current		-	-	0.48	mA
	REFOUT Output Capacitance		0.4	0.1	2.2	µF
ENABLE/SOFT-START (SS/EN 1,2)						
	Enable Threshold Voltage	High level input voltage	2	-	-	V
		Low level input voltage	-	-	0.4	
	SS/EN Pin Soft-Start Current		-	-30	-	µA
	Soft-Start High Voltage	End of ramp	-	3.5	-	V
GATE DRIVERS						
	OUT1 GATE Driver Source	V_{UGATE1}, V_{LGATE1}=3V, V_{BOOT}=12V	-	1.8	-	A
	OUT2 GATE Driver Source	V_{UGATE2}, V_{LGATE2}=3V, V_{BOOT}=12V	-	1	-	A
	OUT1 GATE Driver Sink	V_{UGATE1}, V_{LGATE1}=3V, V_{CC12}=12V	-	2.5	-	Ω
	OUT2 GATE Driver Sink	V_{UGATE2}, V_{LGATE2}=3V, V_{CC12}=12V	-	4	-	Ω

Typical Operating Characteristics

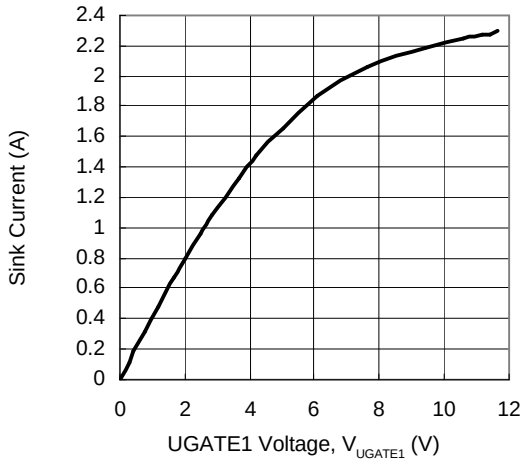
REFOUT Voltage vs. Source Current



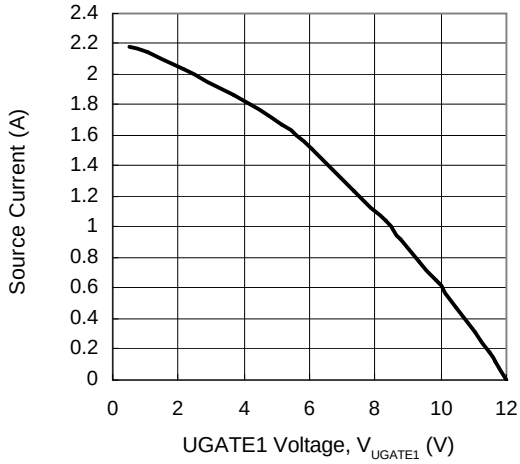
VREF Voltage vs. Source Current



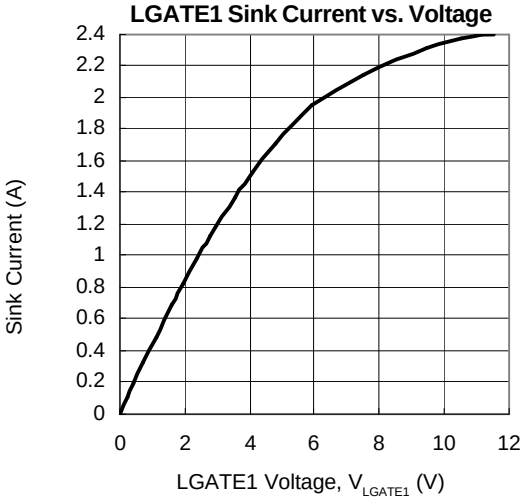
UGATE1 Sink Current vs. Voltage



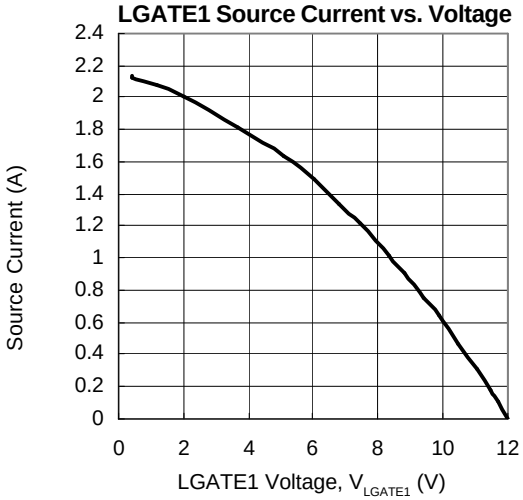
UGATE1 Source Current vs. Voltage



LGATE1 Sink Current vs. Voltage

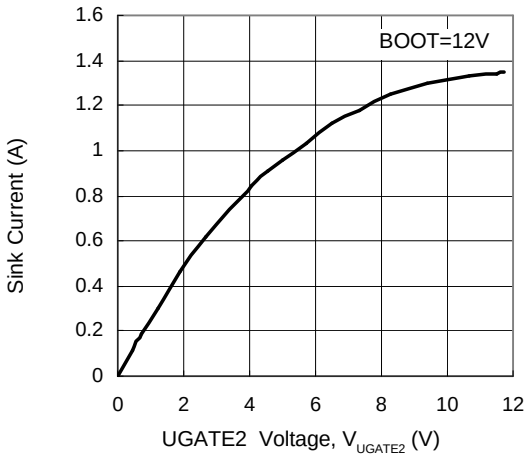


LGATE1 Source Current vs. Voltage

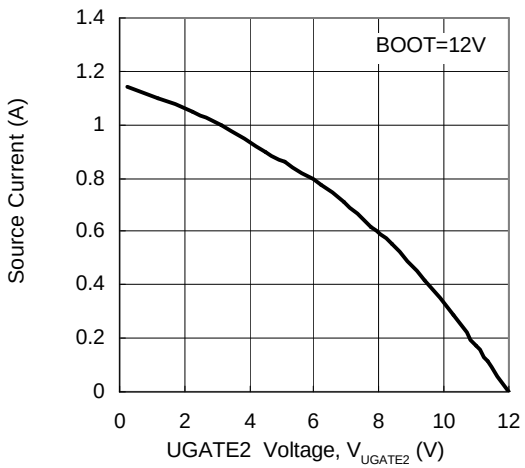


Typical Operating Characteristics (Cont.)

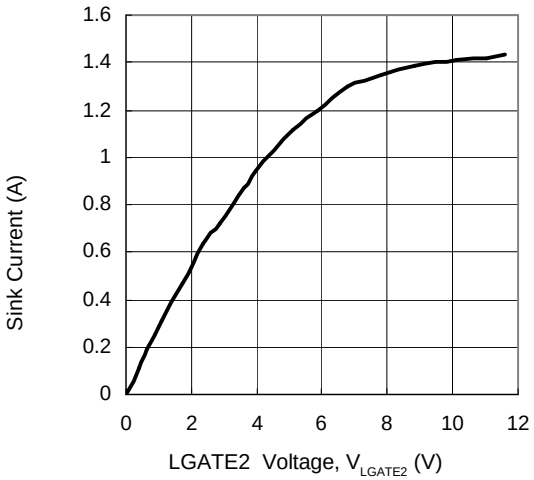
UGATE2 Sink Current vs. Voltage



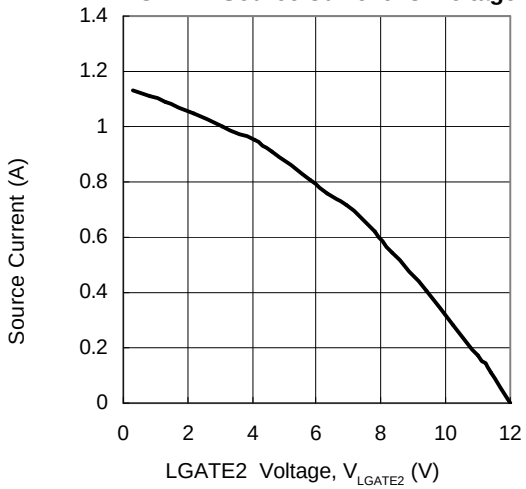
UGATE2 Source Current vs. Voltage



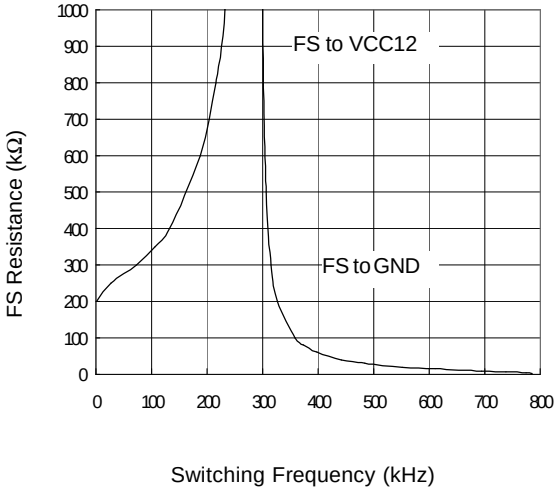
LGATE2 Sink Current vs. Voltage



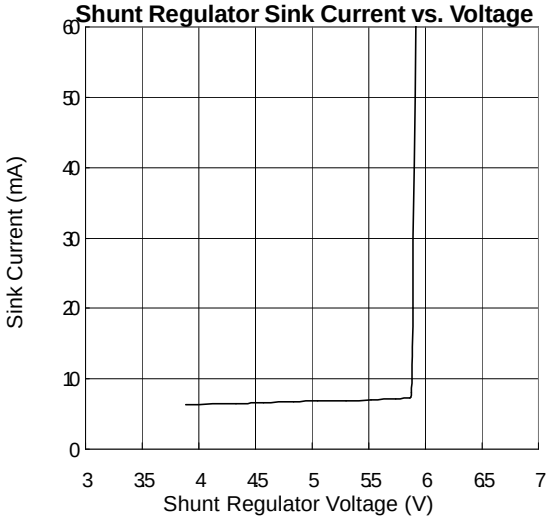
LGATE2 Source Current vs. Voltage



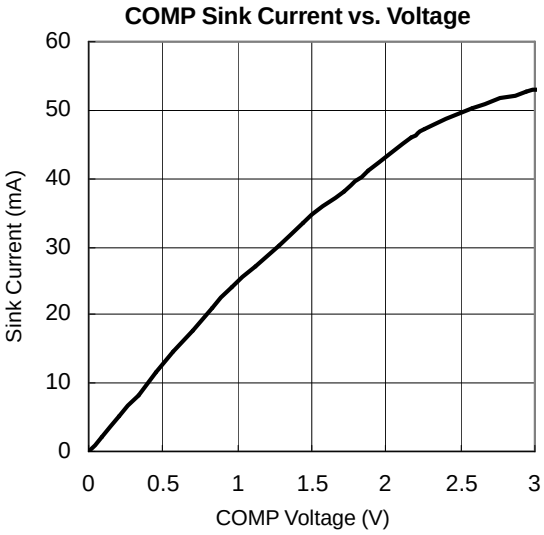
FS Resistance vs. Switching Frequency

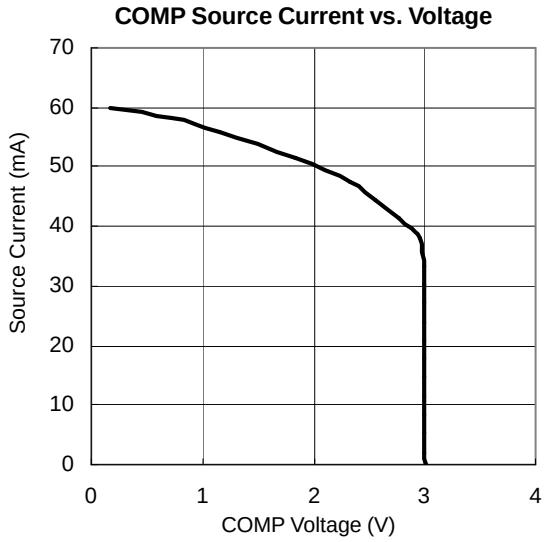


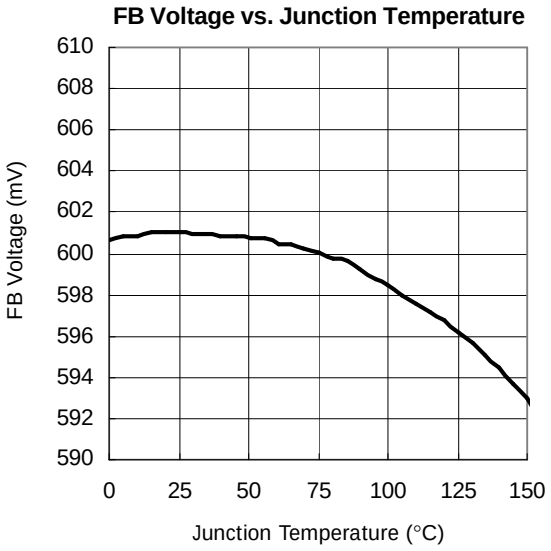
Shunt Regulator Sink Current vs. Voltage

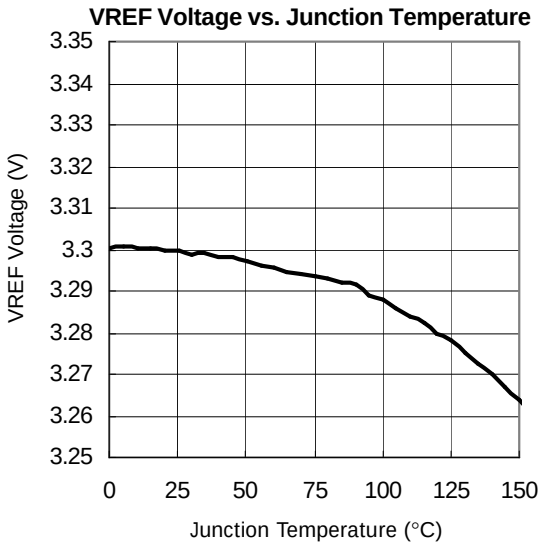


Typical Operating Characteristics (Cont.)





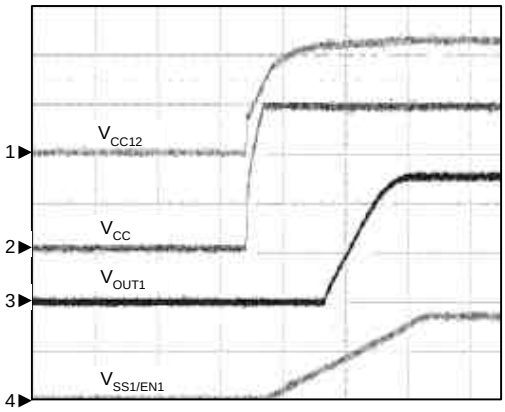




Operating Waveforms

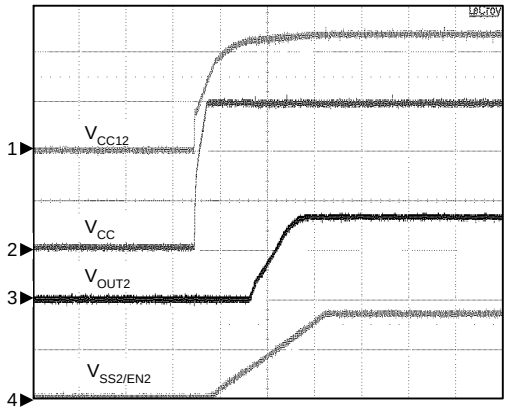
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

OUT1 Power On



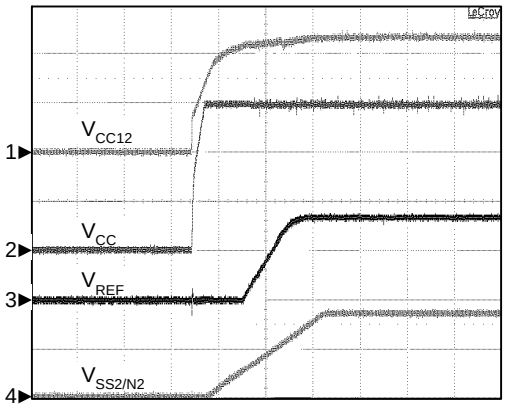
CH1: V_{CC12}, 5V/Div, DC
CH2: V_{CC}, 2V/Div, DC
CH3: V_{OUT1}, 2V/Div, DC
CH4: $V_{SS1/EN1}$, 2V/Div, DC
TIME: 5ms/Div

OUT2 Power On



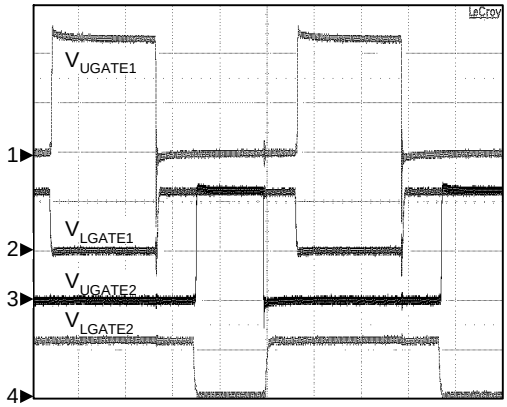
CH1: V_{CC12}, 5V/Div, DC
CH2: V_{CC}, 2V/Div, DC
CH3: V_{OUT2}, 2V/Div, DC
CH4: $V_{SS2/EN2}$, 2V/Div, DC
TIME: 5ms/Div

VREF Output Voltage Power On



CH1: V_{CC12}, 5V/Div, DC
CH2: V_{CC}, 2V/Div, DC
CH3: V_{REF}, 2V/Div, DC
CH4: $V_{SS2/EN2}$, 2V/Div, DC
TIME: 5ms/Div

Phase Shift 180 Degress

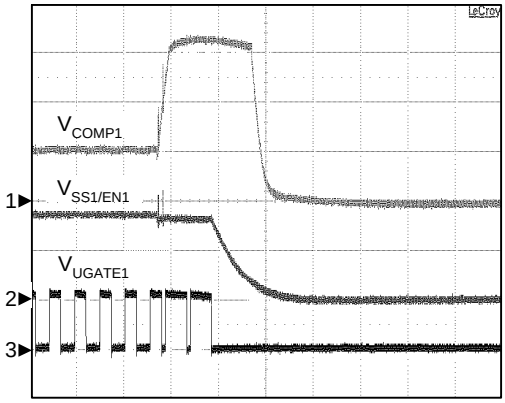


CH1: V_{UGATE1}, 10V/Div, DC
CH2: V_{LGATE1}, 10V/Div, DC
CH3: V_{UGATE2}, 10V/Div, DC
CH4: V_{LGATE2}, 10V/Div, DC
TIME: 2 µs/Div

Operating Waveforms (Cont.)

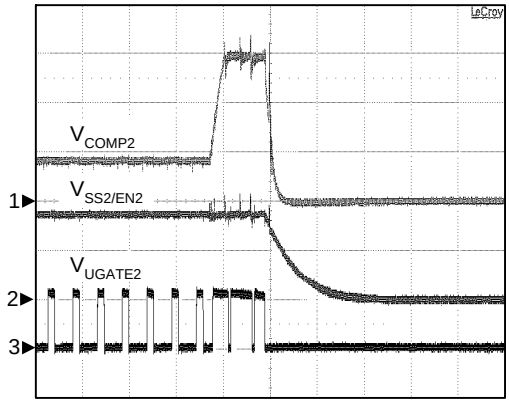
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

OUT1 Short Circuit Protection



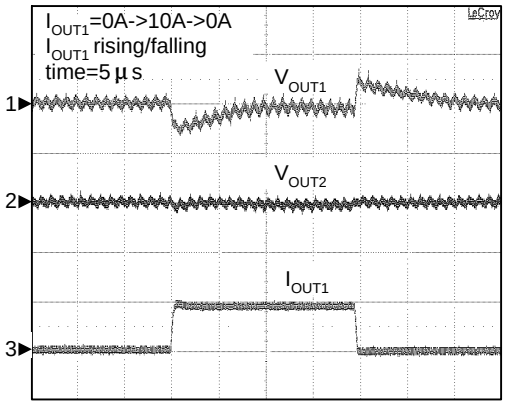
CH1: V_{COMP1}, 2V/Div, DC
CH2: $V_{SS1/EN1}$, 2V/Div, DC
CH3: V_{UGATE1}, 20V/Div, DC
TIME: 20 µs/Div

OUT2 Short Circuit Protection



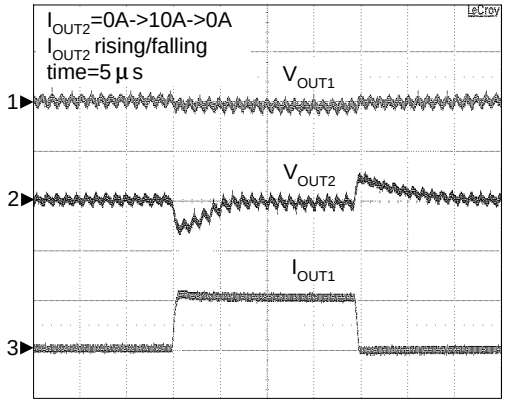
CH1: V_{COMP2}, 2V/Div, DC
CH2: $V_{SS2/EN2}$, 2V/Div, DC
CH3: V_{UGATE2}, 20V/Div, DC
TIME: 20 µs/Div

OUT1 Load Transient



CH1: V_{OUT1}, 200mV/Div, AC
CH2: V_{OUT2}, 200mV/Div, AC
CH3: I_{OUT1}, 10A/Div, DC
TIME: 50 µs/Div

OUT2 Load Transient

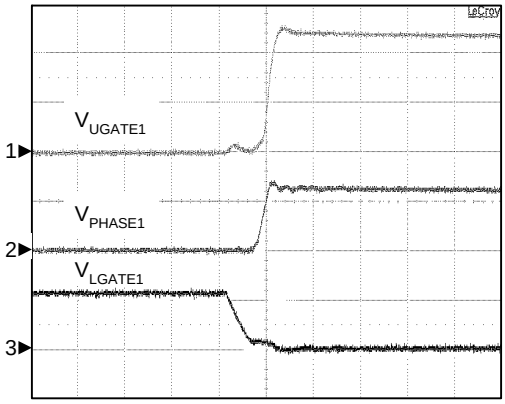


CH1: V_{OUT1}, 200mV/Div, AC
CH2: V_{OUT2}, 200mV/Div, AC
CH3: I_{OUT2}, 10A/Div, DC
TIME: 50 µs/Div

Operating Waveforms (Cont.)

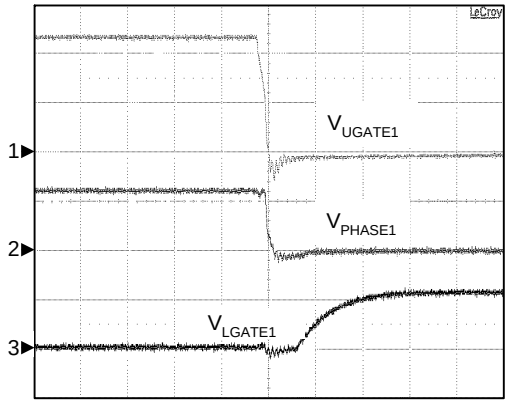
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

UGATE1 Voltage Rising



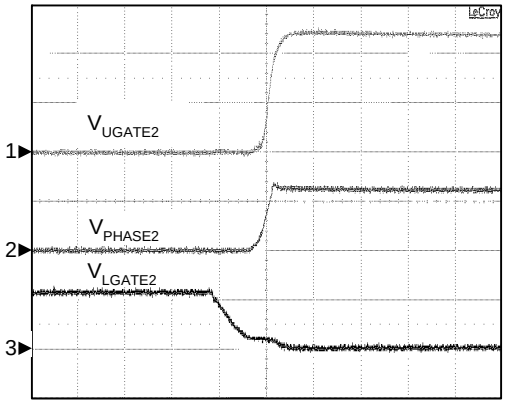
CH1: V_{UGATE1}, 10V/Div, DC
CH2: V_{PHASE1}, 10V/Div, DC
CH3: V_{LGATE1}, 10V/Div, DC
TIME: 100ns/Div

UGATE1 Voltage Falling



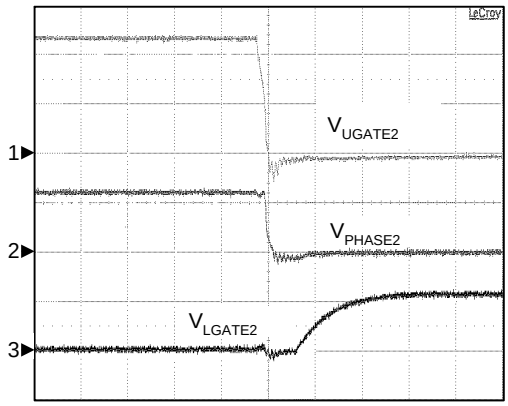
CH1: V_{UGATE1}, 10V/Div, DC
CH2: V_{PHASE1}, 10V/Div, DC
CH3: V_{LGATE1}, 10V/Div, DC
TIME: 100ns/Div

UGATE2 Voltage Rising



CH1: V_{UGATE2}, 10V/Div, DC
CH2: V_{PHASE2}, 10V/Div, DC
CH3: V_{LGATE2}, 10V/Div, DC
TIME: 100ns/Div

UGATE2 Voltage Falling

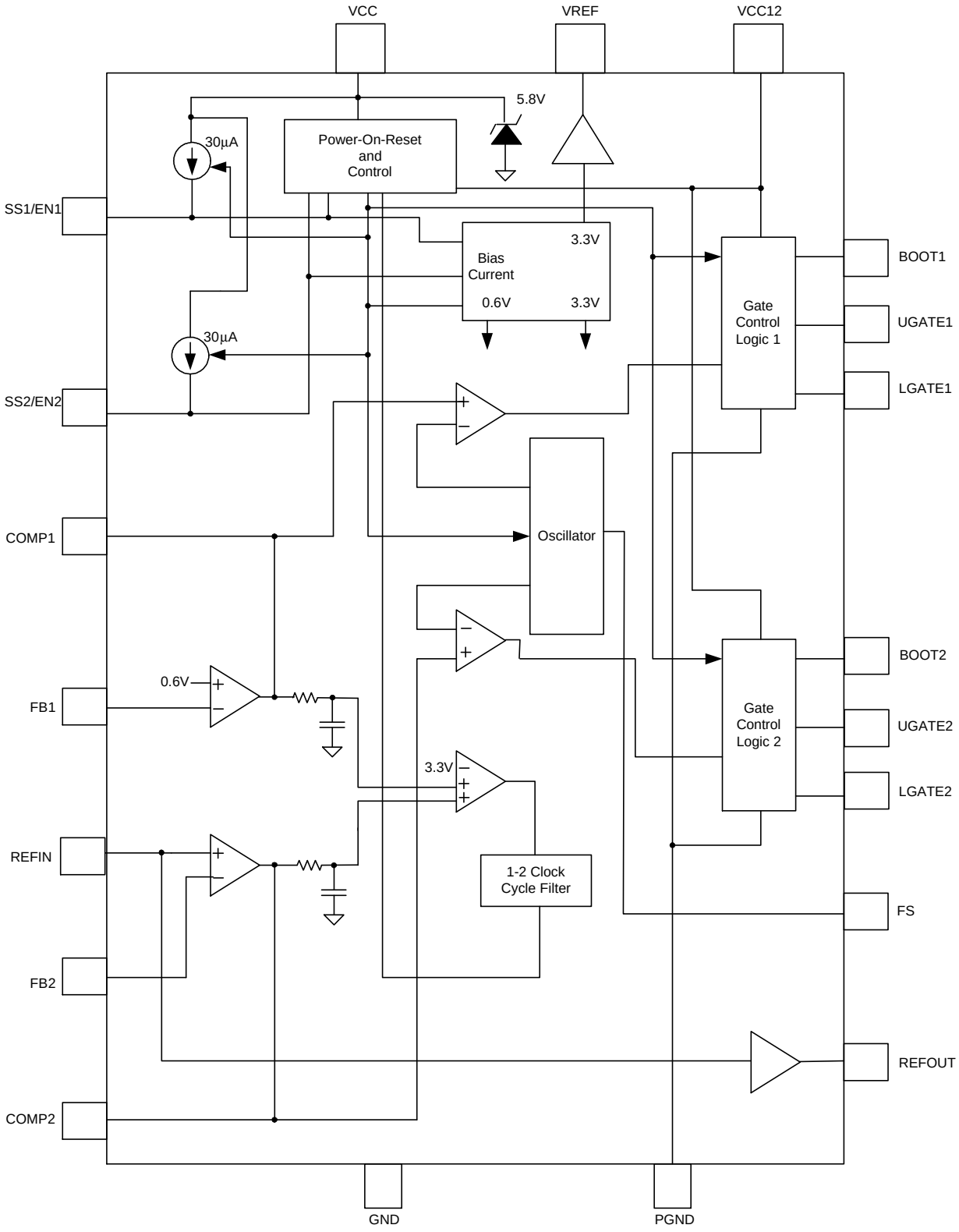


CH1: V_{UGATE2}, 10V/Div, DC
CH2: V_{PHASE2}, 10V/Div, DC
CH3: V_{LGATE2}, 10V/Div, DC
TIME: 100ns/Div

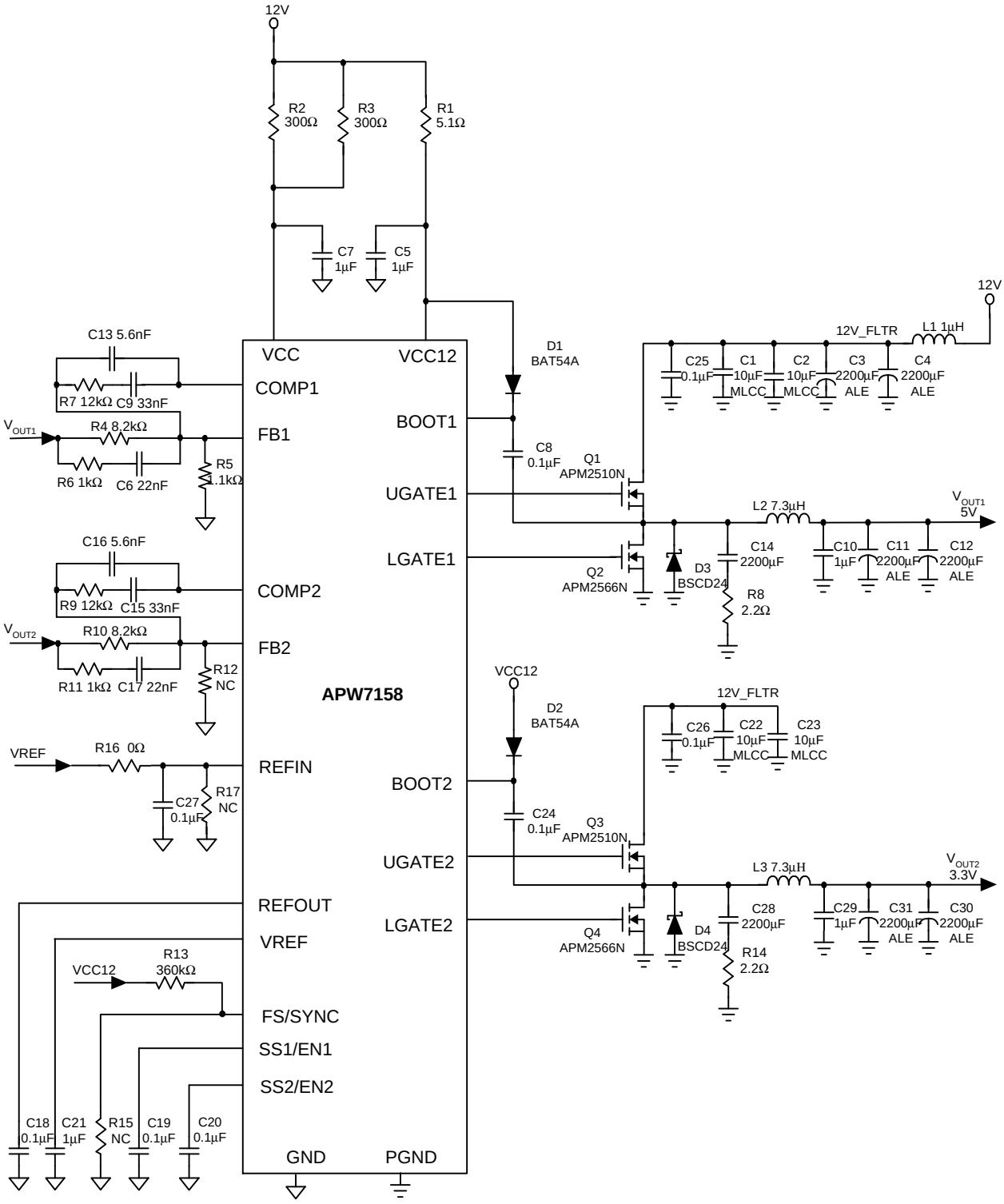
Pin Description

PIN		FUNCTION
NO.	NAME	
1	FB1	These pins are the inverting inputs of the error amplifiers of their respective regulators. They are used to set the output voltage and the compensation components.
2	COMP1	These pins are the outputs of error amplifiers of their respective regulators. They are used to set the compensation components.
3	COMP2	These pins are the outputs of error amplifiers of their respective regulators. They are used to set the compensation components.
4	FB2	These pins are the inverting inputs of the error amplifiers of their respective regulators. They are used to set the output voltage and the compensation components.
5	REFIN	This pin is the reference input voltage of error amplifier of OUT2. It also provides the voltage into a buffer, which is out on the REFOUT pin.
6	REFOUT	This pin provides a buffed voltage, which is from REFIN pin. A 0.1μF capacitor to ground is recommended for stability.
7	SS1/EN1	These pins provide two functions. Connect a capacitor to the GND for setting the soft-start time. Use an open drain logic signal to pull the SS/EN pin low to disable the respective output, leave it open to enable the respective output.
8	SS2/EN2	
9	VREF	This pin provides a 3.3V reference voltage, which can be used by the REFIN pin or other ICs as a voltage reference. A 1μF capacitor to ground is recommended for stability.
10	FS	This pin is used to adjust the switching frequency. Connecting a resistor from FS pin to GND increases the switching frequency. Conversely, connecting a resistor from this pin to VCC12 reduces the switching frequency.
11	GND	This pin is the signal ground pin for the IC.
12	UGATE2	These pins provide the gate driver for the upper MOSFETs of OUT1 and OUT2 respectively.
13	BOOT2	These pins provide the bootstrap voltage to the gate driver for driving the upper MOSFETs. A boostrap circuit may be used to create a BOOT voltage.
14	PGND	This pin is the power ground for the gate driver circuits. It should be tied to the GND.
15	LGATE2	These pins provide the gate driver for the lower MOSFETs of OUT1 and OUT2.
16	LGATE1	
17	VCC12	Power Supply Input Pin. Connect a nominal 12V power supply to this pin for the gate driver circuits. A decoupling capacitor (1 to 10μF) to GND is recommended for noise decoupling.
18	UGATE1	These pins provide the gate driver for the upper MOSFETs of OUT1 and OUT2 respectively.
19	BOOT1	These pins provide the bootstrap voltage to the gate driver for driving the upper MOSFETs. A boostrap circuit may be used to create a BOOT voltage.
20	VCC	Power Supply Input Pin. Connect a nominal 5V power supply to this pin for the control circuits, or connect a resistor (nominally 300Ω) to VCC12 to function this pin as a shunt regulator (typical 5.8V). A decoupling capacitor (1 to 10μF) to GND is recommended for noise decoupling.

Block Diagram



Typical Application Circuit



Function Description

Phase Shift

The device offers 180° phase shift function between OUT1 and OUT2. The advantage of Phase shift is to avoid overlapping the switching current spikes of the two channels or interaction between the channels; it also reduces the RMS current of the input capacitors, allowing fewer caps to be employed. However, because the phase shift between the rising edge of V_{LGATE1} and V_{LGATE2} (See Figure 1.) depends on the duty cycles, the falling edges of the two channels might overlap. Therefore, the user should check it.

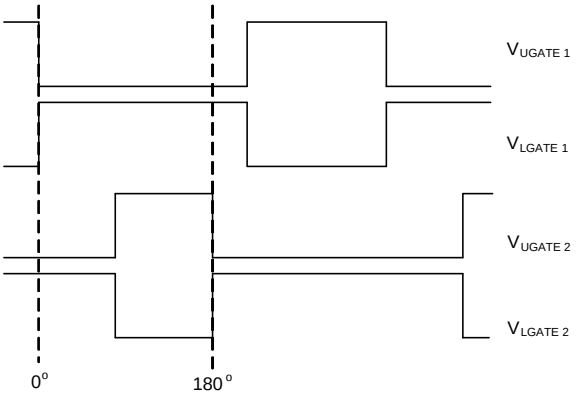


Figure 1. Phase of V_{LGATE2} with respect to rising edge of V_{LGATE1}

Soft-Start/Enable

The SS/EN pins control the soft-start and enable or disable the controller. The two regulators have independent soft-start and enable functions. Connect a soft-start capacitor from each SS/EN pin to the GND to set the soft-start interval, and an open drain logic signal for each SS/EN pin will enable or disable the respective output.

Figure 2 shows the soft-start interval. When both V_{CC} and V_{CC12} reach their Power-On-Reset threshold 4.23V and 7.8V, a 30µA current source starts to charge the capacitor. When the V_{SS} reaches the enabled threshold about 1V, the internal 0.6V reference starts to rise and follows the V_{SS}; the error amplifier output (V_{COMP}) suddenly raises to 1.1V, which is the valley of the oscillator's triangle wave, and leads the V_{OUT} to start up.

Until the V_{SS} reaches about 3.0V, the internal reference completes the soft-start interval and reaches to 0.6V, and then V_{OUT} is in regulation. The V_{SS} still rises to 3.5V and then stops.

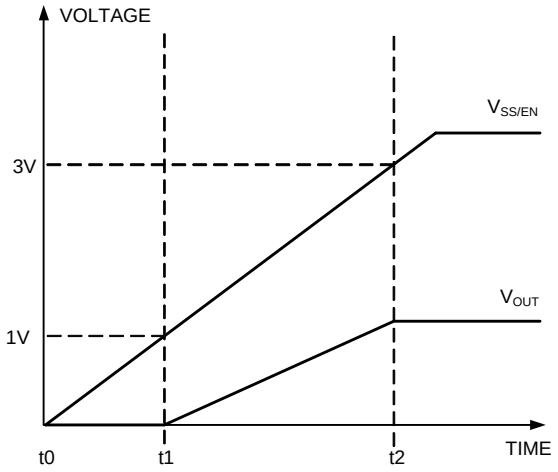


Figure 2. Soft-Start Interval

$$T_{SOFT-START} = t_2 - t_1 = \frac{C_{SS}}{I_{SS}} \cdot 2V$$

Where:

C_{SS} = external Soft-Start capacitor

I_{SS} = Soft-Start current = 30µA

Shunt Regulator

The APW7158 must have two power supplies V_{CC} (5V) and V_{CC12} (12V) to drive the IC; V_{CC} (5V) is for the control circuits and V_{CC12} (12V) is for the drivers of outputs. The shunt regulator is designed for these systems like figure 3 that do not have a 5V power supply; the range of the shunt regulator voltage (5.8V, typical) is designed over the usual range 4.5V to 5.5V of typical 5V power supplies. Connect a resistor from VCC12 pin to VCC pin for shunt regulator and for the supply current; the typical value, 300Ω of the resistor is recommended.

Function Description (Cont.)

Shunt Regulator (Cont.)

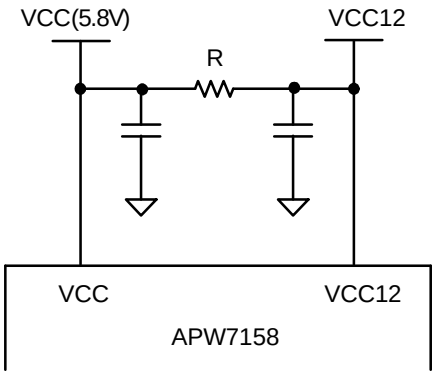


Figure 3. Optional R for Shunt Regulator

Oscillator

The APW7158 provides the oscillator switching frequency adjustment. Connect a resistor from FS pin to the ground; the nominal 300kHz oscillator switching frequency is increased according to the value of the resistor. Thus, the adjustment range of the switching frequency is nominal 300kHz to 800kHz. Conversely, connecting a resistor from FS pin to the VCC12 pin reduces the switching frequency according to the value of the resistor. Thus, the adjustment range of the switching frequency is 70kHz to nominal 300kHz. (See Figure 4.).

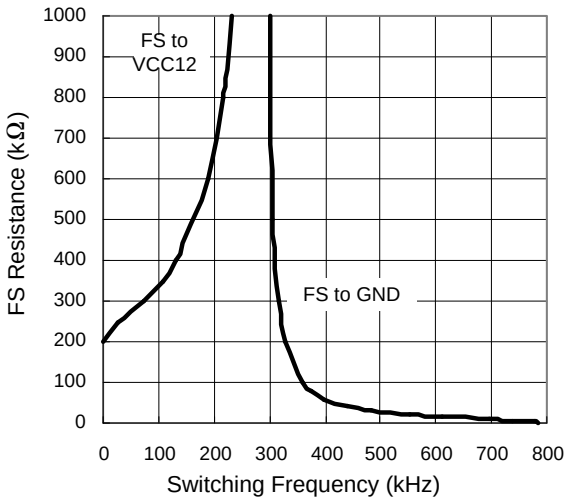


Figure 4. FS Resistance vs. Frequency

Short-Circuit Protection

The APW7158 has a simple short-circuit protection to monitor COMP1 pin and COMP2 pin for OUT1 and OUT2. When output voltage has a short, the FB pin should start to follow output since it is a resistor divider from the output. The FB pin is the inverting input of Error-Amp. When FB pin is lower than the Error-Amp reference, the V_{COMP} will rise to increase the duty-cycle of the upper MOSFET gate driver, and this allows output to get higher voltage. If the short-circuit condition is long enough, the V_{COMP} will exceed the trip point 3.3V and the duty circle will hit the maximum. This means that either Over-Current or Under-Voltage condition is detected. If any of the V_{COMP1} and V_{COMP2} exceed their trip points and hold over a filter time (1-2 clock cycles of switching frequency), all regulators will shut down and require a POR on either of VCC or VCC12 pin to restart.

Application Information

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with –40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between V_{COMP}, V_{FB} and V_{OUT} should be added.

The compensation network is shown in Fig. 8. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1+s\times ESR\times C_{OUT}}{s^2\times L\times C_{OUT}+s\times ESR\times C_{OUT}+1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L\times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$

The FLC is the double poles of the LC filter, and FESR is the zero introduced by the ESR of the output capacitor.

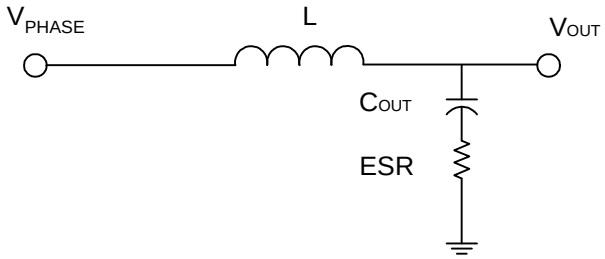


Figure 5. The Output LC Filter

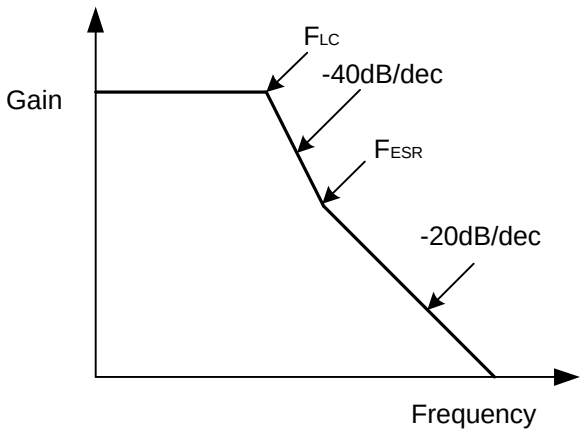


Figure 6. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure. 7. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

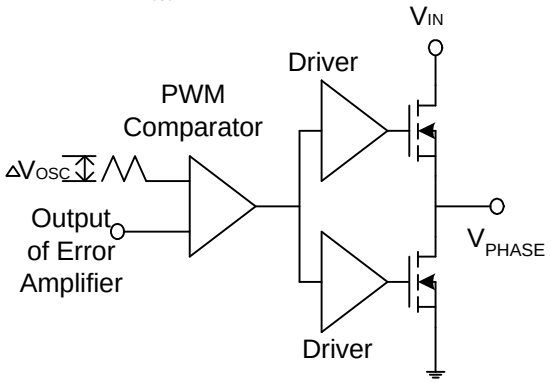


Figure 7. The PWM Modulator

The compensation circuit is shown in Figure 8. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin.

The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

Application Information (Cont.)

PWM Compensation (Cont.)

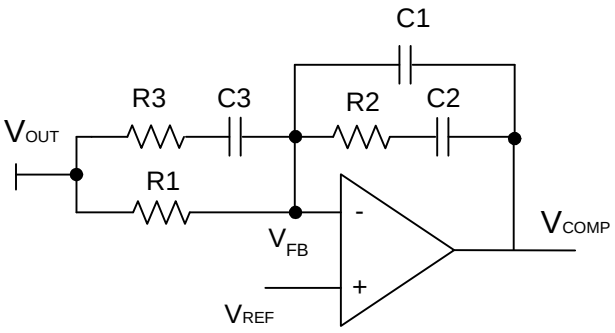


Figure 8. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times GAIN_{AMP}$$

Figure 9. Shows the asymptotic plot of the closed loop converter gain and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.
2. Select the desired zero crossover frequency F_O:
   (1/5 ~ 1/10) x F_S >F_O>F_{ESR}

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

   F_{Z1} = 0.75 x F_{LC}

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4.Set the pole at the ESR zero frequency F_{ESR}:

F_{P1} = F_{ESR}

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at half the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5xF_O

F_{Z2} = F_{LC}

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

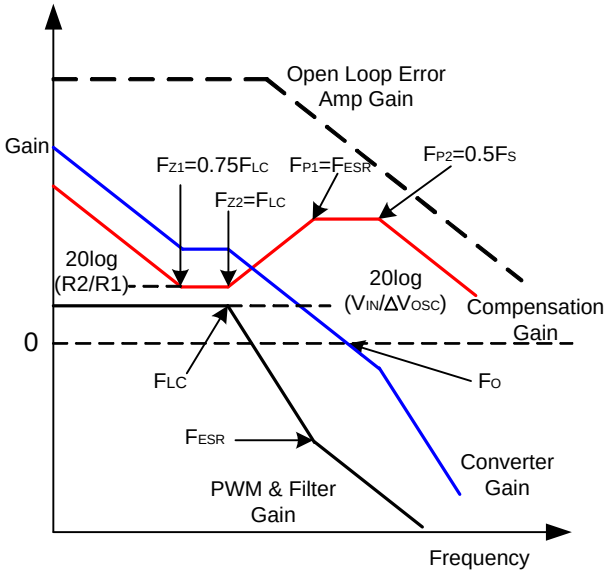


Figure 9. Converter Gain & Frequency

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta VOUT = I_{RIPPLE} \times ESR$$

Application Information (Cont.)

Output Inductor Selection (Cont.)

Where Fs is the switching frequency of the regulator. Although increase the inductor value and frequency reduce the ripple current and voltage, but there is a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_S) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher Capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore select high performance low ESR capacitors that are intended for switching regulator applications. In some applications, multiple capacitors have to be parallel to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.

The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1uF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following :

$$P_{UPPER}=I_{OUT}(1+TC)(R_{DS(ON)})D+(0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$$

$$P_{LOWER}=I_{OUT}(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current
TC is the temperature dependency of RDS(ON)
F_S is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching internal, t_{sw}, is a function of the reverse transfer capacitance C_{RSS}.

The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Short Circuit Protection

The APW7158 provides a simple short circuit protection function, and it is not easy to predict its performance, since many factors can affect how well it works. Therefore, the limitations and suggestions of this method must be provided for users to understand how to work it well.

- The short circuit protection was not designed to work for the output in initial short condition. In this case, the short circuit protection may not work, and damage the MOSFETs. If the circuit still works, remove the short can cause an inductive kick on the phase pin, and it may damage the IC and MOSFETs.
- If the resistance of the short is not low enough to cause protection, the regulator will work as the load has

Application Information (Cont.)

Short Circuit Protection (Cont.)

increased, and continue to regulate up until the MOSFETs is damaged. The resistance of the short should include wiring, PCB traces, contact resistances, and all of the return paths.

- The higher duty cycle will give a higher COMP voltage level, and it is easy to touch the trip point. The compensation components also affect the response of COMP voltage; smaller caps may give a faster response.
- The output current has faster rising time during short; the COMP pin will have a sharp rise. However, if the current rises too fast, it may cause a false trip. The output capacitance and its ESR can affect the rising time of the current during short.

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short, wide printed circuit traces.
Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 10 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout :

- The metal plate of the bottom of the packages (SOP-20) must be soldered to the PCB and connected to the GND plane on the backside through several thermal vias.
- Keep the switching nodes (UGATE, LGATE and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UGATE1, LGATE1, UGATE2, LGATE2) should be short and wide.
- Decoupling capacitor, compensation component, the resistor dividers, boot capacitors, and SS capacitors should be close their pins.
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (VIN and phase nodes) should be a large plane for heat sinking.

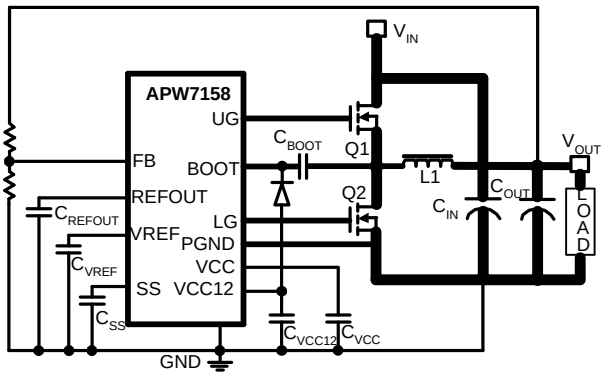
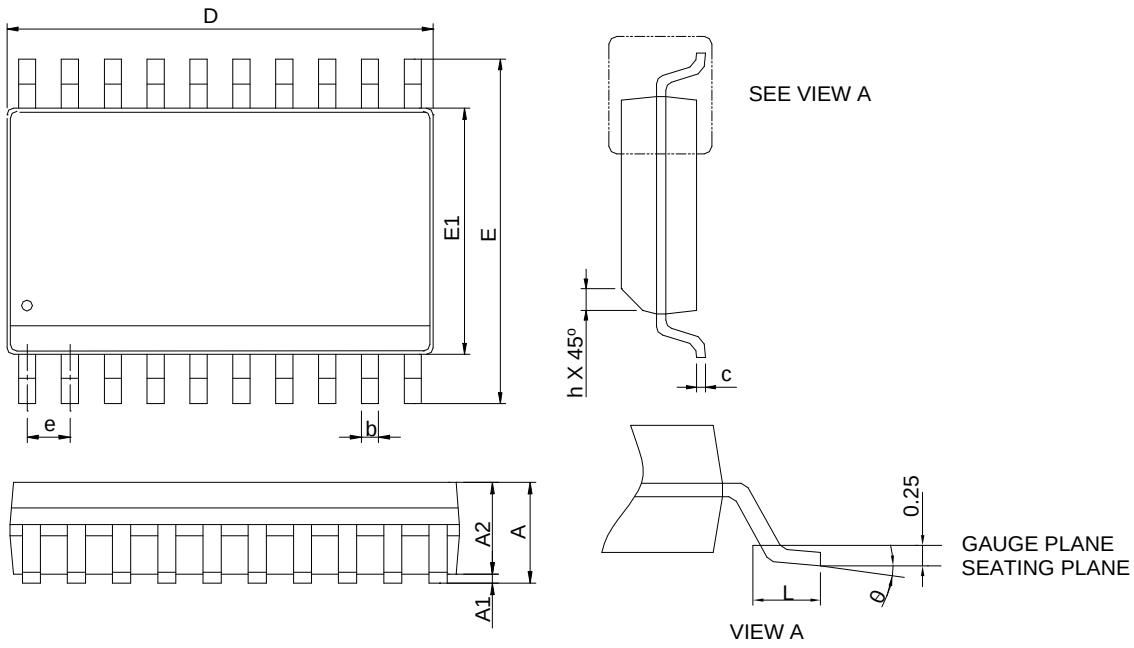


Figure 10. Layout Guidelines

Package Information

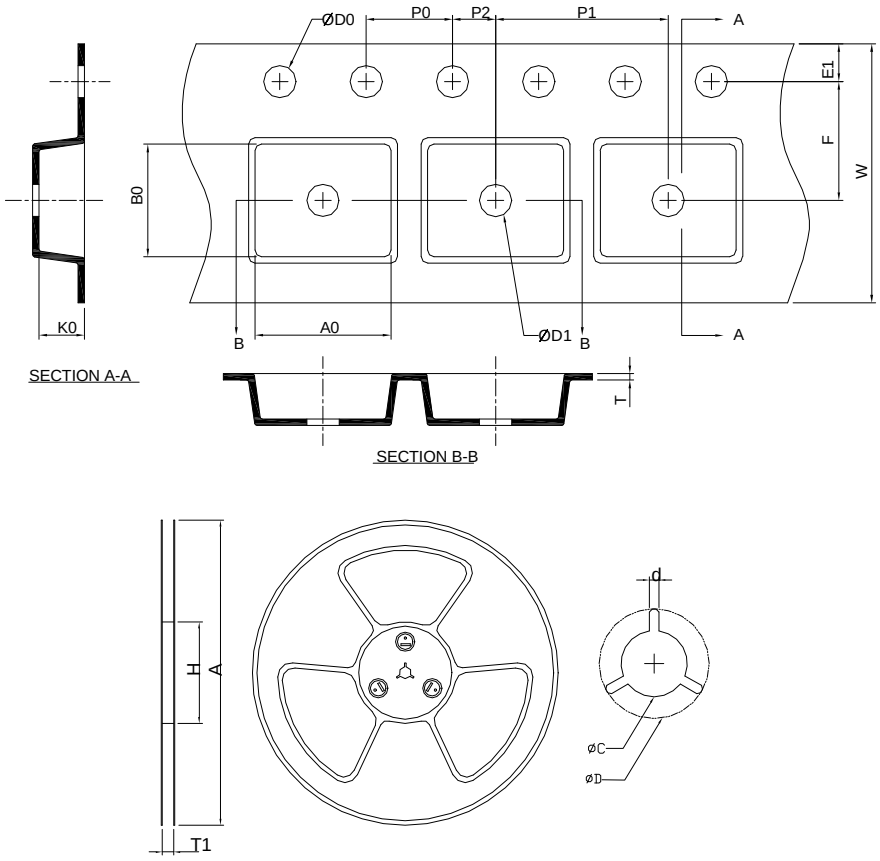
SOP-20



SYMBOL	SOP-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		2.65		0.104
A1	0.10	0.30	0.004	0.012
A2	2.05		0.081	
b	0.31	0.51	0.012	0.020
c	0.20	0.33	0.008	0.013
D	12.60	13.00	0.496	0.512
E	10.10	10.50	0.398	0.413
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
h	0.25	0.75	0.010	0.030
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MS-013 AC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-20	330.0±2.00	50 MIN.	24.40+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	24.0±0.30	1.75±0.10	11.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	10.9±0.20	13.3±0.20	3.1±0.20

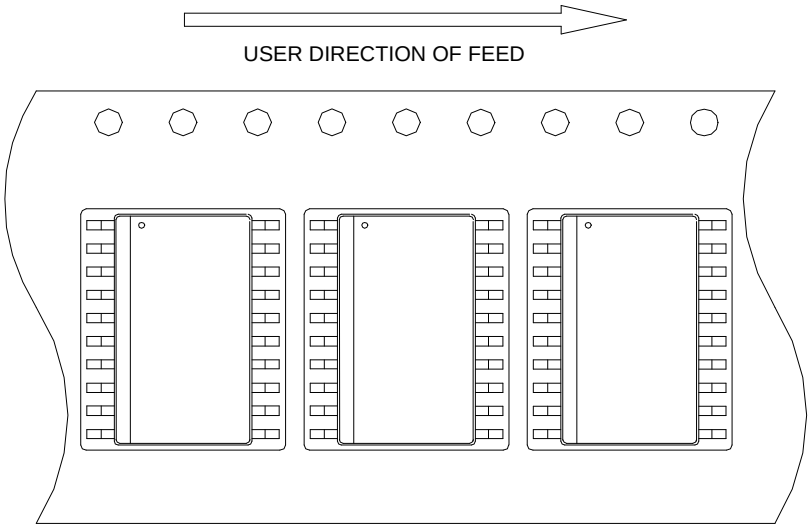
(mm)

Devices Per Unit

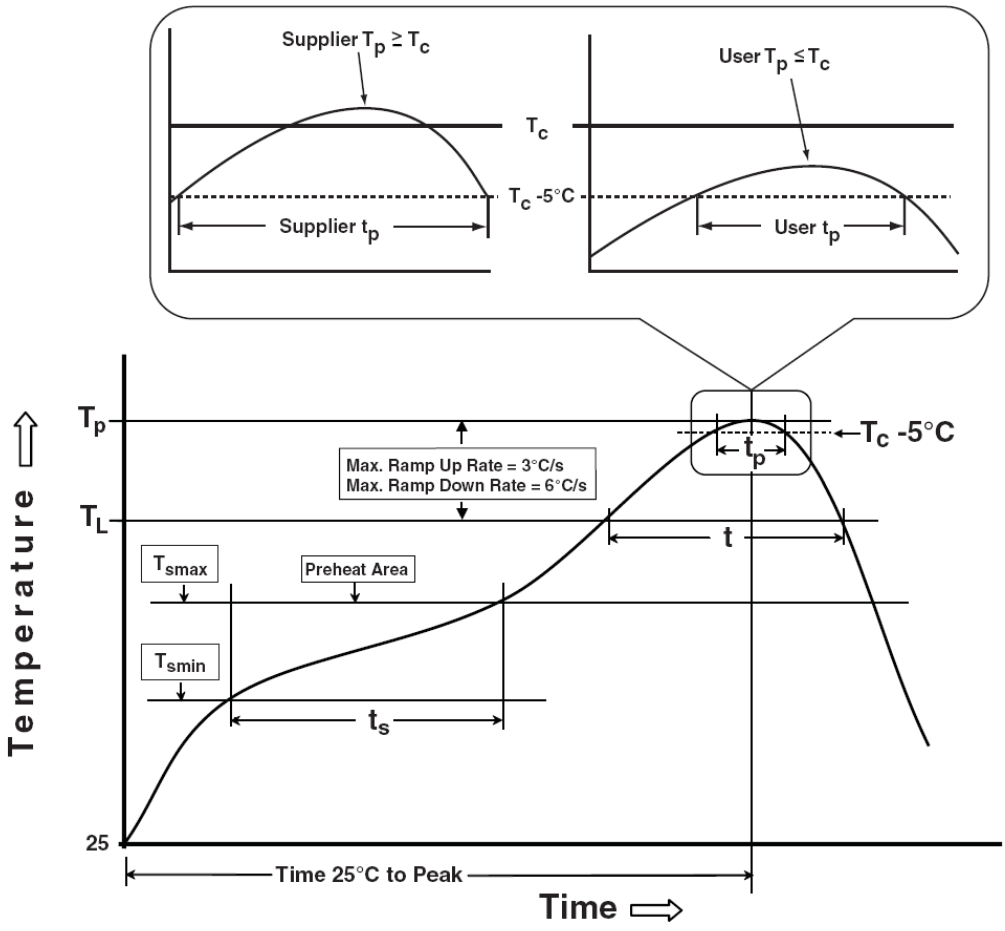
Package Type	Unit	Quantity
SOP-20	Tape & Reel	1000

Taping Direction Information

SOP-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838