

# MJD128T4G, NJVMJD128T4G (PNP)

## Complementary Darlington Power Transistor

### DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

#### Features

- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain:  $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Epoxy Meets UL 94 V-0 @ 0.125 in.
- ESD Ratings:
  - ♦ Human Body Model,  $3B > 8000$  V
  - ♦ Machine Model,  $C > 400$  V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	120	Vdc
Collector-Base Voltage	$V_{CB}$	120	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current Continuous Peak	$I_C$	8 16	Adc
Base Current	$I_B$	120	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

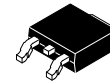
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**ON Semiconductor®**

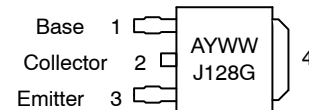
<http://onsemi.com>

**SILICON  
POWER TRANSISTOR  
8 AMPERES  
120 VOLTS, 20 WATTS**



**DPAK  
CASE 369C  
STYLE 1**

#### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
J128 = Device Code  
G = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping†
MJD128T4G	DPAK (Pb-Free)	2,500/Tape & Reel
NJVMJD128T4G	DPAK (Pb-Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MJD128T4G, NJVMJD128T4G (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	120	-	Vdc
Collector Cutoff Current ( $V_{CE} = 120\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	-	5	mA
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	-	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	-	2	mAdc

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 8\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	1000 100	12,000 -	-
Collector-Emitter Saturation Voltage ( $I_C = 4\text{ Adc}$ , $I_B = 16\text{ mAdc}$ ) ( $I_C = 8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{CE(sat)}$	- -	2 4	Vdc
Base-Emitter Saturation Voltage (1) ( $I_C = 8\text{ Adc}$ , $I_B = 80\text{ mAdc}$ )	$V_{BE(sat)}$	-	4.5	Vdc
Base-Emitter On Voltage ( $I_C = 4\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	-	2.8	Vdc

### DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ MHz}$ )	$ h_{fe} $	4	-	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	-	300	pF
Small-Signal Current Gain ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	300	-	-

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

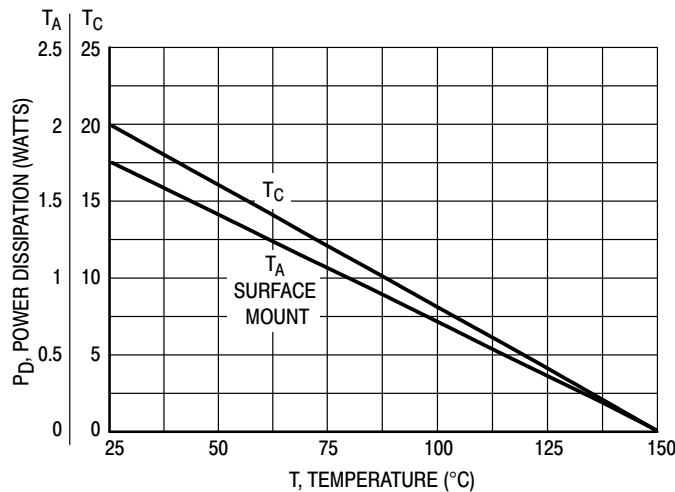


Figure 1. Power Derating

# MJD128T4G, NJVMJD128T4G (PNP)

## TYPICAL ELECTRICAL CHARACTERISTICS

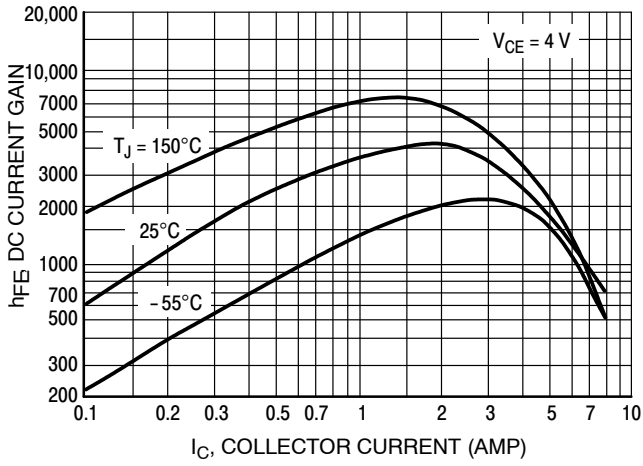


Figure 2. DC Current Gain

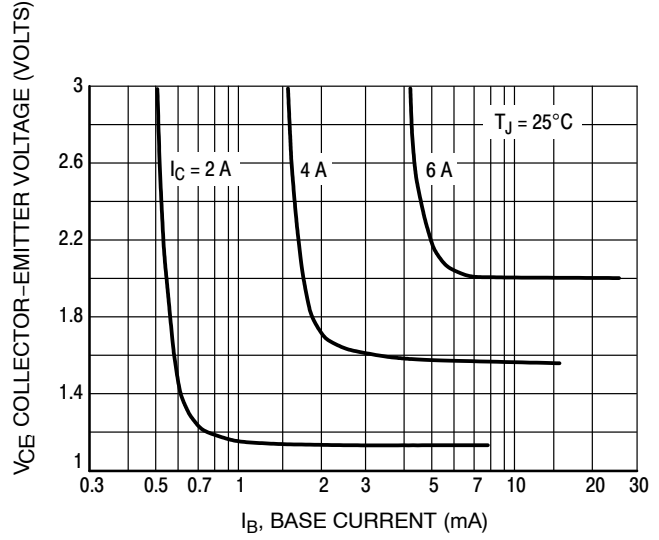


Figure 3. Collector Saturation Region

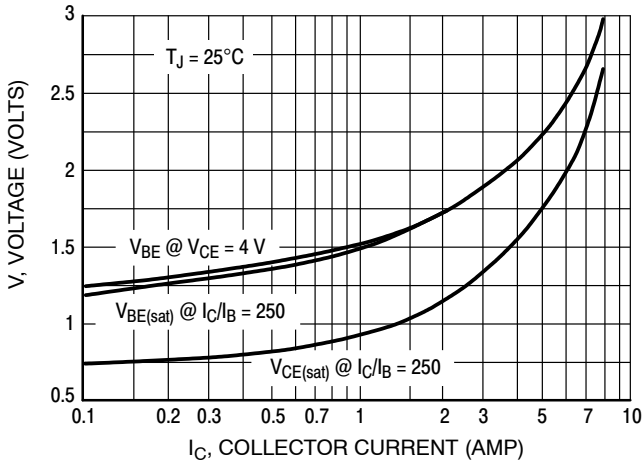


Figure 4. "On" Voltages

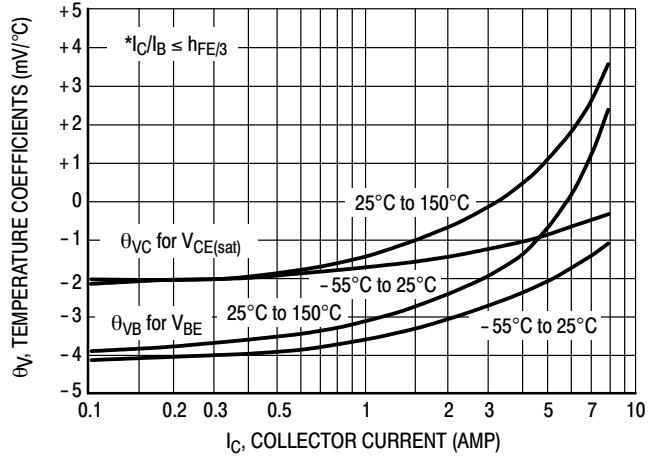


Figure 5. Temperature Coefficients

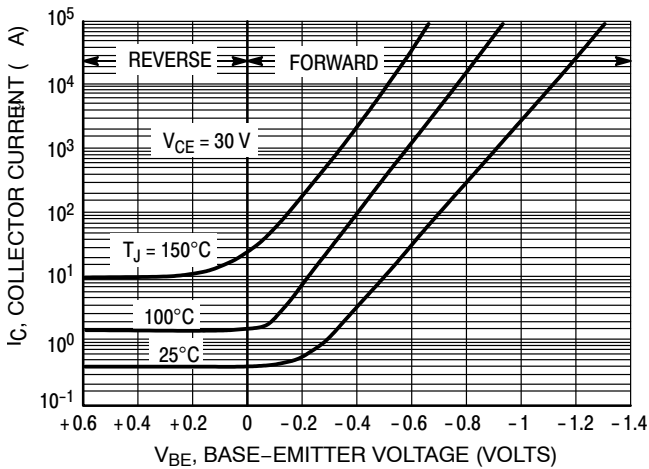


Figure 6. Collector Cut-Off Region

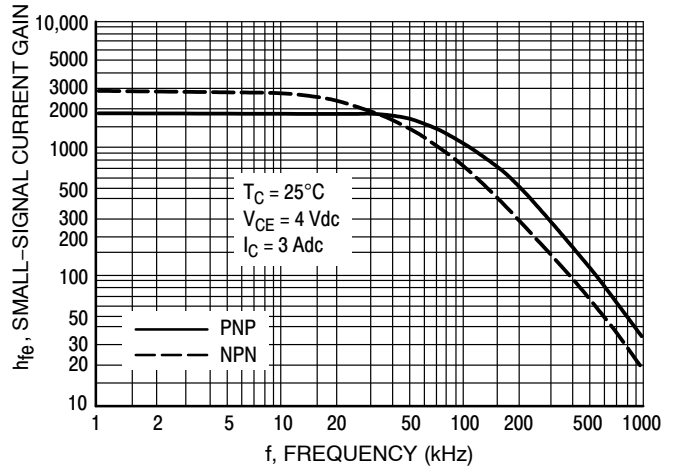


Figure 7. Small-Signal Current Gain

# MJD128T4G, NJVMJD128T4G (PNP)

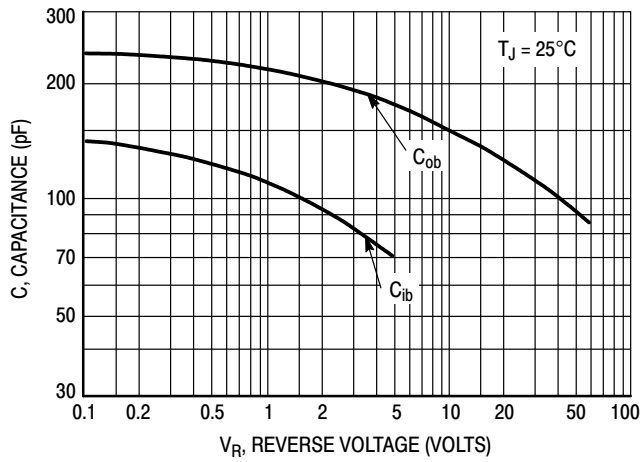


Figure 8. Capacitance

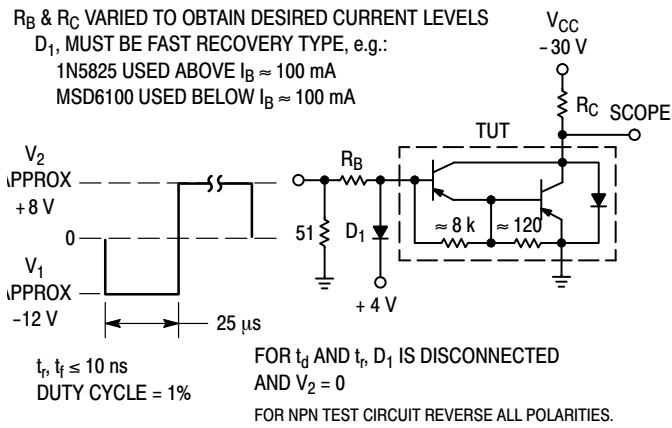


Figure 9. Switching Times Test Circuit

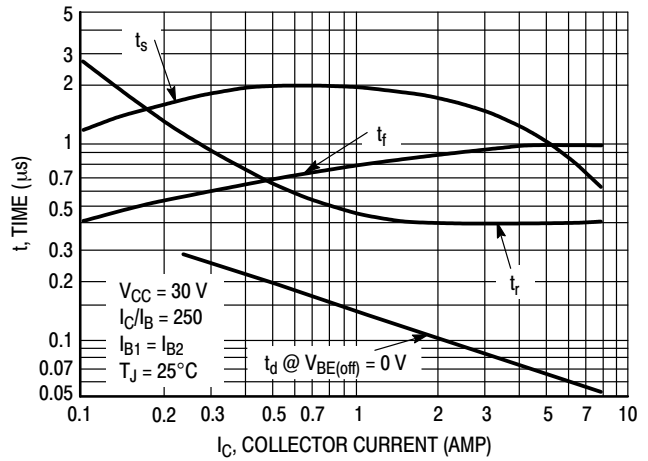


Figure 10. Switching Times

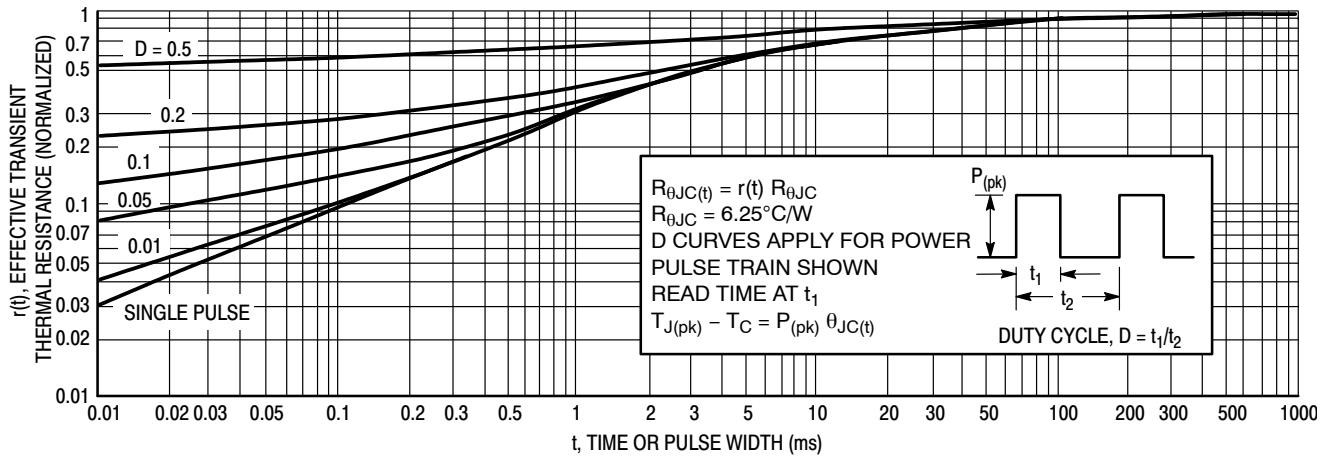
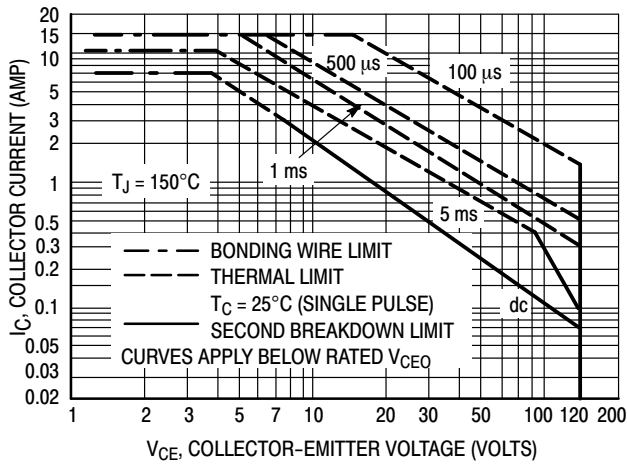


Figure 11. Thermal Response

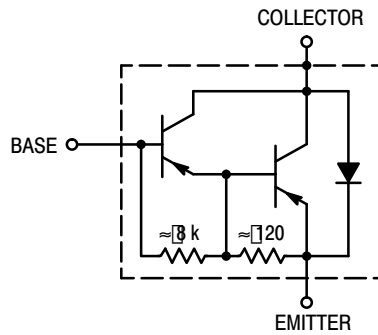
## MJD128T4G, NJVMJD128T4G (PNP)



**Figure 12. Maximum Forward Bias Safe Operating REA**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

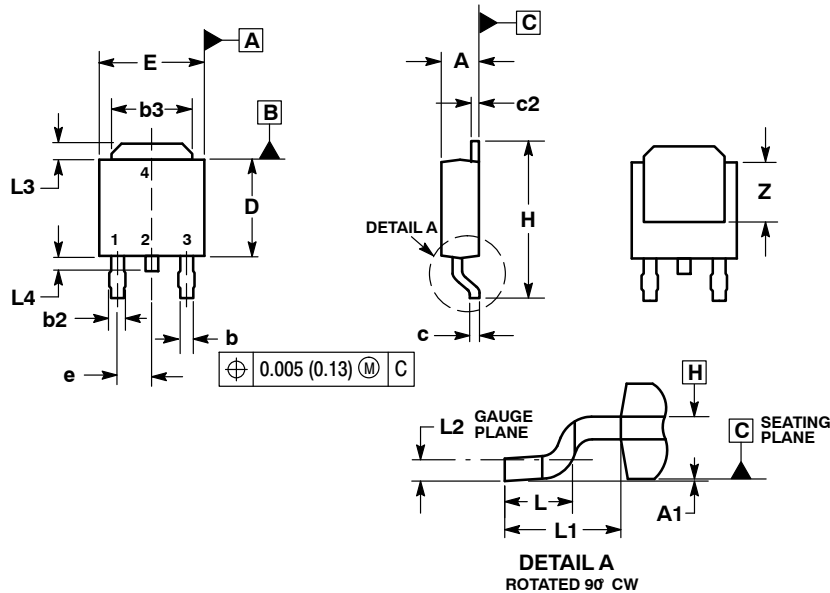


**Figure 13. Darlington Schematic**

# MJD128T4G, NJVMJD128T4G (PNP)

## PACKAGE DIMENSIONS

DPAK  
CASE 369C-01  
ISSUE D

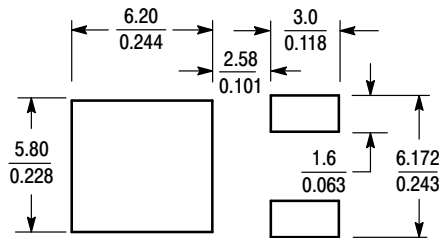


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative