KDS8333C

■ Features

- N-Channel

  4.1 A, 30 V $R_{DS(ON)}$ = 80mΩ @ V_{GS} = 10 V

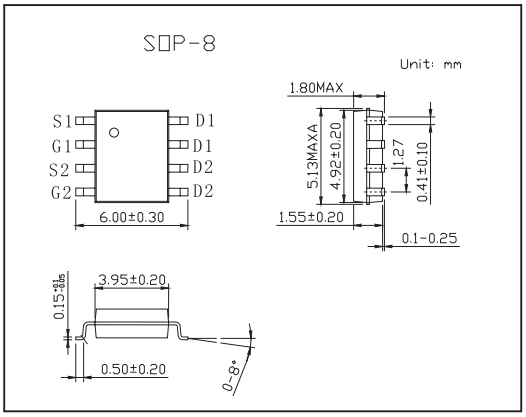
  $R_{DS(ON)}$ = 130mΩ @ V_{GS} =4.5V

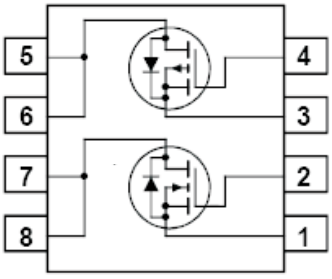
- P-Channel

  -3.4 A, 30 V $R_{DS(ON)}$ = 130 mΩ @ V_{GS} =- 10 V

  $R_{DS(ON)}$ = 200 mΩ @ V_{GS} =-4.5V

- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and handling capability in a widely used surface mount package.





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	30	-60	V
Gate to Source Voltage	V_{GS}	±16	±20	V
Drain Current Continuous (Note 1a)	I_D	4.1	-3.4	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation	P_D	2		W
Power Dissipation for Single Operation (Note 1a)	P_D	1.6		W
(Note 1b)		1		
(Note 1c)		0.9		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		℃/W

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■ Electrical Characteristics Ta = 25℃

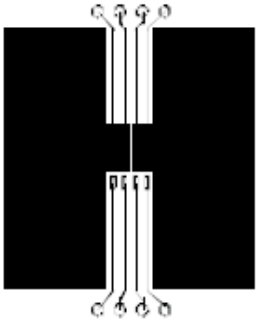
Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 μA	P-Ch	-30			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		25		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		-22		
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0 V	N-Ch			1	μA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-1	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±16V, V_{DS} = 0 V	N-Ch			±100	nA
		V_{GS} = ±20 V, V_{DS} = 0 V	P-Ch			±100	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	1	1.7	3	V
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch	-1	-1.8	-3	
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃	N-Ch		-4.2		mV/℃
		I_D = -250 μA, Referenced to 25℃	P-Ch		3.7		
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D =4.1A	N-Ch		67	80	mΩ
		V_{GS} = 10 V, I_D = 4.1 A,T_J = 125℃			81	130	
		V_{GS} = 4.5 V, I_D =3.2 A			103	145	
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10 V, I_D =-3.4A	P-Ch		105	130	
		V_{GS} = -10 V, I_D =-3.4 A,TJ = 125℃			167	200	
		V_{GS} = -4.5 V, I_D =-2.5A			147	220	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 5V	N-Ch	10			A
		V_{GS} = -10 V, V_{DS} = -5V	P-Ch	-5			
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 4.1A	N-Ch		9		S
		V_{DS} = -5V, I_D = -3.4A	P-Ch		5		
Input Capacitance	C_{iss}	N-Channel	N-Ch		282		pF
		V_{DS} = 10 V, V_{GS} = 0 V,f = 1.0 MHz	P-Ch		185		
Output Capacitance	C_{oss}		N-Ch		49		pF
		P-Channel	P-Ch		56		
Reverse Transfer Capacitance	C_{rss}	V_{DS} = -10 V, V_{GS} = 0 V,f = 1.0 MHz	N-Ch		20		pF
			P-Ch		26		
Gate Resistance	R_G	V_{GS}= 15 mV, f=1.0MHz	N-Ch		2.3		Ω
		V_{GS}=-15 mV, f=1.0MHz	P-Ch		-9.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel	N-Ch		4.5	9	ns
		V_{DD} = 10 V, I_D = 1 A,	P-Ch		4.5	9	
Turn-On Rise Time	tr	V_{GS} = 4.5 V, R_{GEN} = 6 Ω (Note 2)	N-Ch		6	12	ns
			P-Ch		13	23	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel	N-Ch		19	34	ns
		V_{DD} = -10 V, I_D = -1 A,	P-Ch		11	20	
Turn-Off Fall Time	tf	V_{GS} = -4.5 V, R_{GEN} = 6 Ω (Note 2)	N-Ch		1.5	3	ns
			P-Ch		2	4	
Total Gate Charge	Q_g	N-Channel	N-Ch		4.7	6.6	nC
		V_{DS} =10V,I_D=4.1A,V_{GS}=4.5V	P-Ch		4.1	5.7	
Gate-Source Charge	Q_{gs}	R_{GEN} = 6 Ω (Note 2)	N-Ch		0.9		nC
		P-Channel	P-Ch		0.8		
Gate-Drain Charge	Q_{gd}	V_{DS}=-10V,I_D=-3.4A,V_{GS}=-4.5V(Note 2)	N-Ch		0.6		nC
			P-Ch		0.4		

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.3A (Not 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -1.3A (Not 2)	P-Ch		0.8	-1.2	
Diode Reverse Recovery Time	t_{rr}	I_F = 4.1 A, di_F/dt = 100 A/μs	N-Ch		16.3		nS
		I_F = -3.4 A, di_F/dt = 100 A/μs	P-Ch		14.5		
Diode Reverse Recovery Charge	Q_{rr}	I_F = 4.1 A, di_F/dt = 100 A/μs	N-Ch		26.7		nC
		I_F = -3.4 A, di_F/dt = 100 A/μs	P-Ch		21.1		

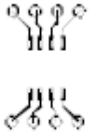
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper

b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%