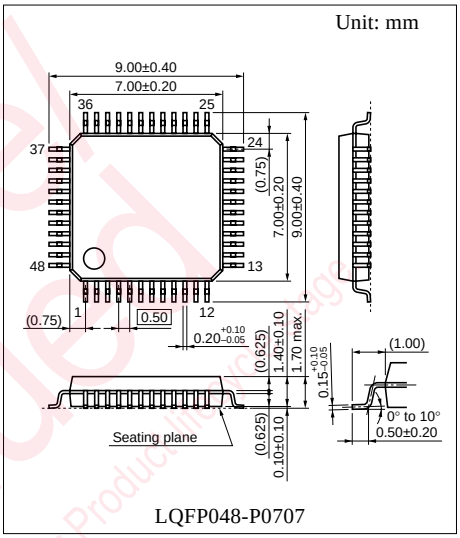
AN2537FHQ

Liquid crystal signal processing IC with built-in AV panel controller

■ Overview

The AN2537FHQ is an IC for driving a color liquid crystal panel (480-dot COG). The RGB decoder function for color difference signal, driver function and timing generator for panel drive are integrated on a single chip. The circuits and components required for liquid crystal panel driving can be drastically reduced.



LQFP048-P0707

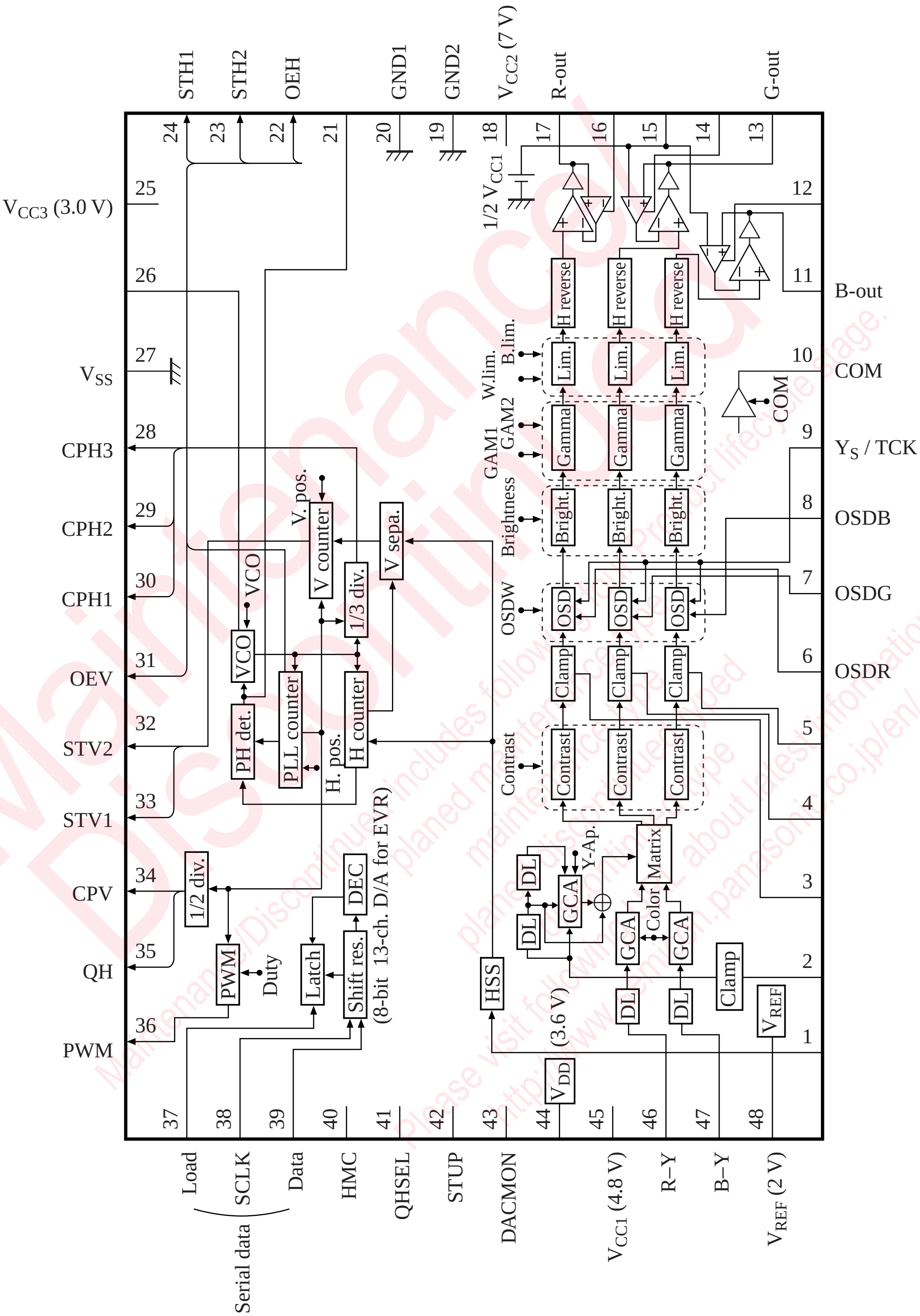
■ Features

- Built-in serial interface circuit
- Built-in electronic volume (D/A converter)
- Built-in gamma correction circuit
- Serial adjustment function of horizontal display position and vertical display position
- Back light control pulse output

■ Applications

- Small-sized liquid crystal monitors, small-sized crystal projectors

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Composite sync. signal input pin	25	V_{CC3} (Power supply for panel drive pulse: 3 V)
2	Luminance signal input pin	26	VCO free-running frequency adjusting pin
3	R-ch. clamp pin	27	V_{SS} (0 V)
4	G-ch. clamp pin	28	Horizontal shift clock 3 output pin
5	B-ch. clamp pin	29	Horizontal shift clock 2 output pin
6	R-ch. OSD signal input pin	30	Horizontal shift clock 1 output pin
7	G-ch. OSD signal input pin	31	Gate driver enable pulse output pin
8	B-ch. OSD signal input pin	32	Vertical display start pulse 2 output pin
9	OSD black signal control pulse input pin	33	Vertical display start pulse 1 output pin
10	Common signal output pin	34	Vertical shift clock output pin
11	B-ch. driver output pin	35	Arrangement changeover signal output pin
12	B-ch. driver feedback pin	36	Back light pulse output pin
13	G-ch. driver output pin	37	Serial data write pulse input pin
14	G-ch. driver feedback pin	38	Serial data shift clock input pin
15	Chroma signal output center voltage pin	39	Serial data input pin
16	R-ch. driver feedback pin	40	Screen right and left reversing control signal input pin
17	R-ch. driver output pin	41	Screen up side down control signal input pin
18	V_{CC2} (Power supply for chroma driver: 7 V)	42	Control signal output inhibit control pin
19	GND2 (0 V)	43	DAC monitor pin
20	GND1 (0 V)	44	V_{DD} (Power supply for internal Logic: 3.6 V)
21	Horizontal PLL loop filter connection pin	45	V_{CC1} (Power supply for signal processing: 4.8 V)
22	Source driver enable pulse output pin	46	R−Y signal input pin
23	Horizontal display start pulse 2 output pin	47	B−Y signal input pin
24	Horizontal display start pulse 1 output pin	48	V_{REF} (Internal reference voltage)

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1}	5.5	V
	V_{CC2}	8.5	
	V_{CC3}	3.8	
Supply current	I_{CC}	—	mA
Power dissipation *2	P_D	249	mW
Operating ambient temperature *1	T_{opr}	−20 to +70	°C
Storage temperature *1	T_{stg}	−55 to +125	°C

Note) ∗1: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.
∗2: The power dissipation shall be at operating ambient temperature T_a = 70°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	4.5 to 5.1	V
	V_{CC2}	6.0 to 8.0	
	V_{CC3}	2.7 to 3.6	
Y input signal voltage (Pedestal to white)	Y_{IN}	0.5 to 0.7(typ.) to 1.0	V[p-p]
R−Y input signal	RY_{IN}	150 to 190 (typ.) to 230	mV[p-p]
B−Y input signal	BY_{IN}	190 to 240 (typ.) to 290	mV[p-p]
Sync. signal input (Pedestal to sync. chip)	H_{SYNC}	0.08 to 0.286 (typ.)	V[p-p]
Serial data transfer frequency	f_{SD}	1.0 (max.)	MHz
MOS input signal low-level voltage	V_{MOSL}	0 to 0.8	V
MOS input signal high-level voltage	V_{MOSH}	2.8 to lower than V_{CC1} (pin 45)	V

■ Electrical Characteristics at T_a = 25°C

1. DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit current 1	I_{CC1}	V_{CC1} = 4.8 V, V_{CC2} = 7 V	15.4	—	30.6	mA
Circuit current 2	I_{CC2}	V_{CC1} = 4.8 V, V_{CC2} = 7 V	2.89	—	6.81	mA
Circuit current 3	I_{CC3}	V_{CC3} = 3 V	—	—	1.0	mA

2. AC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chroma block						
Sharpness control characteristics	G_{SH}	SG1, CH5 = "FF"/"02"	7.6	—	—	dB
Sharpness frequency characteristics	f_{SH}	SG1, CH5 = "80", f = 2 MHz/100 kHz	3.3	—	—	dB
Contrast adjustment range 1	G_{CONT1}	SG3, CH10 = "FF"/"80"	3.0	4.0	—	dB
Contrast adjustment range 2	G_{CONT2}	SG3, CH10 = "00"/"80"	—	—	–5.8	dB
R-ch./G-ch. relative amplitude	V_{RG}	SG3	– 0.3	0.0	+0.3	V[p-p]
B-ch./G-ch. relative amplitude	V_{BG}	SG3	– 0.3	0.0	+0.3	V[p-p]
R, G, B output pedestal amplitude min.	V_{PEDmin}	CH15 = "FF", (A): SG3	—	—	–1.3	V[p-p]
R,G,B output pedestal amplitude max.	V_{PEDmax}	CH15 = "00", (A): SG3	3.6	—	—	V[p-p]
R,G,B output DC voltage	V_{ODC}	SG3	2.18	2.4	2.62	V
Gamma 1 characteristics 1	V_{GAM11}	SG3	–5.7	–3.0	– 0.3	dB
Gamma 1 characteristics 2	V_{GAM12}	SG3	–8.2	—	—	dB
Gamma 1 characteristics 3	V_{GAM13}	SG3	–3.7	—	—	dB
OSD white level min.	V_{WHmin}	SG3, CH4 = "00"	—	—	2 600	mV[p-p]
OSD white level max.	V_{WHmax}	SG3, CH4 = "FF"	90	—	—	mV[p-p]
OSD black level	V_{BL}	SG2	– 0.52	—	0.22	V
Black limiter level min.	V_{LIMBL}	SG2, CH9 = "FF"	3.7	—	—	V[p-p]
Black limiter level max.	V_{LIMBH}	SG2, CH9 = "00"	—	—	3.3	V[p-p]
White limiter level min.	V_{LIMWL}	SG2, CH11 = "00"	1.48	—	—	V[p-p]
White limiter level max.	V_{LIMWH}	SG2, CH11 = "FF"	—	—	4.3	V[p-p]
R–Y typical gain	G_{RY}	(C): SG4	22.0	—	32.0	dB
B–Y typical gain	G_{BY}	(B): SG4	22.0	—	32.0	dB
R–Y/G–Y relative gain	G_{RYGY}	(C): SG4	–2.0	0.0	+2.0	dB
B–Y/G–Y relative gain	G_{BYGY}	(B): SG4	–2.0	0.0	+2.0	dB
Common amplitude level min.	V_{COML}	CH14 = "00"	—	—	0.1	V[p-p]
Common amplitude level max.	V_{COMH}	CH14 = "FF"	3.4	—	—	V[p-p]

■ Electrical Characteristics at T_a = 25°C (continued)

2. AC characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Logic block						
LCD drive pulse output level low	V_{OL}		—	—	0.6	V
LCD drive pulse output level high	V_{OH}		2.4	—	—	V
CMOS block input level low	V_{THL}		—	—	1.1	V
CMOS block input level high	V_{THH}		2.9	—	—	V
Horizontal sync. pull-in range low	P_{RHDL}	SG2 (Y_S = 300 mV, Y_Y = 0 mV)	—	—	−1.0	kHz
Horizontal sync. pull-in range high	P_{RHDH}	SG2 (Y_S = 300 mV, Y_Y = 0 mV)	1.0	—	—	kHz
Clock driver Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.						
Horizontal clock rise time (CPHn, /CPHn)	t_{r1}	n: 1 to 3	—	—	50	ns
Horizontal clock fall time (CPHn, /CPHn)	t_{f1}	n: 1 to 3	—	—	50	ns
Phase error between horizontal clocks (CPHn, /CPHn)	t_{d1}	n: 1 to 3	−20	—	+20	ns
STH 1, STH2 rise time	t_{r2}		—	—	50	ns
STH 1, STH2 fall time	t_{f2}		—	—	50	ns
CPH1, /CPH1, STH1, STH2 rise and fall error	t_{d2}		−50	—	+50	ns
Vertical clock rise time (CPV)	t_{r3}		—	—	50	ns
Vertical clock fall time (CPV)	t_{f3}		—	—	50	ns
STV1, STV2 rise time	t_{r4}		—	—	50	ns
STV1, STV2 fall time	t_{f4}		—	—	50	ns
CPV, STV1, STV2 rise and fall error	t_{d4}		−50	—	50	ns

■ Electrical Characteristics at T_a = 25°C (continued)

3. Operation timing

1) Horizontal-system output timing

Parameter		NTSC	Unit
Horizontal line period *1	H	63.5 202	µs FY
Video effective period *1	t_{Hy}	52.7	µs
Horizontal flyback period *1	t_{Hr}	10.9	µs
Video display effective picture element *1 (on panel)	t_{Hv}	480 50.2	dot µs
Horizontal display ratio (t_{Hv}/t_{Hy}) *1	R_H	95.3	%
Horizontal frequency dividing ratio (1H)	N_H	202	
VCO oscillation frequency *1	f_{VCO}	19.07	MHz
Clock frequency *1	f_{FY}	3.18	MHz
STH rise	TSTH	Serial variable range 17 to 49	 FY
STH pulse width	TwSTH	1.0	FY
CPH1, CPH2, CPH3 clock period	TCPH	1.0	FY
CPH1, CPH2, CPH3 pulse width	t_{wCPH}	0.5	µs
FRP polarity reverse position	TFRP	7 (2.2)	FY(µs)
OEV pulse width	TwOEV	3 (0.9)	FY(µs)

Note) ∗1: The reference values on liquid crystal panel display, not guaranteed values.
The signal name in ( ) indicates the internal signal name.

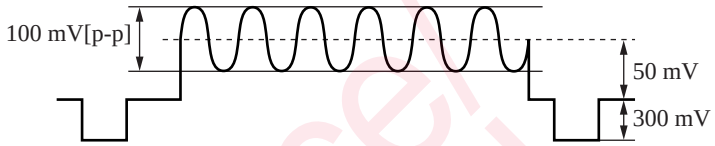
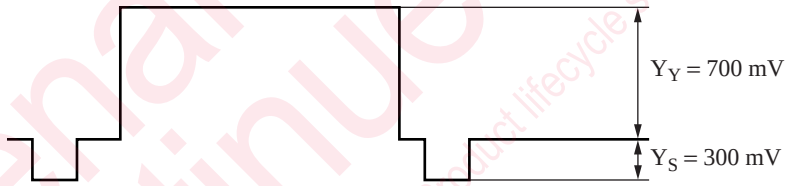
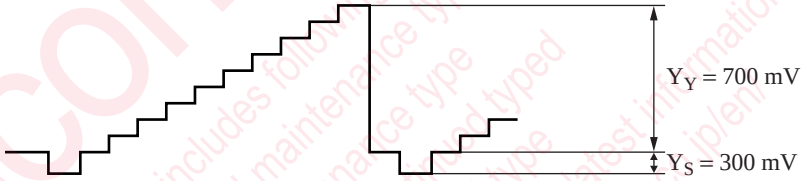
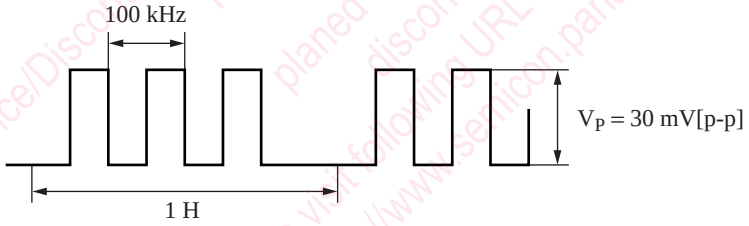
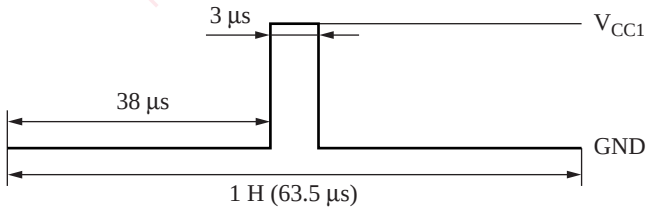
2) Vertical-system output timing

Parameter		NTSC	Unit
Vertical line period *1	V	262.5	H
Video effective period *1	t_{Hy}	242.5	H
Vertical display section *1	t_{Hv}	234	H
Vertical display ratio (t_{Hv}/t_{Hy}) *1	R_V	96.5	%
(V-sync. fall position : Odd number : Even number)	TVS	1.0 0.5/1.5	H
(V-sync. pulse width)	TwVS	1.0	H
STV rise	TSTV	Serial variable range 7 to 23	 H
STV pulse width	TwSTV	1.0	H
CPV clock period	TCPV	1.0	H
CPV pulse width	TwCPV	30 (9.28)	H

Note) ∗1: The reference values on liquid crystal panel display, not guaranteed values.
The signal name in ( ) indicates the internal signal name.

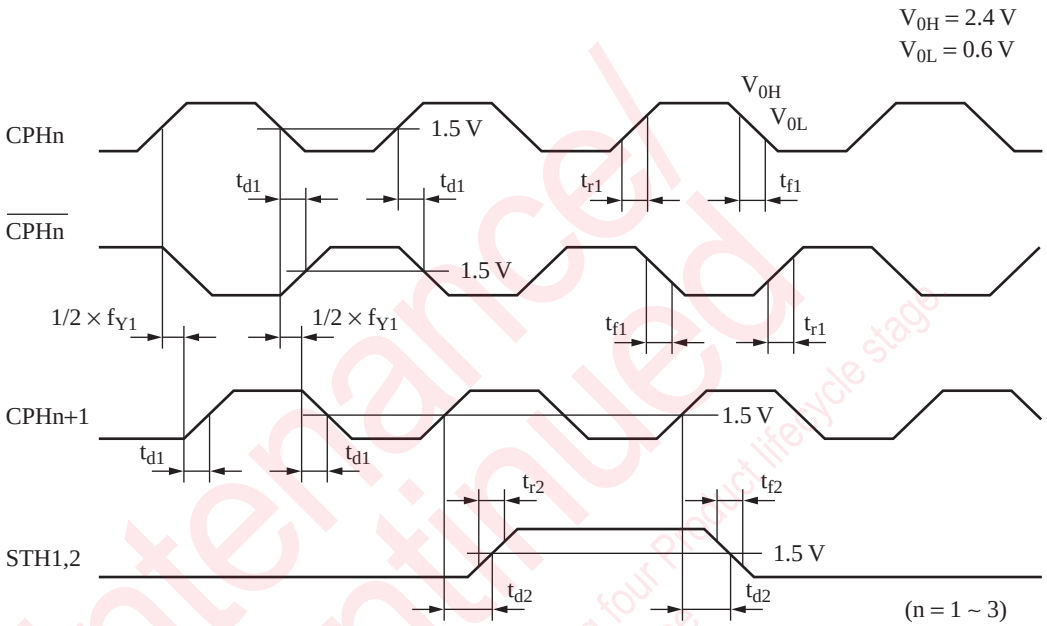
■ Test Circuits

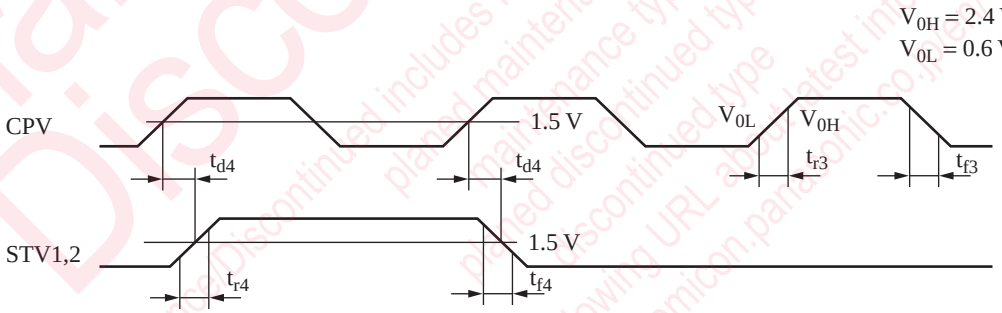
1. Signal waveforms for inspection

Signal name	Signal waveform
SG1 (sine wave video signal)	
SG2 (white signal)	
SG3 (10-step staircase)	
SG4 (Color difference quasi-signal)	
SG5 (OSD signal)	

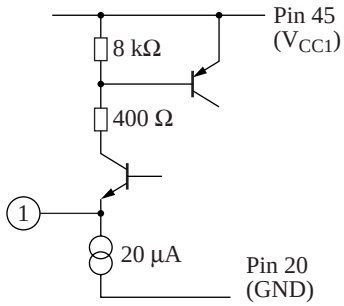
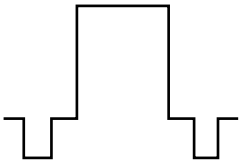
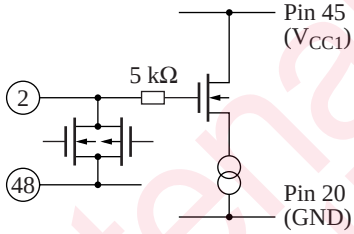
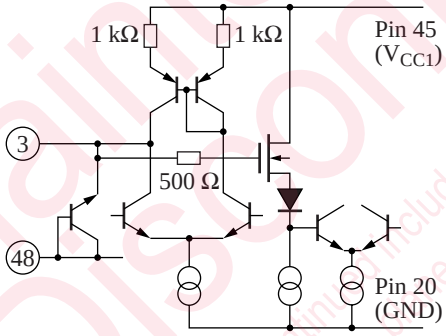
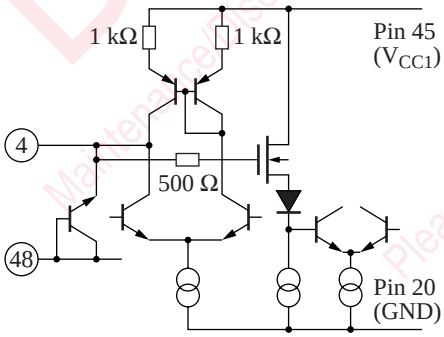
■ Test Circuits (continued)

2. AC characteristics Clock driver output

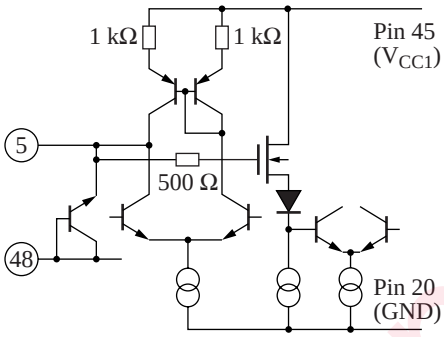
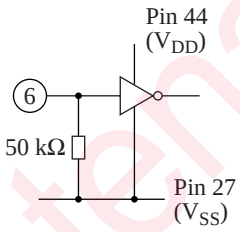
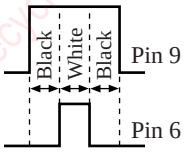
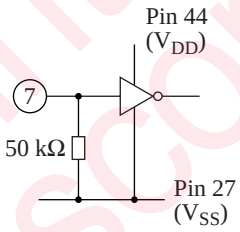
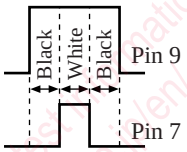
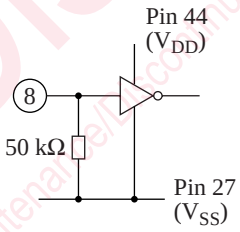
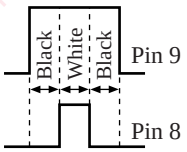
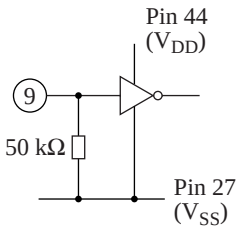
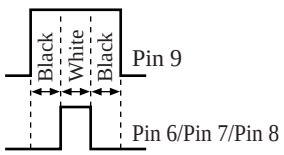




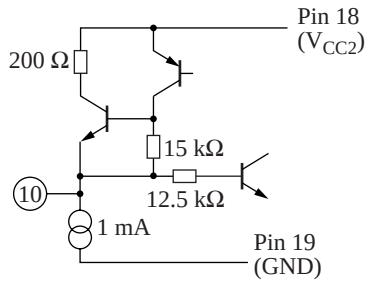
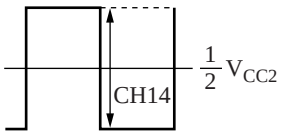
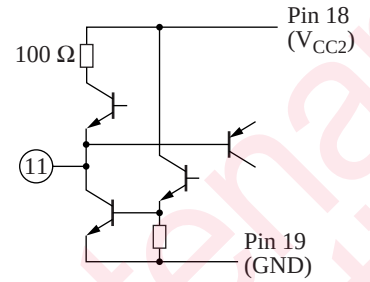
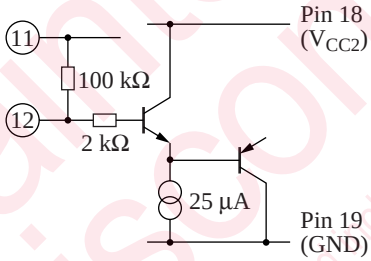
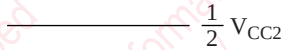
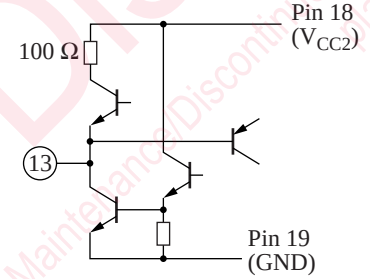
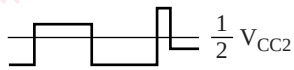
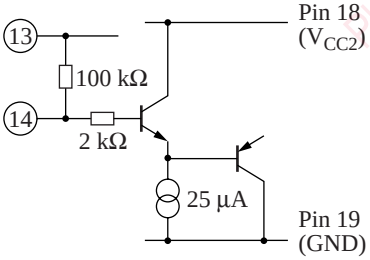
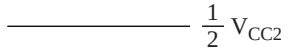
■ Terminal Equivalent Circuits

PinNo.	Equivalent circuit	Description	Signal waveform
1		Sync.: C. Sync. input pin Sync. signal is separated from luminance signal.	
2		Y-in: Luminance signal input pin	
3		RHC: Connection pin for an R-ch. signal clamp capacitor	DC
4		GHC: Connection pin for a G-ch. signal clamp capacitor	DC

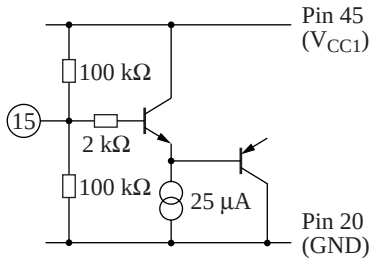
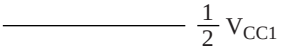
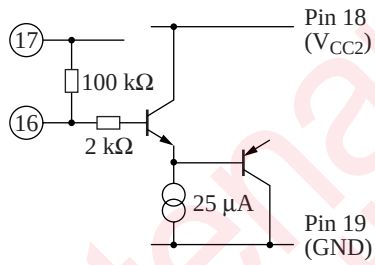
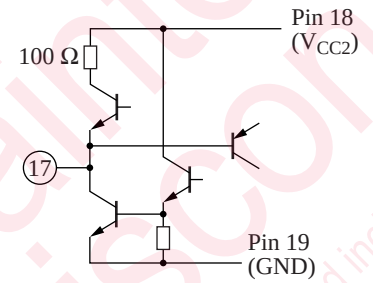
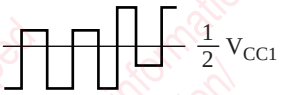
■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
5		BHC: Connection pin for a B-ch. signal clamp capacitor	DC
6		OSDR: R-ch. OSD white signal input CMOS input (50 kΩ pull-down)	
7		OSDG: G-ch. OSD white signal input CMOS input (50 kΩ pull-down)	
8		OSDB: B-ch. OSD white signal input CMOS input (50 kΩ pull-down)	
9		Y_S / TCK: OSD black signal input CMOS input (50 kΩ pull-down)	

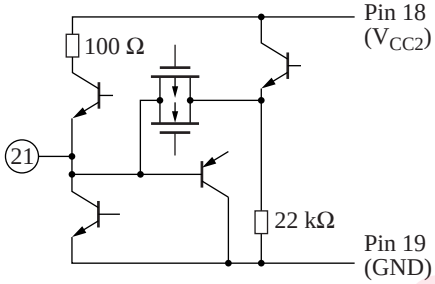
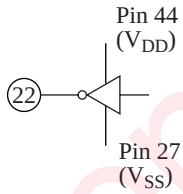
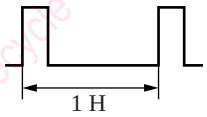
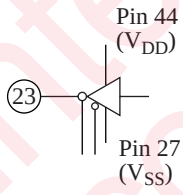
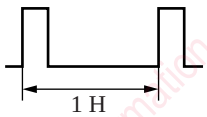
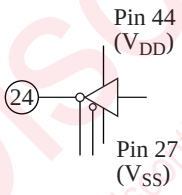
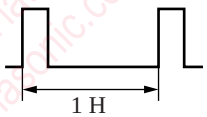
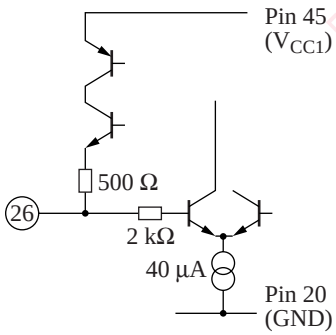
■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
10		COM: Common drive pulse Output pin	
11		B-out: B signal output pin Z_O = approx. 70 Ω	
12		B-det.: Pin for connecting a capacitor for B signal output DC feedback	
13		G-out: G signal output pin Z_O = approx. 70 Ω	
14		G-det.: Pin for connecting a capacitor for G signal output DC feedback	

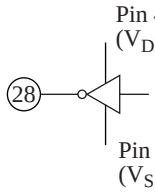
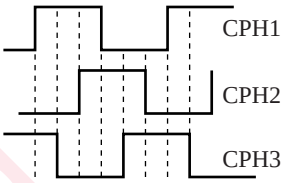
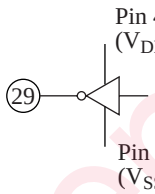
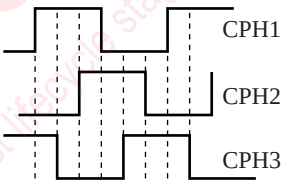
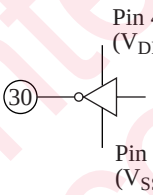
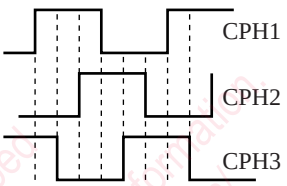
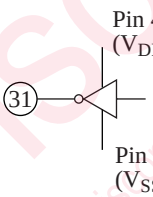
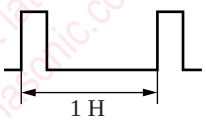
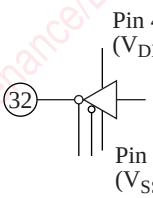
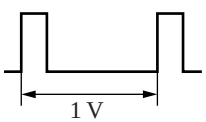
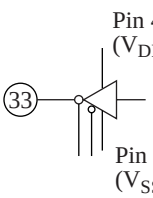
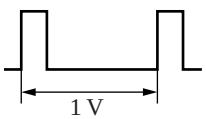
■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
15		V-center: Chroma signal output center voltage pin	
16		R-det.: Pin for connecting a capacitor for R signal output DC feedback	
17		R-out: R signal output pin Z_O = approx. 70 Ω	
18	—	V_{CC2}: Power supply pin (7 V) for chroma signal driver Supply current: 4.4 mA typ.	—
19	—	GND2: Grounding pin (0 V) for chroma signal driver system	—
20	—	GND1: Grounding pin (0 V) for chroma signal processing system	—

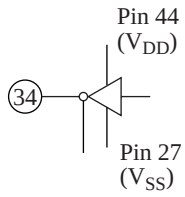
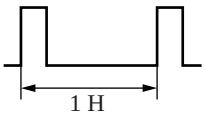
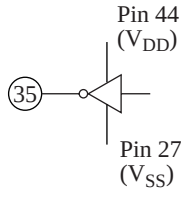
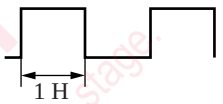
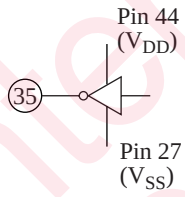
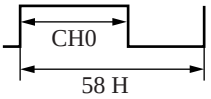
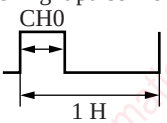
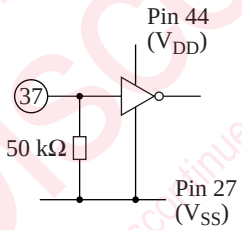
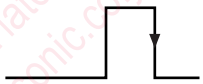
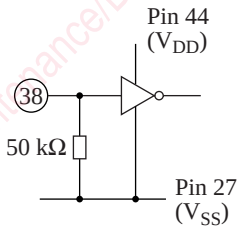
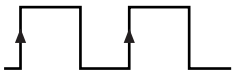
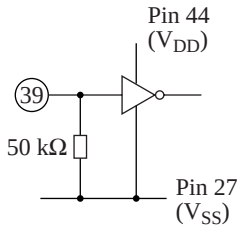
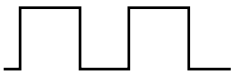
■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
21		AFC: Horizontal AFC loop filter connection pin	DC
22		OEH: Horizontal driver enable pulse output pin CMOS output	
23		STH2: Horizontal display start pulse 2 output pin TInv output	
24		STH1 Horizontal display start pulse 1 output pin TInv output	
25	—	V_{CC3} Power supply pin for clock driver 3 V typ.	—
26		f_O VCO free-running adjustment pin Pin voltage fluctuates with CH3 data value	DC

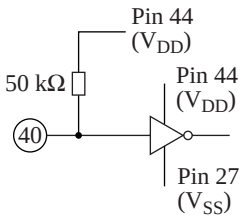
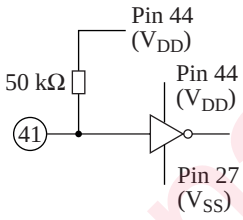
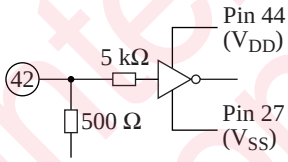
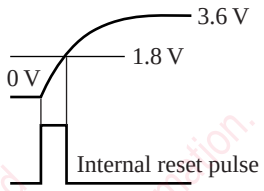
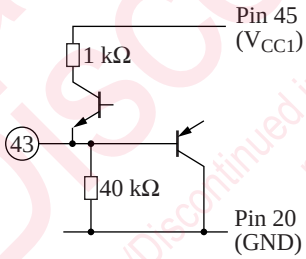
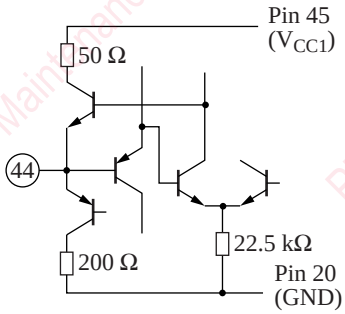
■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
27	—	V_{SS} Logic block grounding pin (0 V)	—
28		CPH3 Horizontal shift clock 3 output pin CMOS output	
29		CPH2 Horizontal shift clock 2 output pin CMOS output	
30		CPH1 Horizontal shift clock 1 output pin CMOS output	
31		OEV Gate driver enable pulse output pin CMOS output	
32		STV2 Vertical display start pulse 2 output pin TInv output	
33		STV1 Vertical display start pulse 1 output pin TInv output	

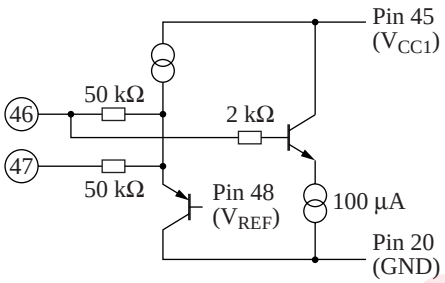
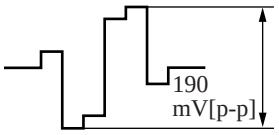
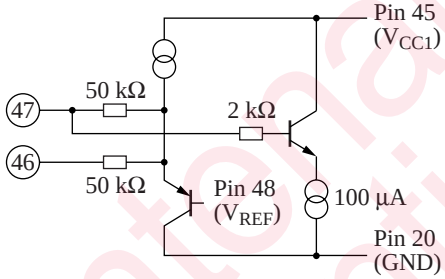
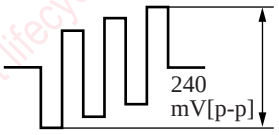
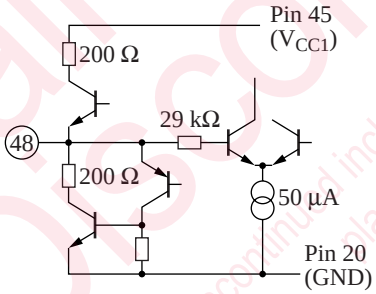
■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
34		CPV Vertical shift clock output pin TInv output	
35		QH Arrangement changeover signal output pin CMOS output	
36		PWM Back light pulse output pin CMOS output	PWM mode  Back light pulse mode 
37		Load Serial data write pulse input pin CMOS input (50 kΩ pull-down)	
38		SCLK Serial data Shift clock input pin CMOS input (50 kΩ pull-down)	
39		Data Serial data Data input pin CMOS input (50 kΩ pull-down)	

■ Terminal Equivalent Circuits (continued)

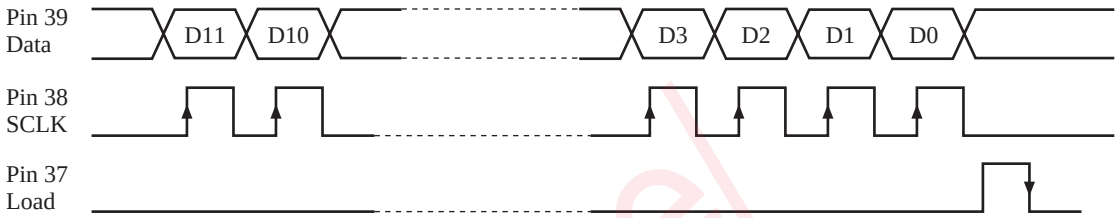
PinNo.	Equivalent circuit	Description	Signal waveform
40		HMC Right and left reversing control signal input pin CMOS input (50 kΩ pull-up)	High or Low
41		QHSEL Upper and lower reversing control signal input pin CMOS input (50 kΩ pull-up)	High or Low
42		STUP Control signal output inhibit control pin	
43		DACMON DAC output voltage monitor pin	—
44		V_{DD} Power generating circuit for internal logic processing Bypass capacitor connection pin	DC: 3.6 V
45	—	V_{CC1} Power supply pin (4.8 V) for chroma signal processing Supply current 21 mA typ.	—

■ Terminal Equivalent Circuits (continued)

PinNo.	Equivalent circuit	Description	Signal waveform
46		R–Y Input R–Y signal	Input waveform 
47		B–Y Input B–Y signal	Input waveform 
48		V_{REF} Reference voltage circuit for chroma signal processing Bypass capacitor connection pin	DC: 2 V

■ Technical Information

1. Serial data input timing chart



The shift data clock should be entered at a frequency of 1 MHz of less.

2. Serial data format

MSB

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D0 to D7: Data part (EVR control bit)
D8 to D11: Data part (EVR selection bit)

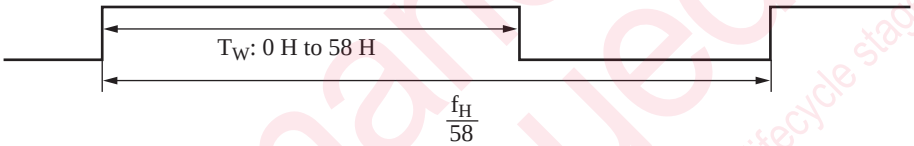
D8	D9	D10	D11	Selection ch.	EVR control function
0	0	0	0	0	Back light pulse
0	0	0	1	1	Horizontal display position
0	0	1	0	2	Vertical display position
0	0	1	1	3	VCO free-running
0	1	0	0	4	OSD white level
0	1	0	1	5	Aperture (Note: The data part should be used within the range of "02" to"FF".)
0	1	1	0	6	Color gain
0	1	1	1	7	Gamma 1-knee level
1	0	0	0	8	Gamma 2-knee level
1	0	0	1	9	Black limiter
1	0	1	0	10	Contrast
1	0	1	1	11	White peak limiter
1	1	0	0	12	R-ch. sub-brightness
1	1	0	1	13	B-ch. sub-brightness
1	1	1	0	14	Common amplitude
1	1	1	1	15	Brightness

■ Technical Information (continued)

3. CH0: Back light pulse width

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	NTEST0	CPWM	BL5	BL4	BL3	BL2	BL1	BL0
					0	PWM output					
					1	Back light pulse output					
				0	Inspection mode						
				1	Normal using mode						

1) D6 = "0": PWM mode



The adjustment characteristic becomes a discontinuity near max. duty cycle.

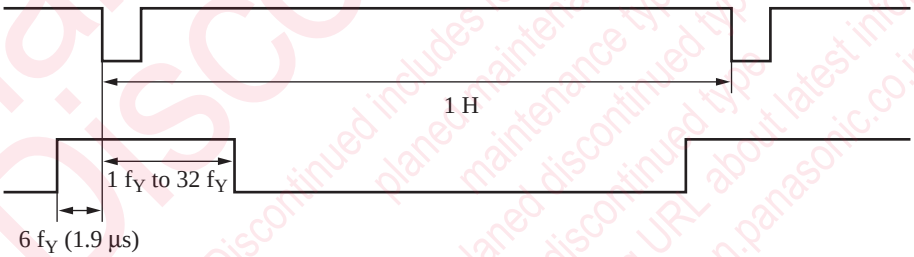
(D5, D4, D3, D2, D1, D0) = (000000): t_W = 1 H

(110111): t_W = 56 H

(111000): t_W = 0 H

(111001) to (111111) : t_W = 58 H

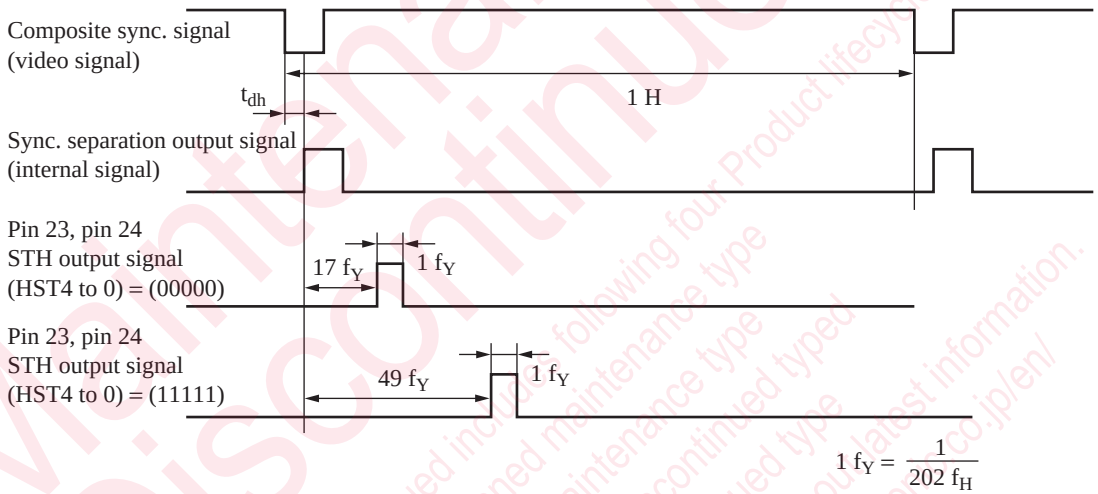
2) D6 = "1": Back light pulse mode



■ Technical Information (continued)

4. CH1: Horizontal display position adjustment

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				DCST	NOSHIFT	CPHSEL	HST4	HST3	HST2	HST1	HST0
						0	Half shift normal				
						1	Half shift reverse (odd number / even number line)				
1	0	0	0		0	Half shift present					
					1	Half shift not present					
				0	Controller stop mode						
				1	Normal using mode						



$$1\ f_Y = \frac{1}{202\ f_H}$$

The STH signal output adjustment range has been designed using the composite sync. signal input to pin 1 (horizontal sync. signal) as the reference point. The delay time of the video signal and the sync. separation output (t_{dh}) varies slightly depending on the constant of external filter to be attached to the sync. signal input block.

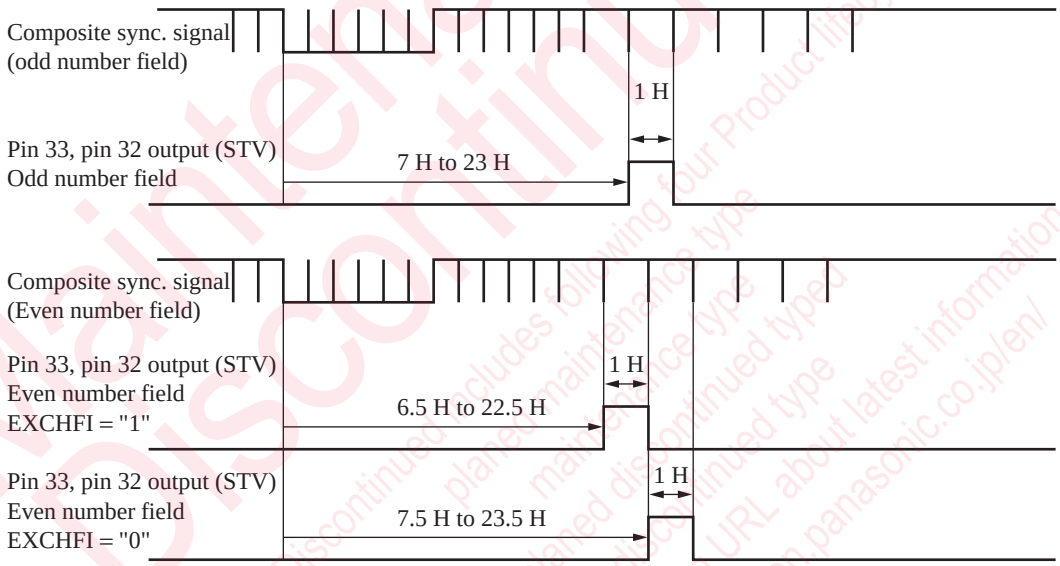
About the external constant, it is necessary to determine it after evaluating the characteristics for the special play back mode.

Note) In the case of serial variable of STH, the left side of the rear edges of CPV and OEH are interlocked with these rear edges.

■ Technical Information (continued)

5. CH2: Vertical display position adjustment

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				NHST	EXCHFI	CFRP	QMODE	VST3	VST2	VST1	VST0
							0	Normal operation			
							1	QH polarity reverse			
						0	Normal operation				
0	1	0	0			1	Internal POL polarity reverse				
					0	Even number field phase advance					
					1	Odd number field phase advance					
				0	H reverse inhibit mode						
				1	Normal operation						



The controller output gives the following output of fixed potential in the case of D6 (CST) = "0" or pin 42 is "L".

Output voltage(V)	Pin name
"H"(V_{CC3})	OEV
"L"(GND)	CPH1, CPH2, CPH3, STH1(STH2), STV1(STV2), CPV, QEH, QH

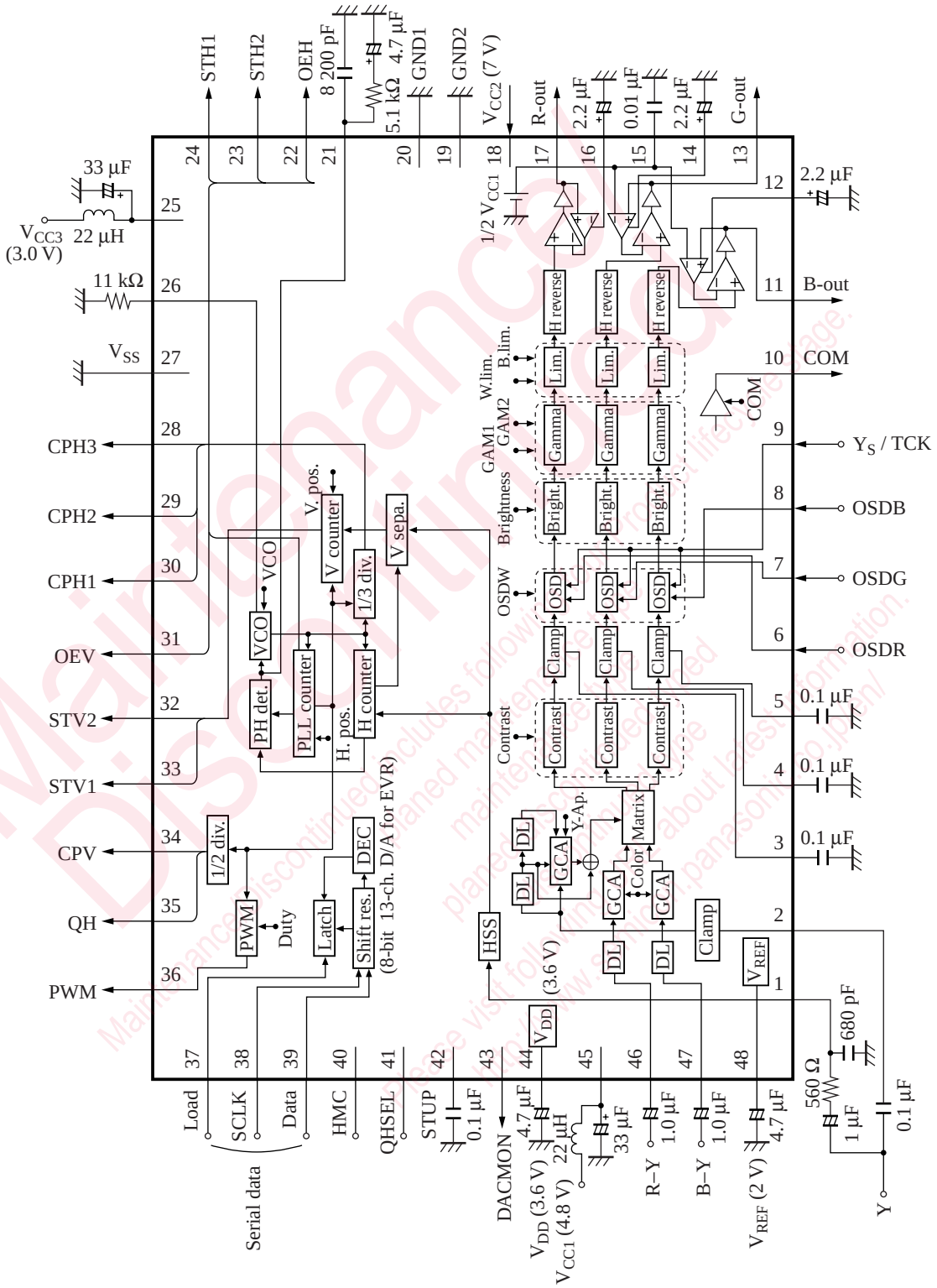
Noes) 1: In the case of serial variation of STV, it changes by 2H for only between D3 to D0 = 0000 and D3 to D0 = 0001.
2: The selection of EXCHFI = "1" / "0" in STV is fixed at "0".

■ Usage Notes

- Give consideration so as to provide the supply voltage to pin 18, pin 25 and pin 45 simultaneously.
- Be careful because the following pins are weak against surge voltage.

Pin 9 surge voltage: +200 V
–200 V
Pin 17 surge voltage: +180 V
–180 V

■ Application Circuit Example



Note) The above values are the typical values, so that it is necessary to give a consideration to the relation with set equipment at setting.

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