Standard Products

UT8R128K32 128K x 32 SRAM

Advanced Data Sheet

May 29, 2003

FEATURES

- 15ns maximum access time
- Asynchronous operation, functionally compatible with industry-standard 128K x 32 SRAMs
- CMOS compatible inputs and output levels, three-state bidirectional data bus
  - I/O Voltage 3.3 volts, 1.8 volt core
- Radiation performance
  - Total-dose: 100K rad(Si)
  - SEL Immune >100 MeV-cm^2/mg
  - Onset LET > TBD
  - Memory Cell Saturated Cross Section: TBD
  - Neutron Fluence: 3.0E14n/cm^2
  - Dose Rate (estimated)
    - Upset 1.0E9 rad(Si)/sec
    - Latchup >1.0E11 rad(Si)/sec
- Packaging options:
  - 68-lead ceramic quad flatpack
- Standard Microcircuit Drawing 5962-03236
  - QML compliant part

INTRODUCTION

The UT8R128K32 is a high-performance CMOS static RAM organized as 131,072 words by 32 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected**.**

Writing to the device is accomplished by taking chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A16). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).

IN DEVELOPMENT

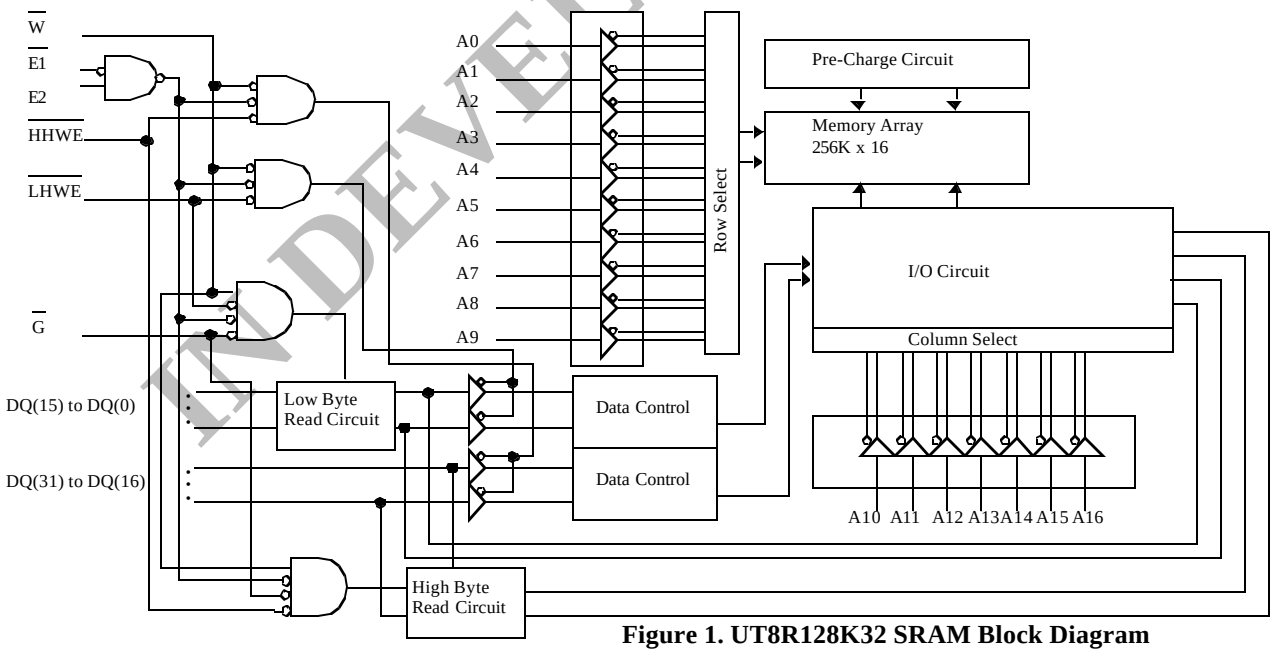


Figure 1. UT8R128K32 SRAM Block Diagram

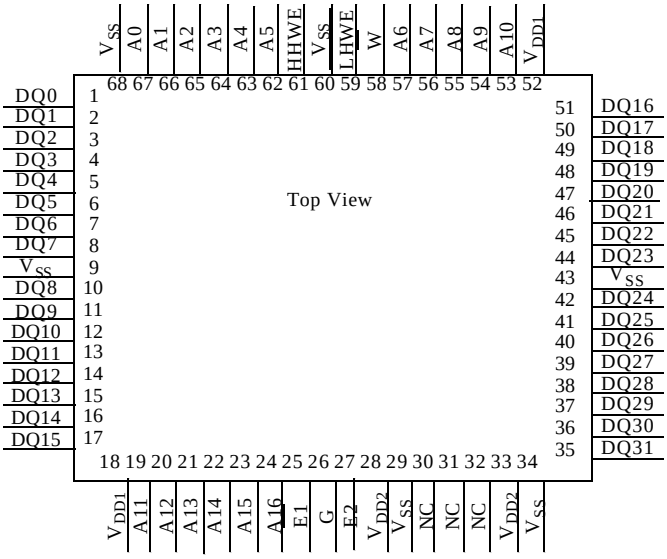


Figure 2. 15ns SRAM Pinout (68)

PIN NAMES

A(16:0)	Address	$\overline{W}$	Write Enable
DQ(31:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E1}$	Enable (Active Low)	V_{DD1}	Power (1.8V)
E2	Enable (Active High)	V_{DD2}	Power (3.3V)
$\overline{HHWE}$ LWHE	High half-word enable Low half-word enable	V_{SS}	Ground

DEVICE OPERATION

The UT8R128K32 has six control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), Half-word Enables ($\overline{HHWE}$/$\overline{LHWE}$) and Output Enable ($\overline{G}$); 17 address inputs, A(16:0); and 32 bidirectional data lines, DQ(15:0). $\overline{E1}$ and E2 device enables control device selection, active, and standby modes. Asserting $\overline{E1}$ and E2 enables the device, causes I_{DD} to rise to its active value, and decodes the 17 address inputs to select one of 131,072 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	E2	$\overline{E1}$	$\overline{LHWE}$	$\overline{HHWE}$	I/O Mode	Mode
X	X	X	H	X	X	DQ(31:16) 3-State DQ(15:0) 3-State	Standby
X	X	L	X	X	X	DQ(31:16) 3-State DQ(15:0) 3-State	Standby
L	H	H	L	L	H	DQ(31:16) 3-State DQ(15:0) Data Out	Low Half-Word Read
L	H	H	L	H	L	DQ(31:16) Data Out DQ(15:0) 3-State	High Half-Word Read
L	H	H	L	L	L	DQ(31:16) Data Out DQ(15:0) Data Out	Word Read
X	L	H	L	L	L	DQ(31:16) Data In DQ(15:0) Data In	Word Write
X	L	H	L	L	H	DQ(31:16) 3-State DQ(15:0) Data In	Low Half-Word Write
X	L	H	L	H	L	DQ(31:16) Data In DQ(15:0) 3-State	High Half-Word Write
H	H	H	L	X	X	DQ(31:16) DQ(15:0) All 3-State	3-State
X	X	H	L	H	H	DQ(31:16) DQ(15:0) All 3-State	3-State

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

IN DEVELOPMENT

READ CYCLE

A combination of $\overline{W}$ and E2 greater than V_{IH} (min) and $\overline{E1}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(31:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by the latter of $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 32-bit word addressed by A(16:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

Write Cycle

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL} (max) and E2 greater than V_{IH} (min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH} (min), or when $\overline{W}$ is less than V_{IL} (max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait user must wait t_{WLQZ} before applying data to the 32 bidirectional pins DQ(15:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by either $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the sixteen bidirectional pins DQ(31:0) to avoid bus contention.

WORD ENABLES

Separate byte enable controls ($\overline{LHWE}$ and $\overline{HHWE}$) allow individual bytes to be accessed. $\overline{LHWE}$ controls the lower bits DQ(15:0). $\overline{HHWE}$ controls the upper bits DQ(31:16). Writing to the device is performed by asserting $\overline{E1}$, E2 and the byte enables. Reading the device is performed by asserting $\overline{E1}$, E2, $\overline{G}$, and the byte enables while $\overline{W}$ is held inactive (HIGH).

$\overline{HHWE}$	$\overline{LHWE}$	OPERATION
0	0	32-bit read or write cycle
0	1	16-bit high half-word read or write cycle (low byte bi-direction pins DQ(15:0) are in 3 -state)
1	0	32-bit low half-word read or write cycle (high half word bi-direction pins DQ(31:16) are in 3 -state)
1	1	High and Low byte bi-directional pins remain in 3-state, write function disabled

RADIATION HARDNESS

The UT8R128K32 SRAM incorporates special design, layout, and process features which allows operation in a limited radiation environment.

Table 2. Radiation Hardness Design Specifications[1]

Total Dose	100K	rad(Si)
Heavy Ion Error Rate[2]	TBD	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles of 128MeV-cm^2/mg.
2. 10% worst case particle environment, Geosynchronous orbit, 0.025 mils of Aluminum.

Supply Sequencing

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

IN DEVELOPMENT

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage	-0.3 to 2.0V
V_{DD2}	DC supply voltage	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[2]	5°C/W
I_I	DC input current	±5 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	Positive supply voltage	1.7 to 1.9V
V_{DD2}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	(C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

IN DEVELOPMENT

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		.7*V_{DD2}		V
V_{IL}	Low-level input voltage			.3*V_{DD2}	V
V_{OL}	Low-level output voltage	I_{OL} = 8mA, V_{DD2} = V_{DD2} (min)		.2*V_{DD2}	V
V_{OH}	High-level output voltage	I_{OH} = -4mA, V_{DD2} = V_{DD2} (min)	.8*V_{DD2}		V
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V		7	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz @ 0V		7	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}	-2	2	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD2} and V_{SS} V_{DD2} = V_{DD2} (max), $\overline{G}$ = V_{DD2} (max)	-2	2	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}	-100	+100	mA
$I_{DD1}(OP_1)$	V_{DD1} Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V , I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		15	mA
$I_{DD1}(OP_2)$	V_{DD1} Supply current operating @ 66MHz,	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		85	mA
$I_{DD2}(OP_1)$	V_{DD2} Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V , I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		1	mA
$I_{DD2}(OP_2)$	V_{DD2} Supply current operating @ 66MHz,	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		12	mA
$I_{DD1}(SB)$[4]	Supply current standby @ 0Hz	CMOS inputs , I_{OUT} = 0 $\overline{E1}$ = V_{DD2} -0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		11	mA
$I_{DD2}(SB)$[4]				100	µA
$I_{DD1}(SB)$[4]	Supply current standby A(16:0) @ 66MHz	CMOS inputs , I_{OUT} = 0 $\overline{E1}$ = V_{DD2} - 0.2, E2 = GND, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		11	mA
$I_{DD2}(SB)$[4]				100	µA

IN DEVELOPMENT

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E5 rad(Si).

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. V_{IH} = V_{DD2} (max), V_{IL} = 0V.

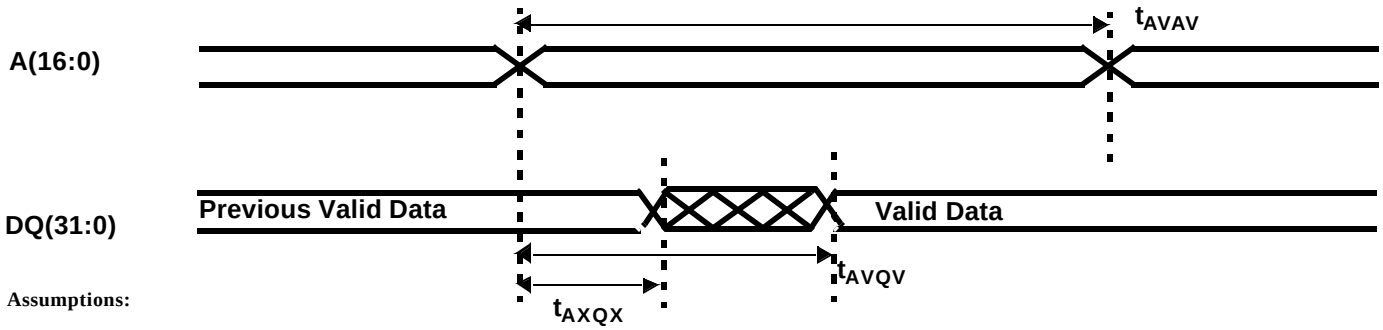
AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

SYMBOL	PARAMETER	8R128K32-15		UNIT
		MIN	MAX	
t_{AVAV}[1]	Read cycle time	15		ns
t_{AVQV}	Address to data valid		15	ns
t_{AXQX}[2]	Output hold time from address change	3		ns
t_{GLQX}[2,1]	$\overline{G}$-controlled output enable time	0		ns
t_{GLQV}	$\overline{G}$-controlled output data valid		7	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		7	ns
t_{ETQX}[2,3]	E-controlled output enable time	5		ns
t_{ETQV}[3]	E-controlled access time		15	ns
t_{EFQZ}[4]	E-controlled output three-state time[2]		7	ns
t_{BLQX}[1]	$\overline{LHWE}$, $\overline{HHWE}$ Enable to Output in Low-Z	0		ns
t_{BHQZ}	$\overline{LHWE}$, $\overline{HHWE}$ Enable to Output in High-Z		7	ns
t_{BLQV}	$\overline{LHWE}$, $\overline{HHWE}$ Enable to data valid		10	ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Guaranteed but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2.
4. The EF (enable false) notation refers to the latter rising edge of E1 or falling edge of E2.

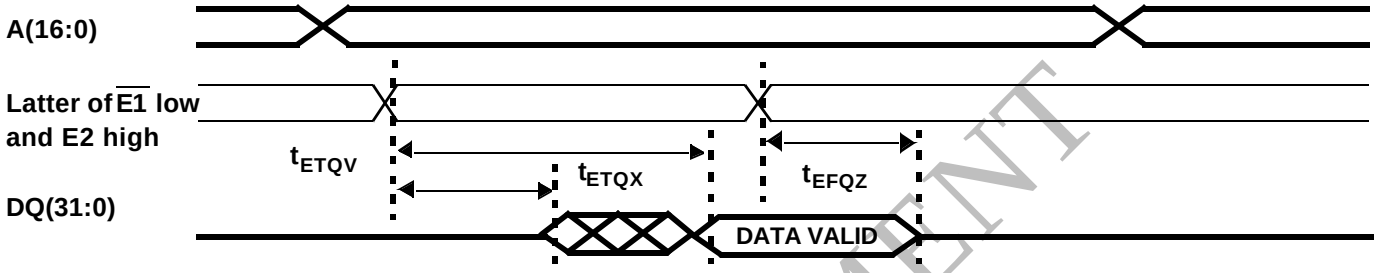
IN DEVELOPMENT



Assumptions:

1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)

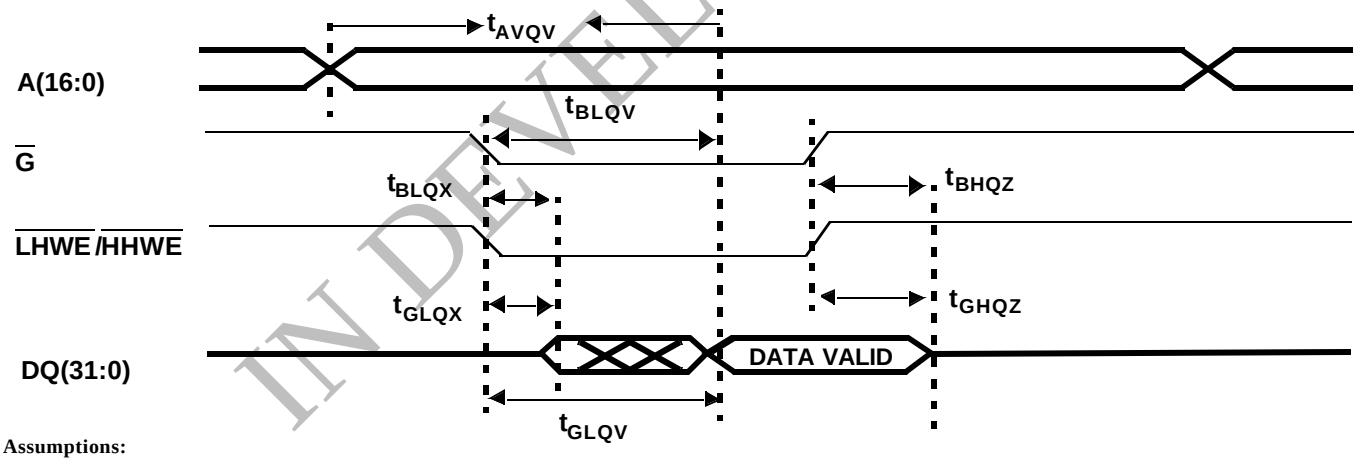
Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:

1. $\overline{G}$, $\overline{HHWE}$, $\overline{LHWE} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:

1. $\overline{E1} \leq V_{IL}$ (max) , E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

IN DEVELOPMENT

AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

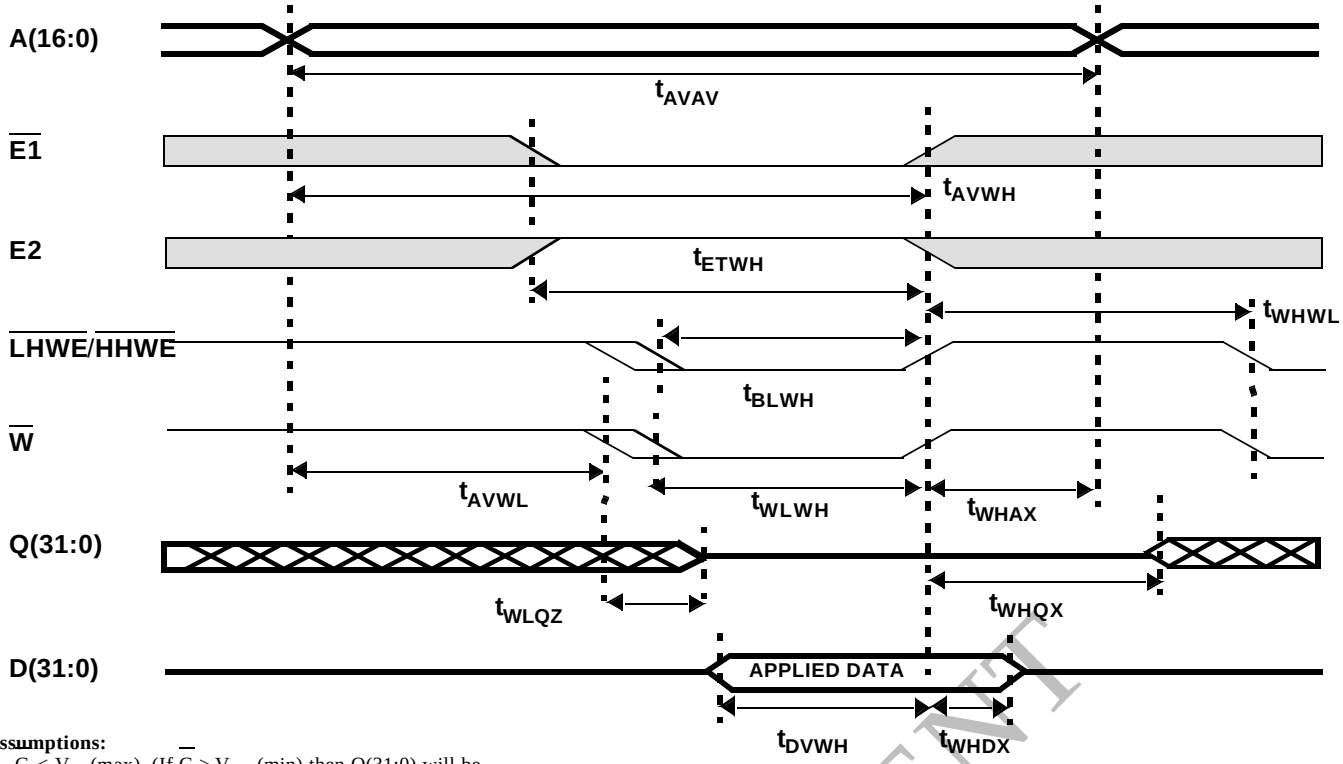
SYMBOL	PARAMETER	8R128K32-15		UNIT
		MIN	MAX	
t_{AVAV}[1]	Write cycle time	15		ns
t_{ETWH}	Device enable to end of write	12		ns
t_{AVET}	Address setup time for write ($\overline{E1}$/E2- controlled)	0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	1		ns
t_{WLWH}	Write pulse width	12		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	2		ns
t_{EFAX}	Address hold time for device enable ($\overline{E1}$/E2- controlled)	0		ns
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		5	ns
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	4		ns
t_{ETEF}	Device enable pulse width ($\overline{E1}$/E2 - controlled)	12		ns
t_{DVWH}	Data setup time	7		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Device enable controlled write pulse width	12		ns
t_{DVEF}	Data setup time	7		ns
t_{EFDX}	Data hold time	0		ns
t_{AVWH}	Address valid to end of write	12		ns
t_{WHWL}	Write disable time	3		ns
t_{BLWH}	$\overline{LHWE}$, $\overline{HHWE}$ low to write high	12		ns
t_{BLEF}	$\overline{LHWE}$, $\overline{HHWE}$ low to enable high	12		ns

Notes :

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Tested with G high.
2. Three-state is defined as 200mV change from steady-state output voltage.

IN DEVELOPMENT

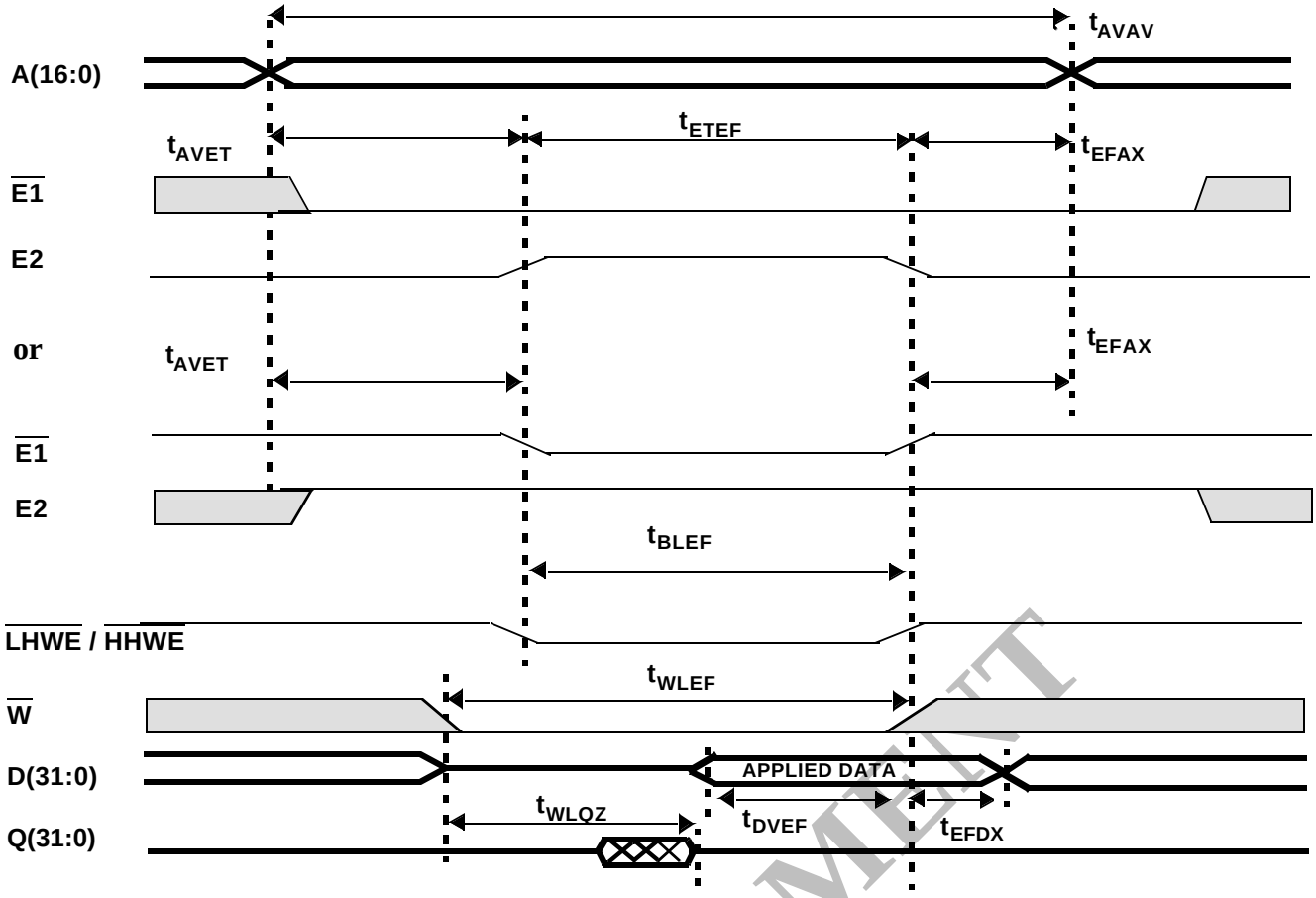


Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) will be in three-state for the entire cycle.)

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access

IN DEVELOPMENT



Assumptions & Notes:

1. $G \leq V_{IL}$ (max). (If $G \geq V_{IH}$ (min) then Q(31:0) will be in three-state for the entire cycle.)
2. Either E1 / E2 scenario can occur.

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access

IN DEVELOPMENT

DATA RETENTION CHARACTERISTICS (Pre and Post-Radiation)
(V_{DD2} = V_{DD2} (min), 1 Sec DR Pulse)

SYMBOL	PARAMETER		MINIMUM	MAXIMUM	UNIT
V_{DR}	V_{DD1} for data retention		1.0		V
I_{DDR} [1]	Data retention current	-55°C		600	µA
		25°C		600	µA
		125°C		12	mA
t_{EFR} [1,2]	Chip deselect to data retention time		0		ns
t_R [1,2]	Operation recovery time		t_{AVAV}		ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. E1 = V_{DD2} or E2 = V_{SS} all other inputs = V_{DD2} or V_{SS}
2. V_{DD2} = 0 volts to V_{DD2} (max)

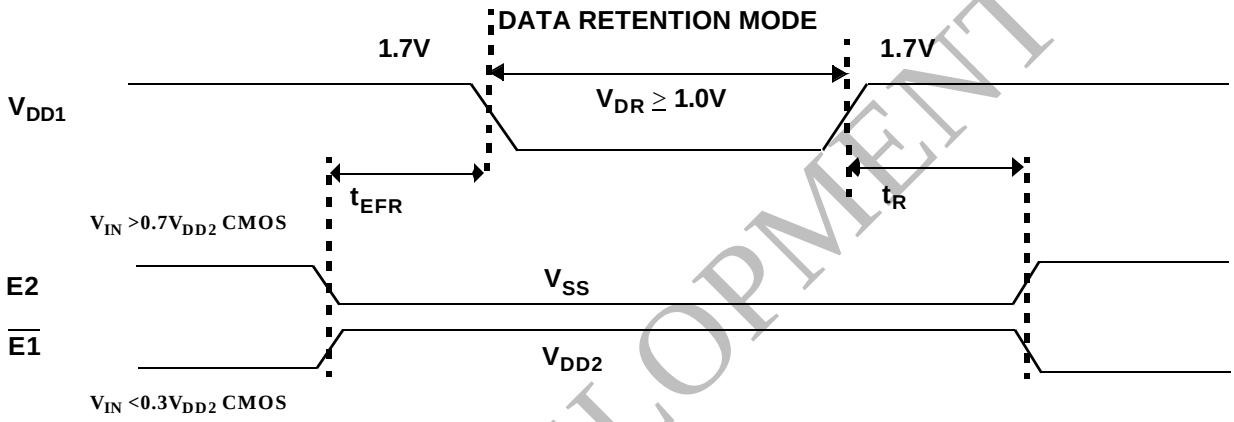
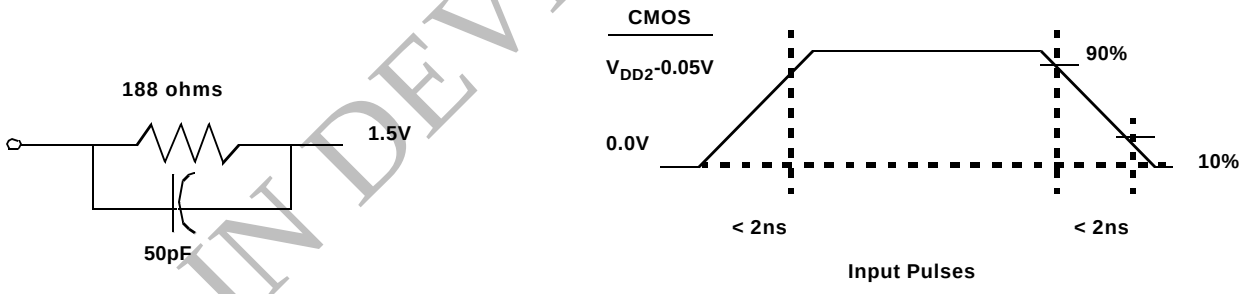


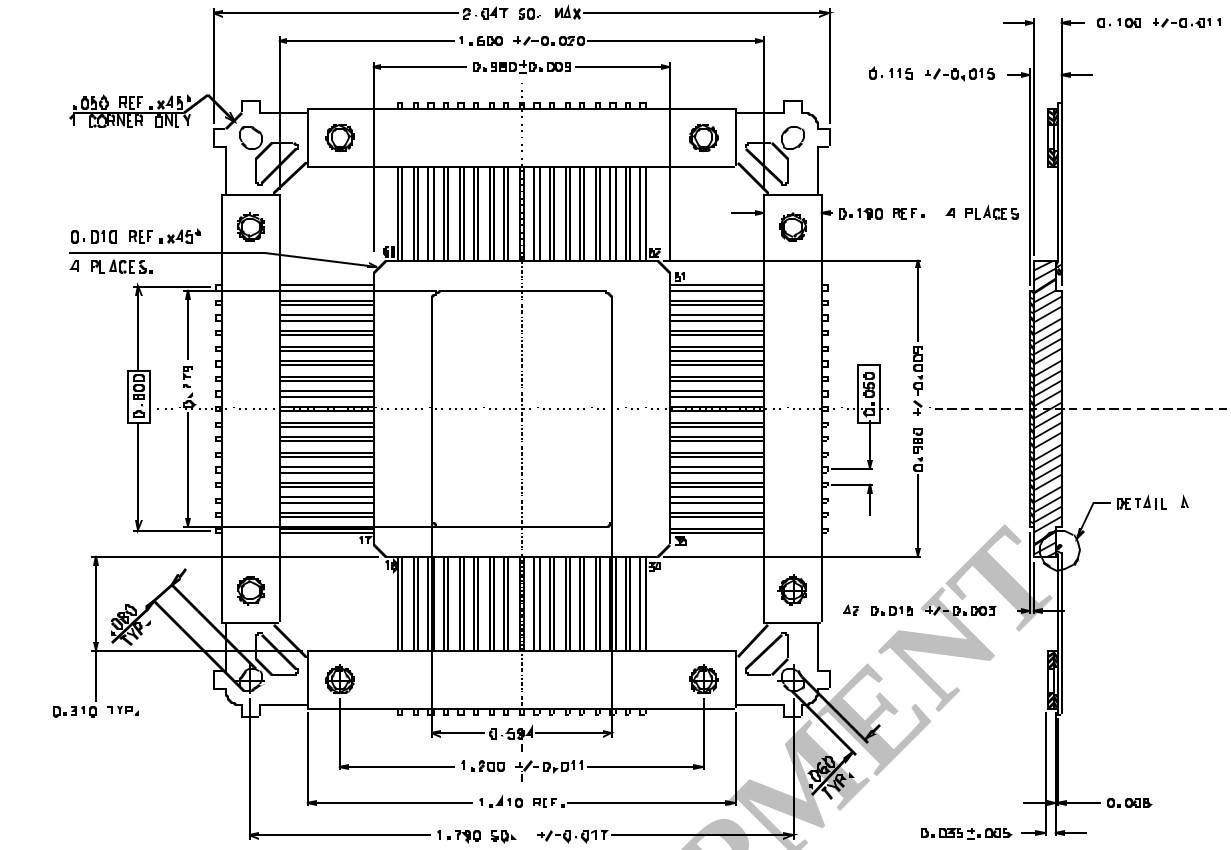
Figure 5. Low V_{DD} Data Retention Waveform



Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD2}/2).

Figure 6. AC Test Loads and Input Waveforms

IN DEVELOPMENT



Notes:

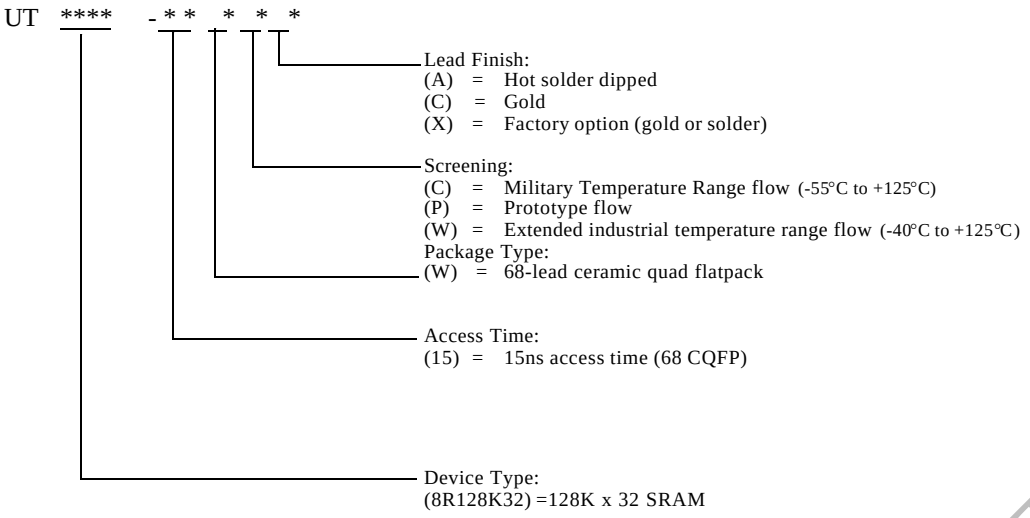
1. All exposed metallized areas are gold plated over nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.

Figure 7. 68-Lead Ceramic Quad Flatpack

IN DEVELOPMENT

ORDERING INFORMATION

128K x 32 SRAM

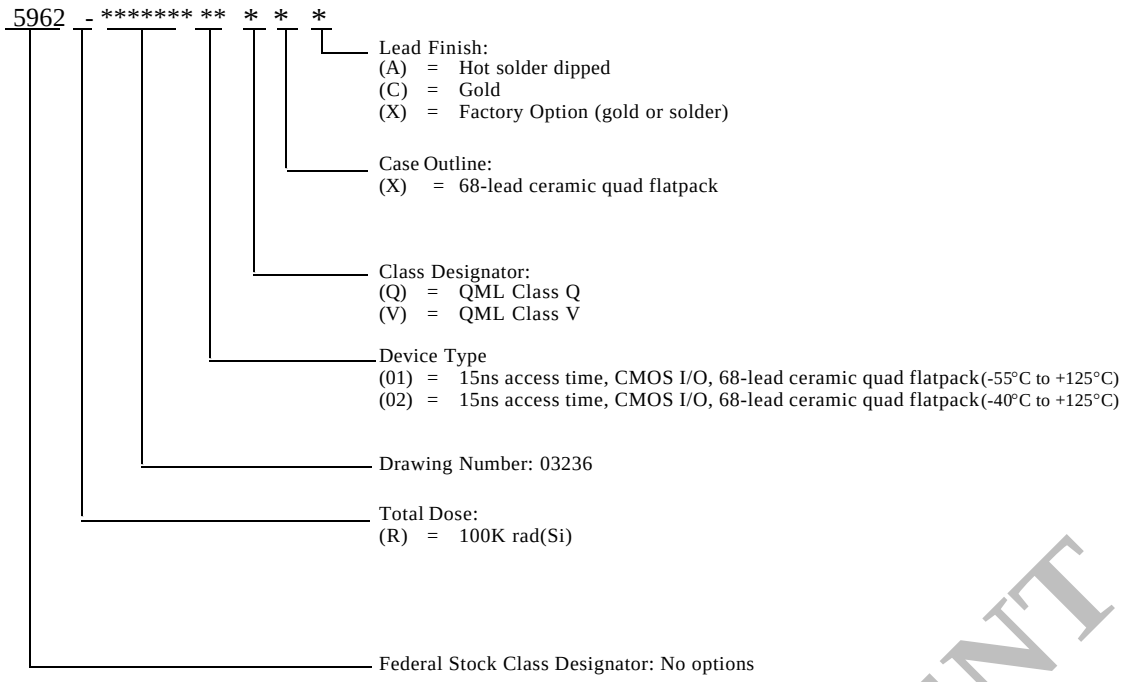


IN DEVELOPMENT

Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

128K x 32 SRAM: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

IN DEVELOPMENT