STL50N25N3LLH5

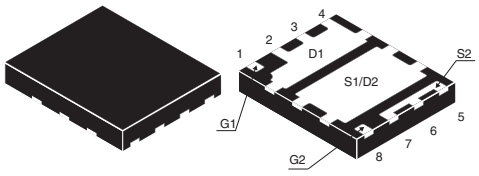
Dual N-channel 30 V, 0.006 Ω typ., 14.6 A PowerFLAT™ STripFET™ V Power MOSFET in 5x6 asymmetrical double island package

Datasheet — preliminary data

Features

Order code		V_{DSS}	$R_{DS(on)}$ max.	I_D
STL50N25N3LLH5	Q_1	30 V	< 0.0135 Ω	12 A
	Q_2	30 V	< 0.0071 Ω	14.6 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



PowerFLAT™5x6 asymmetrical double island

Applications

- Switching applications

Description

This device is a dual N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

Figure 1. Internal schematic diagram

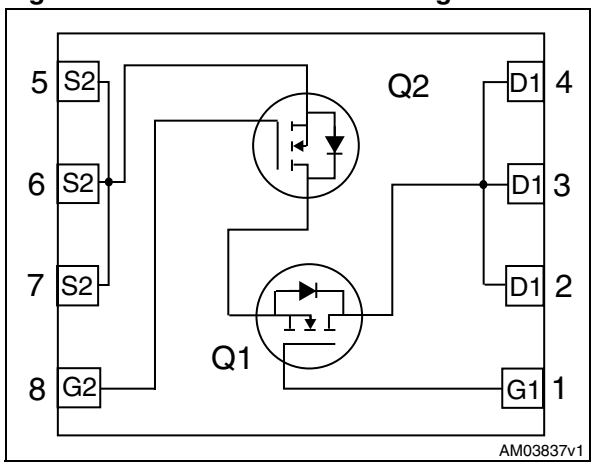


Table 1. Device summary

Order code	Marking	Package	Packaging
STL50N25N3LLH5	50N25N3LLH5	PowerFLAT™5x6 asymmetrical double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Type	Value	Unit
V_{DS}	Drain-source voltage	Q_1 Q_2	30 30	V V
V_{GS}	Gate- source voltage	Q_1 Q_2	± 20 ± 20	V V
I_D(1)	Drain current (continuous) at T_C = 25°C	Q_1 Q_2	25 50	A A
I_D(1)	Drain current (continuous) at T_C = 100°C	Q_1 Q_2	15.6 33	A A
I_D(2)	Drain current (continuous) at T_C = 25°C	Q_1 Q_2	12 14.6	A A
I_D(2)	Drain current (continuous) at T_C = 100°C	Q_1 Q_2	7.5 9.1	A A
I_{DM} (3)	Drain current (pulsed)	Q_1 Q_2	48 58.4	A A
P_{TOT}(1)	Total dissipation at T_C = 25°C	Q_1 Q_2	23 50	W W
P_{TOT}(2)	Total dissipation at T_C = 25°C	Q_1 Q_2	3.12 3.12	W W
E_{AS}(4)	Single pulse avalanche energy		TBD	mJ

1. This value is accordingly $R_{thj\text{-}c}$
2. This value is accordingly $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area
4. Starting T_J = 25 °C, I_D = 7.5 A

Table 3. Thermal data

Symbol	Parameter	Type	Value	Unit
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-ambient max		40	°C/W
$R_{thj\text{-}c}$	Thermal resistance junction-case	Q_1 Q_2	5.5 2.5	°C/W
T_j	Thermal operating junction-ambient		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	Q_1 Q_2	30 30			V V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 30 V	Q_1 Q_2			1 1	µA µA
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} =30 V, T_C= 125 °C	Q_1 Q_2			10 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V	Q_1 Q_2			±100 ±100	nA nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	Q_1 Q_2	1 1			V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 6 A V_{GS} = 10 V, I_D = 7.3 A	Q_1 Q_2		0.0126 0.006	0.0135 0.0071	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 4.5 V, I_D = 6 A V_{GS} = 4.5 V, I_D = 7.3 A	Q_1 Q_2		0.0166 0.0072	0.0175 0.008	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	Q_1 Q_2	-	724 1500	-	pF pF
C_{oss}	Output capacitance		Q_1 Q_2	-	132 295	-	pF pF
C_{rss}	Reverse transfer capacitance		Q_1 Q_2	-	20 39	-	pF pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 12 A, V_{GS} = 4.5 V *(see Figure 25)*	Q_1 Q_2	-	5 12	-	nC nC
Q_{gs}	Gate-source charge		Q_1 Q_2	-	2 4	-	nC nC
Q_{gd}	Gate-drain charge		Q_1 Q_2	-	2 4.7	-	nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V, I_D=6 A, R_G=4.7 Ω, V_{GS}= 4.5 V *(see Figure 29)*	Q_1	-	4	-	ns
			Q_2		9.3		ns
t_r	Rise time		Q_1		42		ns
			Q_2		14.5		ns
$t_{d(off)}$	Turn-off delay time		Q_1	-	2.1	-	ns
			Q_2		22.7		ns
t_f	Fall time		Q_1		3.5		ns
			Q_2		4.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	V_{DD}=15 V, I_D=6 A, R_G=4.7 Ω, V_{GS}=4.5 V	Q_1	-		12	A
			Q_2			14.6	A
I_{SDM} (1)	Source-drain current (pulsed)		Q_1	-		48	A
			Q_2			58.4	A
V_{SD} (2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0	Q_1	-		1.1	V
			Q_2			1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, V_{DD} = 15 V, di/dt = 100 A/µs, T_j = 150°C *(see Figure 29)*	Q_1	-	21		ns
			Q_2		25		ns
Q_{rr}	Reverse recovery charge		Q_1		10		nC
			Q_2		17.5		nC
I_{RRM}	Reverse recovery current		Q_1		1.0		A
			Q_2		1.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves) for Q1

Figure 2. Safe operating area

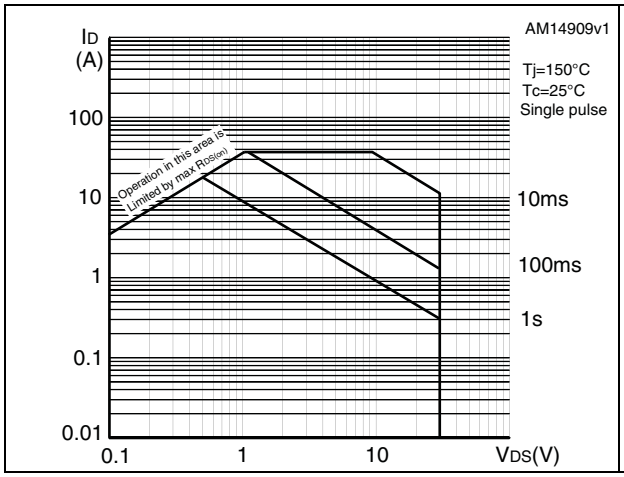


Figure 3. Thermal impedance

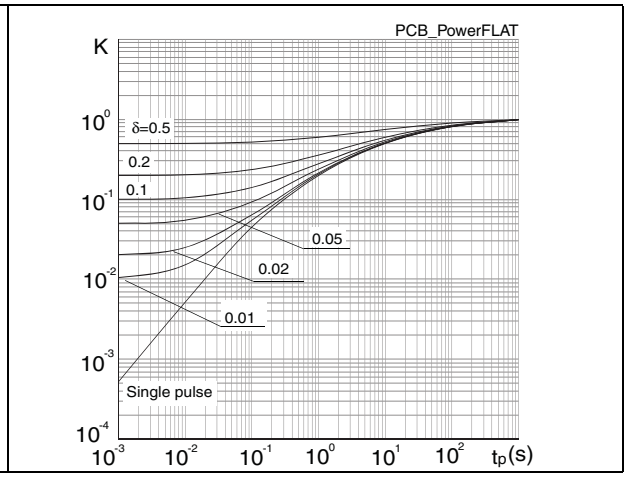


Figure 4. Output characteristics

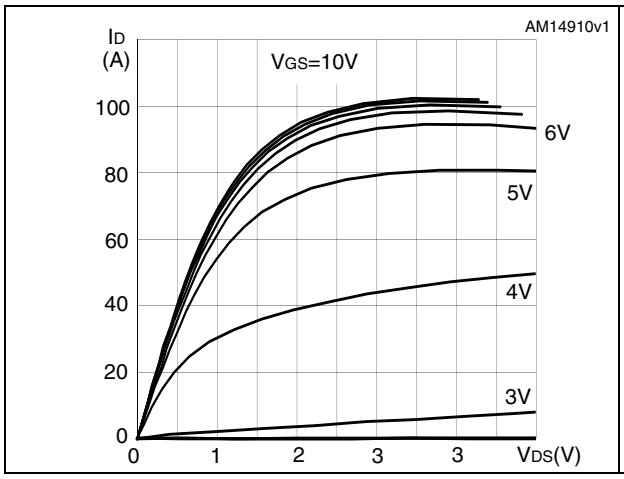


Figure 5. Transfer characteristics

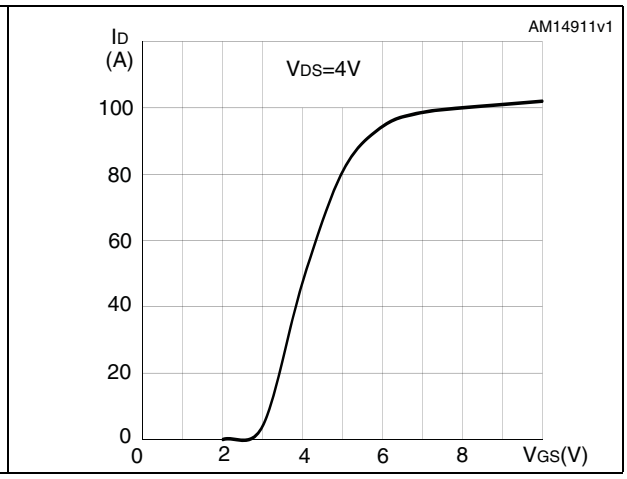


Figure 6. Normalized B_{VDSS} vs temperature

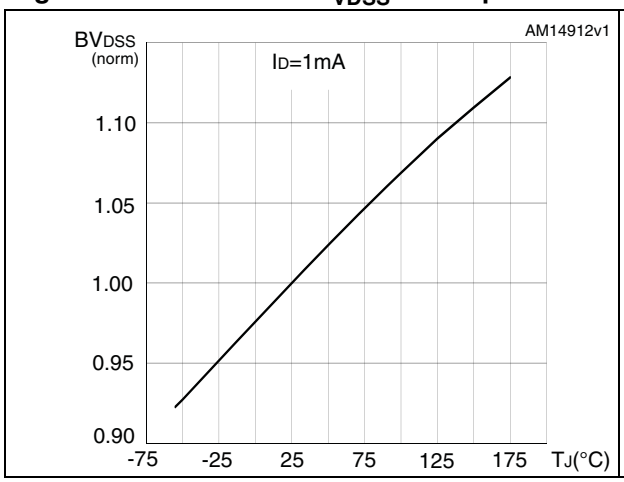


Figure 7. Static drain-source on-resistance

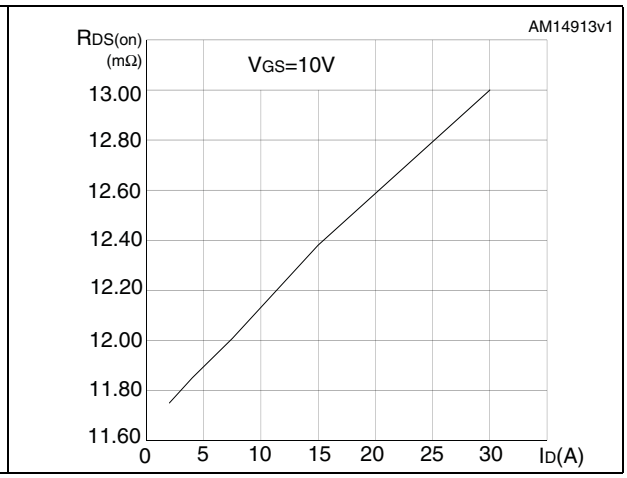


Figure 8. Gate charge vs gate-source voltage

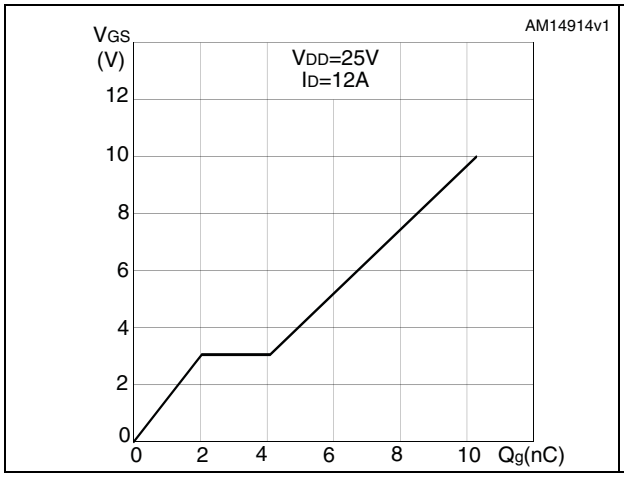


Figure 9. Capacitance variations

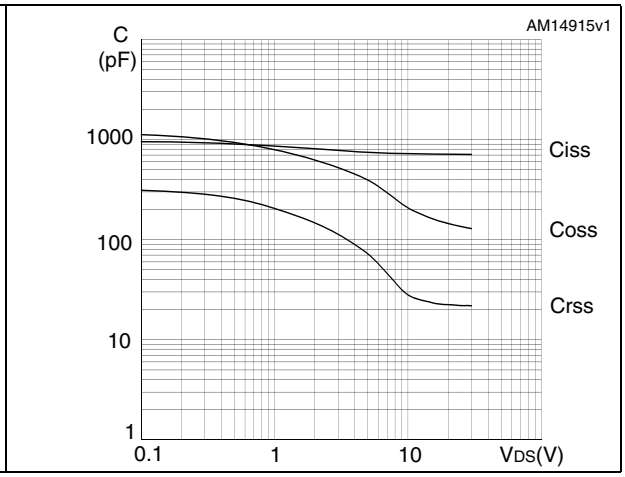


Figure 10. Normalized gate threshold voltage vs temperature

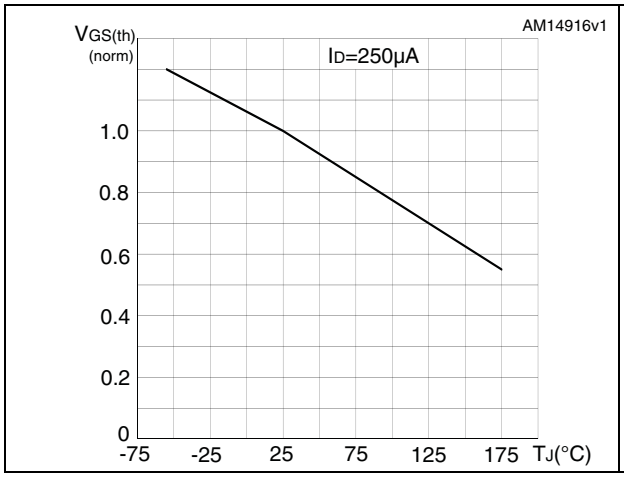


Figure 11. Normalized on-resistance vs temperature

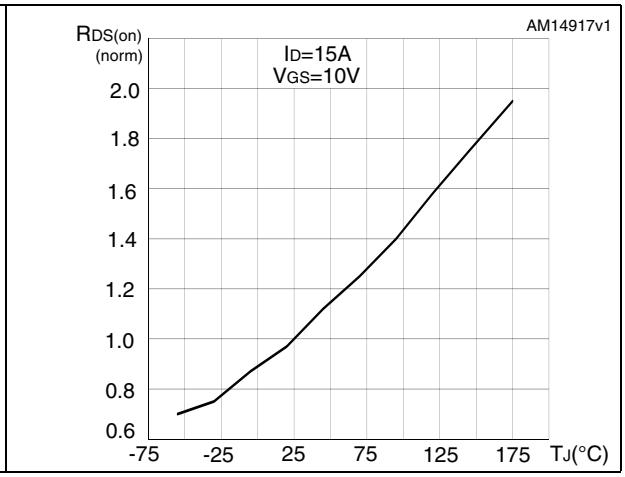
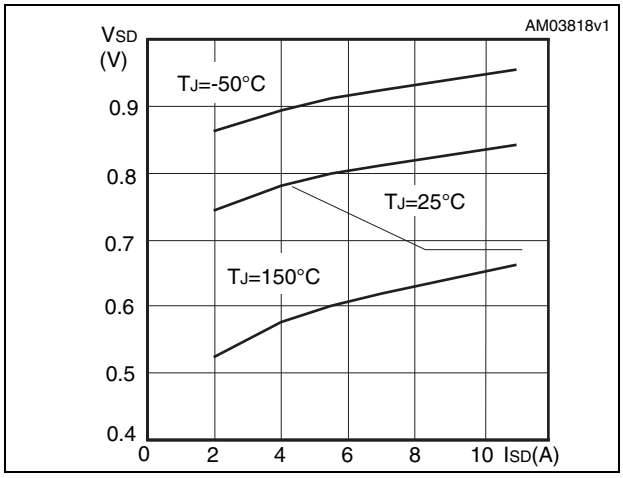


Figure 12. Source-drain diode forward characteristics



2.2 Electrical characteristics (curves) for Q2

Figure 13. Safe operating area

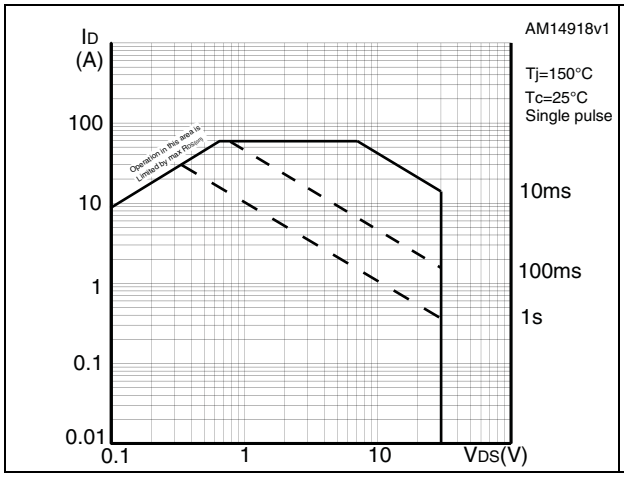


Figure 14. Thermal impedance

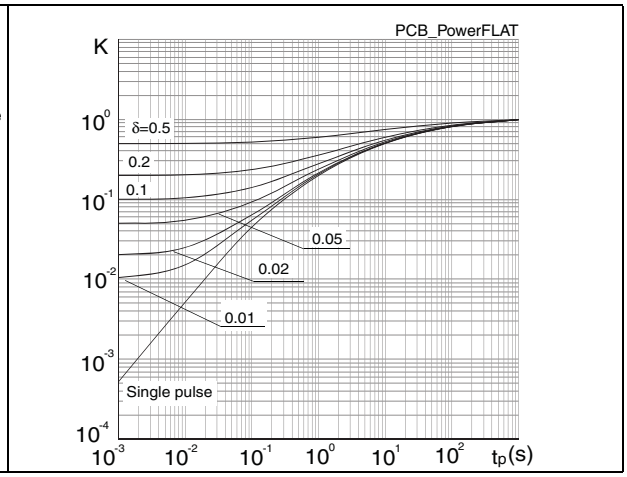


Figure 15. Output characteristics

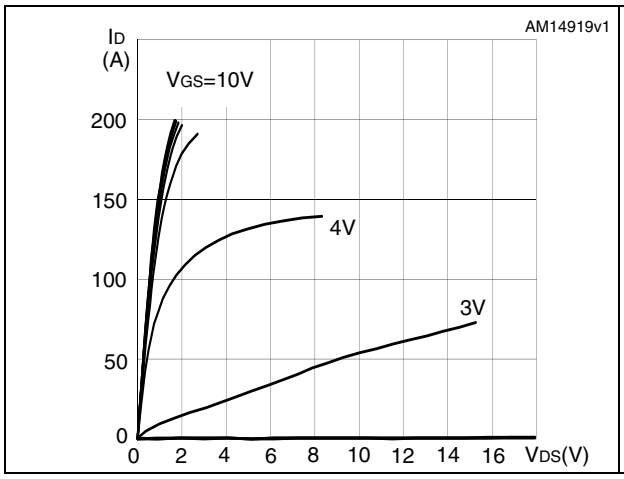


Figure 16. Transfer characteristics

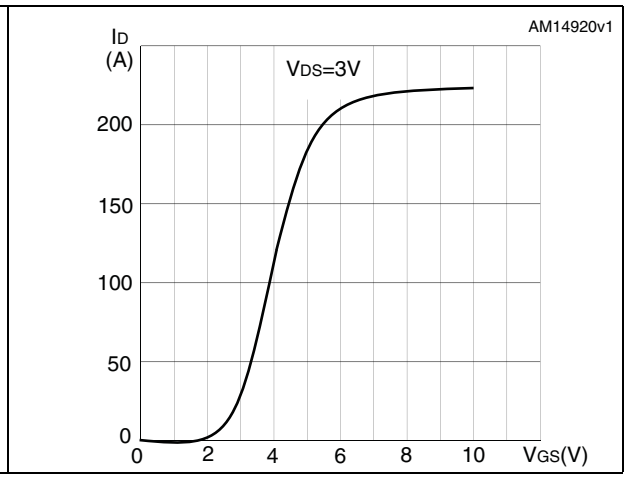


Figure 17. Normalized B_{VDSS} vs temperature

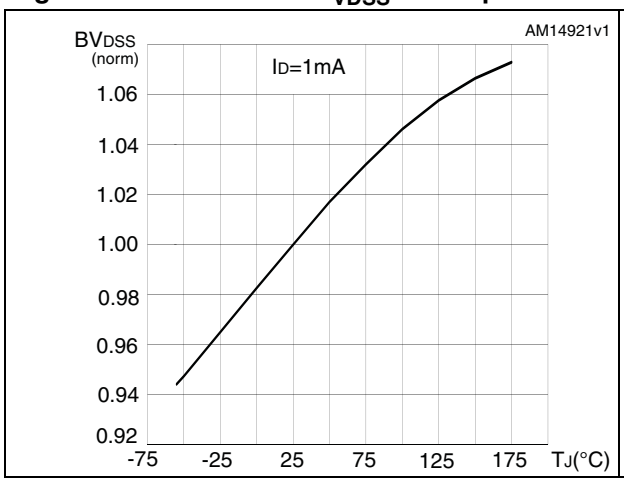


Figure 18. Static drain-source on-resistance

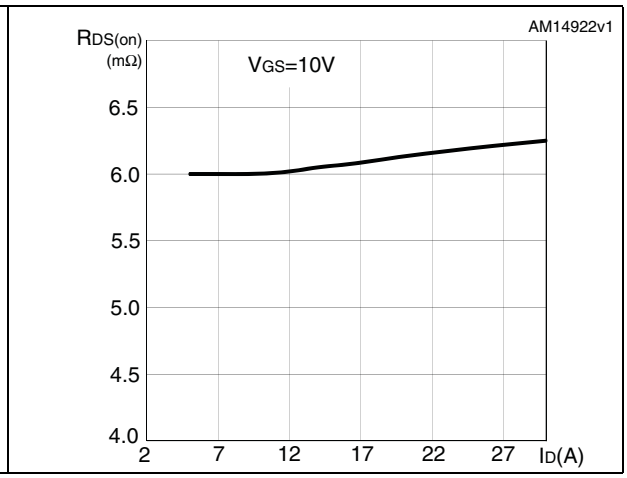


Figure 19. Gate charge vs gate-source voltage

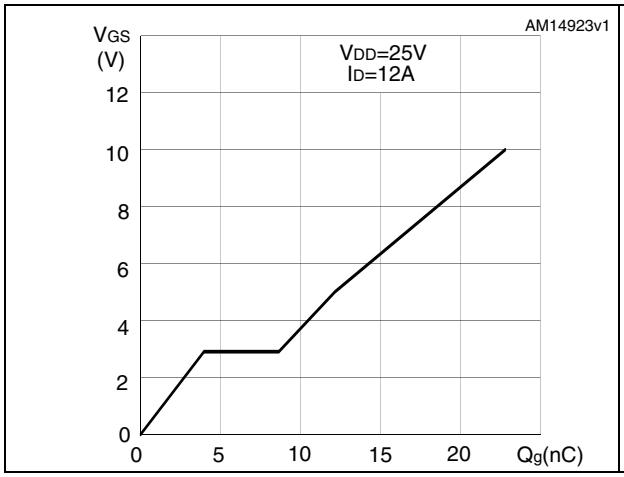


Figure 20. Capacitance variations

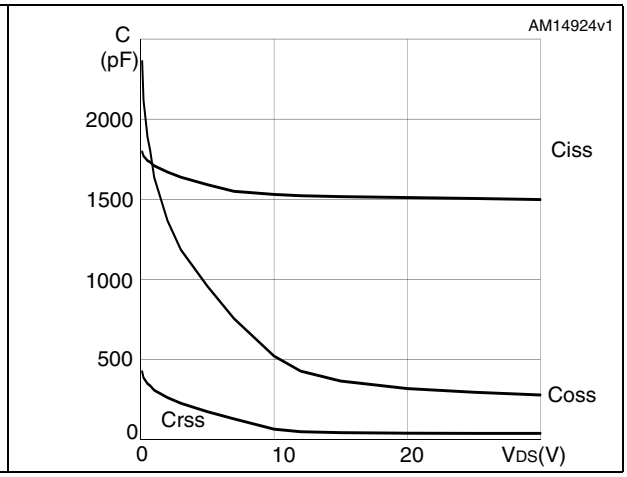


Figure 21. Normalized gate threshold voltage vs temperature

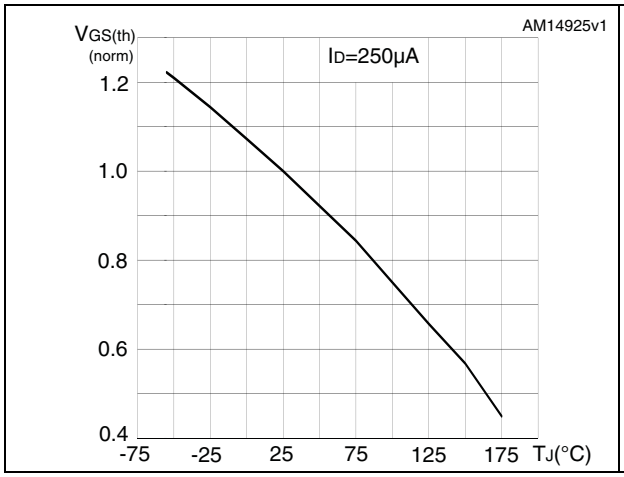


Figure 22. Normalized on-resistance vs temperature

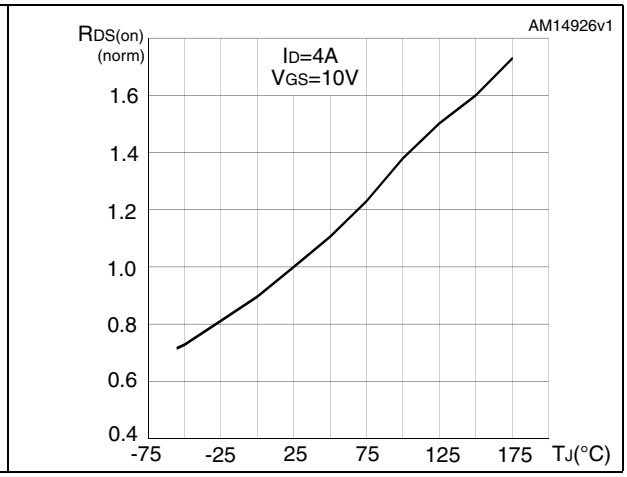
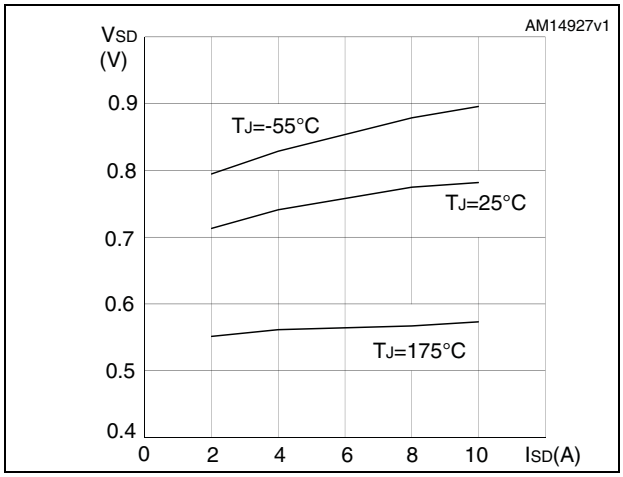


Figure 23. Source-drain diode forward characteristics



3 Test circuits

Figure 24. Switching times test circuit for resistive load

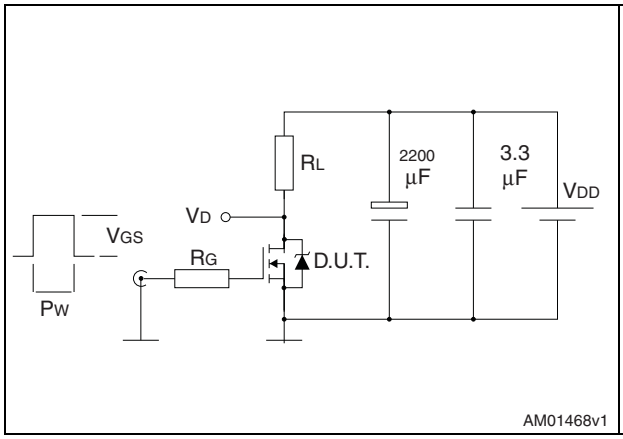


Figure 25. Gate charge test circuit

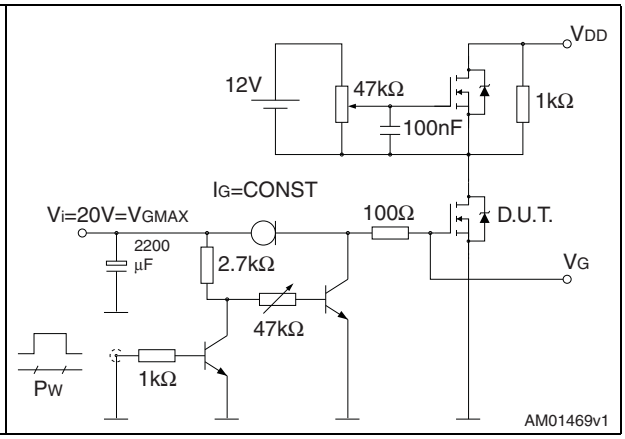


Figure 26. Test circuit for inductive load switching and diode recovery times

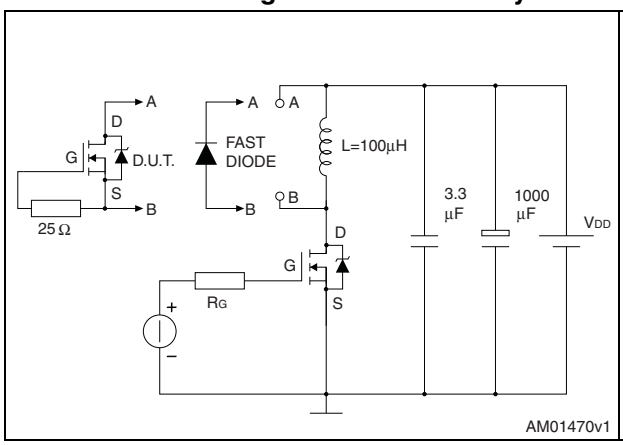


Figure 27. Unclamped inductive load test circuit

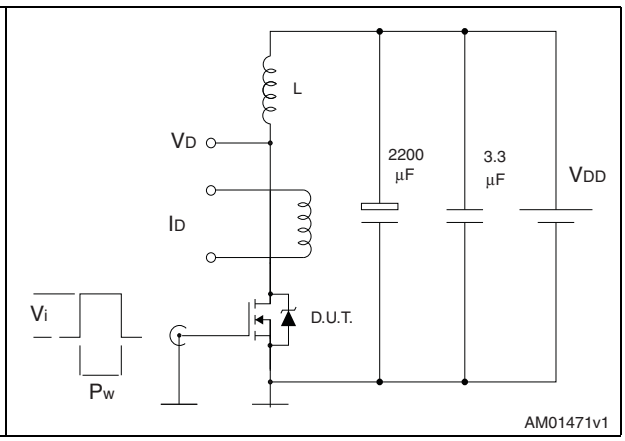


Figure 28. Unclamped inductive waveform

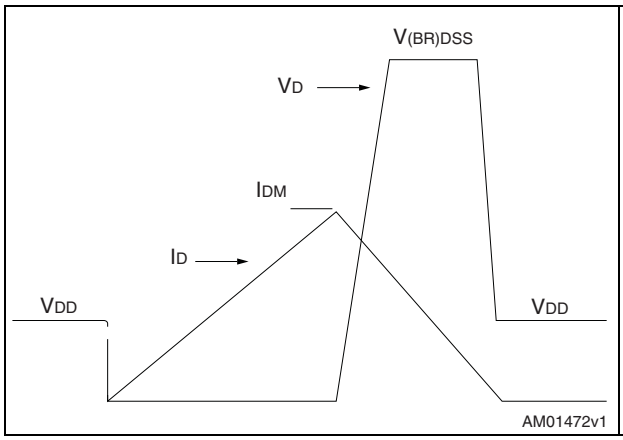
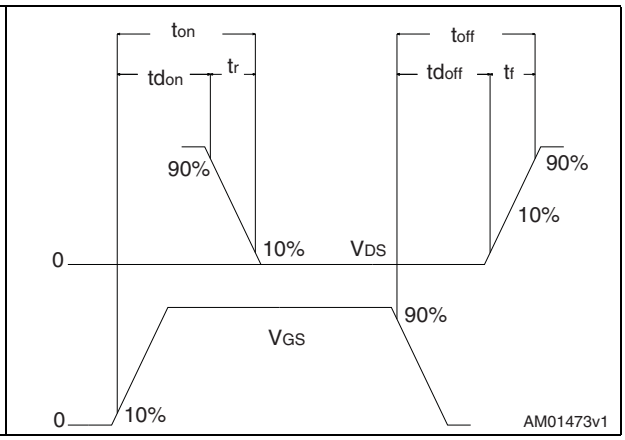


Figure 29. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 asymmetrical double island dimentions

Dim.	mm		
	Min.	Typ.	Max.
A	0.77		0.97
A1			0.03
b	0.42		0.52
D	4.90	5.00‘	5.10
D2	2.40		2.60
E	5.90	6.00	6.10
E2	2.90		3.10
e		1.27	
L	0.40		0.60

Figure 30. Package drawing

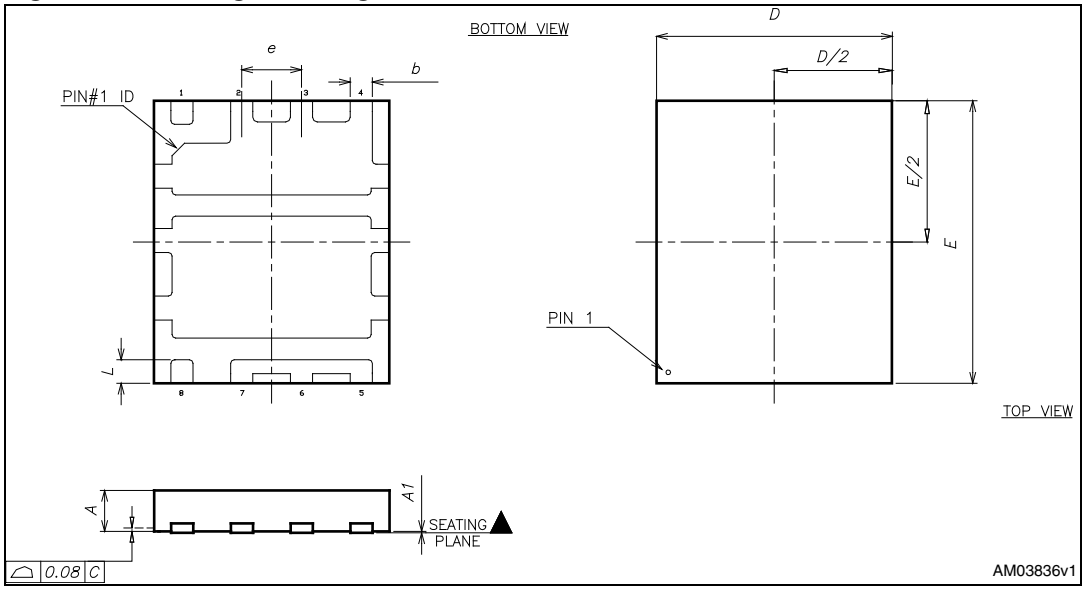
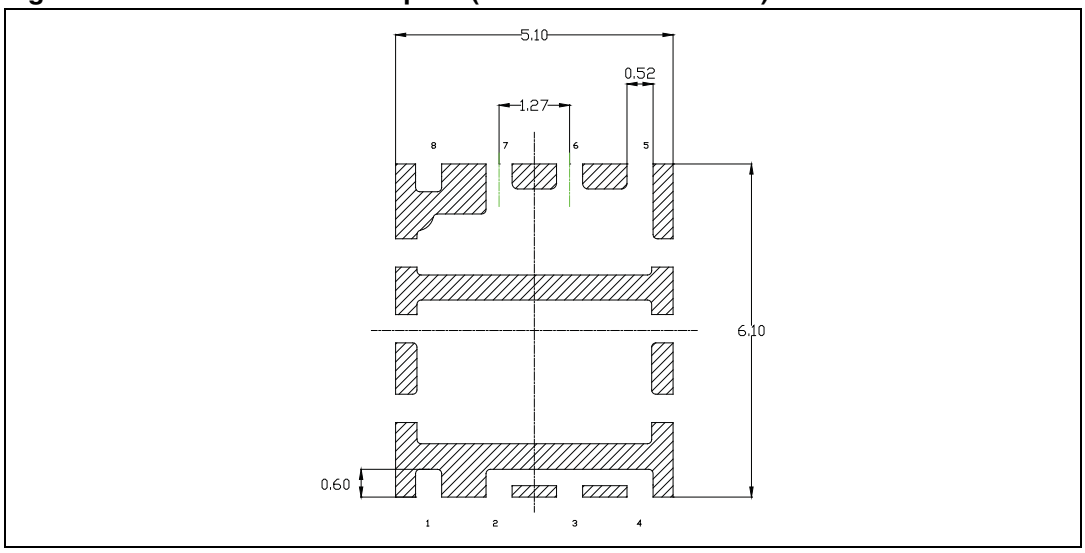


Figure 31. Recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Oct-2012	1	First release.

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