40V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

NEW PRODUCT

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D max T_A = +25°C (Note 7 & 9)
Q1	40V	25mΩ @ V_{GS}= 10V	7.5A
		40mΩ @ V_{GS}= 4.5V	6.2A
Q2	-40V	25mΩ @ V_{GS}= -10V	-7.3A
		45mΩ @ V_{GS}= -4.5V	-5.7A

Features and Benefits

- Reduced Footprint with Two Discrete Devices in Single SO-8
- Low On-Resistance
- Fast Switching Speed
- Low Input/Output Leakage
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **PPAP Available (Note 4)**

Description and Applications

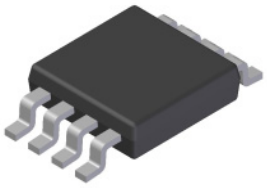
This MOSFET has been designed to ensure that $R_{DS(on)}$ of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSDQ is optimized for use in 3 phases brushless DC motor circuits (BLDC), CCFL backlighting.

- 3 phases BLDC motor
- CCFL backlighting

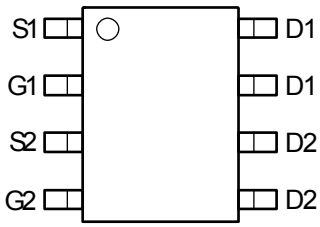
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (approximate)

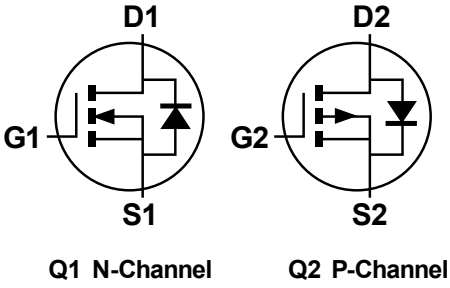
SO-8



Top View



Top View



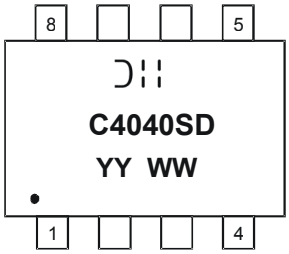
Equivalent Circuit

Ordering Information (Note 4 & 5)

Part Number	Compliance	Case	Packaging
DMC4040SSDQ-13	Automotive	SO-8	2,500/Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Automotive, AEC-Q101 and standard products are electrically and thermally the same, except where specified. For more information, please refer to http://www.diodes.com/quality/product_grade_definitions/.
5. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



= Manufacturer's Marking
C4040SD = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 13 = 2013)
WW = Week (01 - 53)

NEW PRODUCT

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage			V_{GSS}	±20	±20	V
Continuous Drain Current	V_{GS} = 10V	(Notes 7 & 9)	I_D	7.5	-7.5	A
		T_A = +70°C (Notes 7 & 9)		5.8	-5.8	
		(Notes 6 & 9)		5.7	-5.7	
		(Notes 6 & 10)		6.8	-6.8	
Pulsed Drain Current	V_{GS} = 10V	(Notes 8 & 9)	I_{DM}	29.0	-29.0	A
Continuous Source Current (Body diode)		(Notes 7 & 9)	I_S	3.0	-3.0	A
Pulsed Source Current (Body diode)		(Notes 8 & 9)	I_{SM}	29.0	-29.0	A

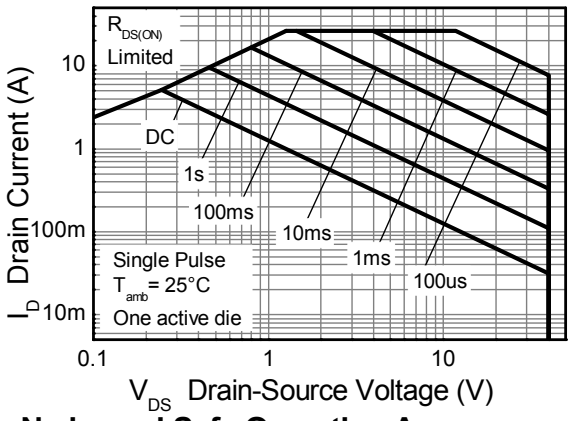
Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	N-Channel - Q1 / P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 6 & 9)	P_D	1.25 10	W mW/°C
	(Notes 6 & 10)		1.8 14.3	
	(Notes 7 & 9)		2.14 17.2	
Thermal Resistance, Junction to Ambient	(Notes 6 & 9)	$R_{\theta JA}$	100	°C/W
	(Notes 6 & 10)		70	
	(Notes 7 & 9)		58	
Thermal Resistance, Junction to Lead	(Notes 9 & 11)	$R_{\theta JL}$	51	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

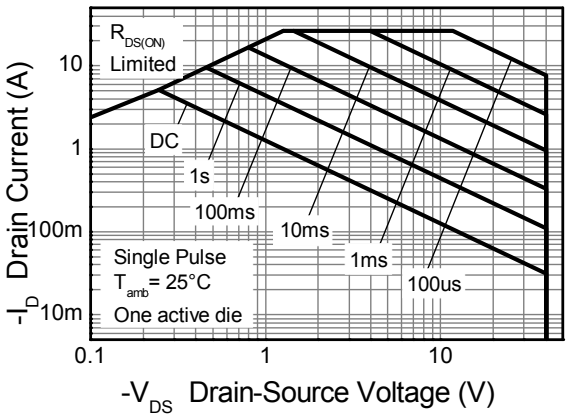
Notes:
6. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
7. Same as note (6), except the device is measured at t ≤ 10 sec.
8. Same as note (6), except the device is pulsed with D= 0.02 and pulse width 300 µs. The pulse current is limited by the maximum junction temperature.
9. For a dual device with one active die.
10. For a device with two active die running at equal power.
11. Thermal resistance from junction to solder-point (at the end of the drain lead).

NEW PRODUCT

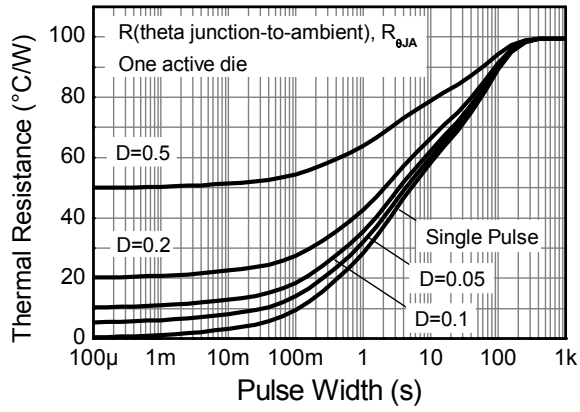
Thermal Characteristics



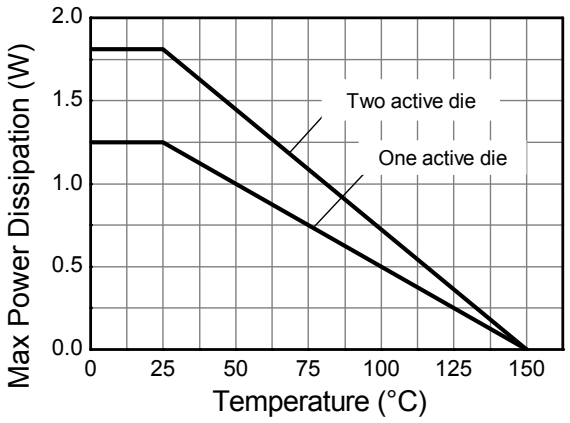
N-channel Safe Operating Area



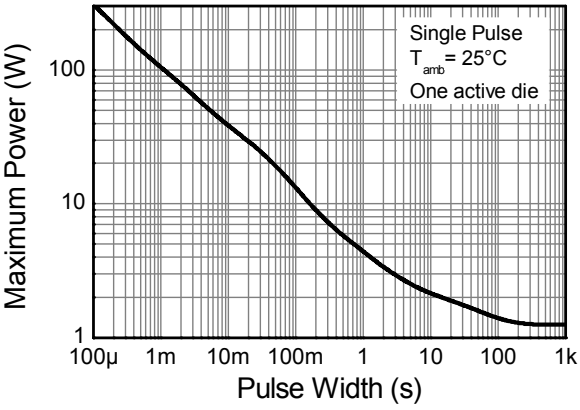
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

NEW PRODUCT

Electrical Characteristics – Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	I_D = 250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	1.3	1.8	V	I_D = 250μA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 12)	$R_{DS\ (ON)}$	—	0.013	0.025	Ω	V_{GS} = 10V, I_D = 3A
			0.028	0.040		V_{GS} = 4.5V, I_D = 3A
Forward Transconductance (Notes 12 & 13)	g_{fs}	—	12.6	—	S	V_{DS} = 5V, I_D = 3A
Diode Forward Voltage (Note 8)	V_{SD}	—	0.7	1.0	V	I_S = 1A, V_{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 13)						
Input Capacitance	C_{iss}	—	1790	—	pF	V_{DS} = 20V, V_{GS} = 0V F = 1MHz
Output Capacitance	C_{oss}	—	160	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	120	—	pF	
Gate Resistance	R_g	—	1.03	—	Ω	V_{DS} = 0V, V_{GS}= 0V, f = 1MHz
Total Gate Charge (Note 14)	Q_g	—	16.0	—	nC	V_{GS} = 4.5V; V_{DS} = 20V, I_D = 3A
Total Gate Charge (Note 14)	Q_g	—	37.6	—	nC	V_{GS} = 10V; V_{DS} = 20V, I_D = 3A
Gate-Source Charge (Note 14)	Q_{gs}	—	7.8	—	nC	V_{GS} = 10V; V_{DS} = 20V, I_D = 3A
Gate-Drain Charge (Note 14)	Q_{gd}	—	6.6	—	nC	V_{GS} = 10V; V_{DS} = 20V, I_D = 3A
Turn-On Delay Time (Note 14)	$t_{D(on)}$	—	8.1	—	ns	V_{DD} = 20V, V_{GS} = 10V I_D = 3A
Turn-On Rise Time (Note 14)	t_r	—	15.1	—	ns	
Turn-Off Delay Time (Note 14)	$t_{D(off)}$	—	24.3	—	ns	
Turn-Off Fall Time (Note 14)	t_f	—	5.3	—	ns	

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
13. For design aid only, not subject to production testing.
14. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics – Q1 N-Channel

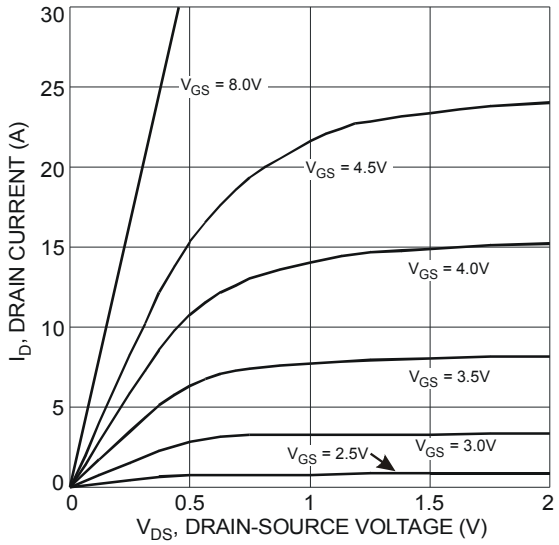


Fig. 1 Typical Output Characteristic

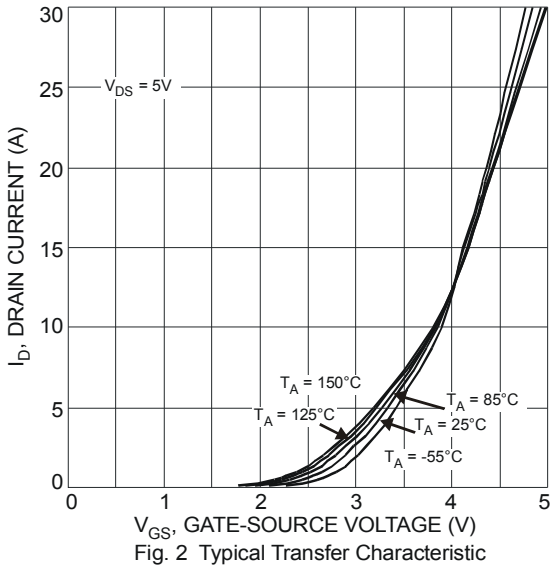


Fig. 2 Typical Transfer Characteristic

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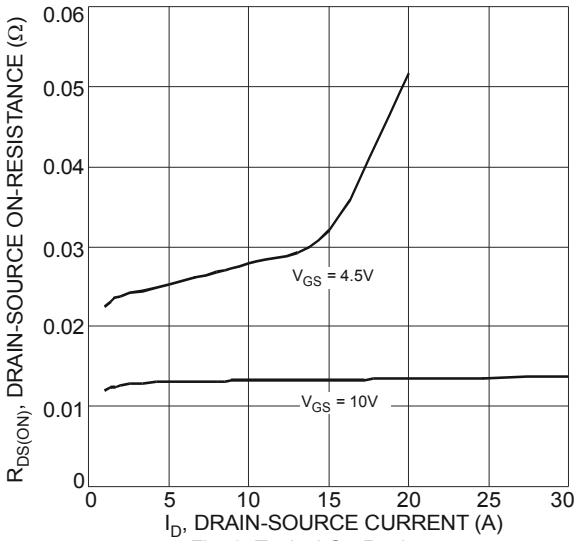

Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

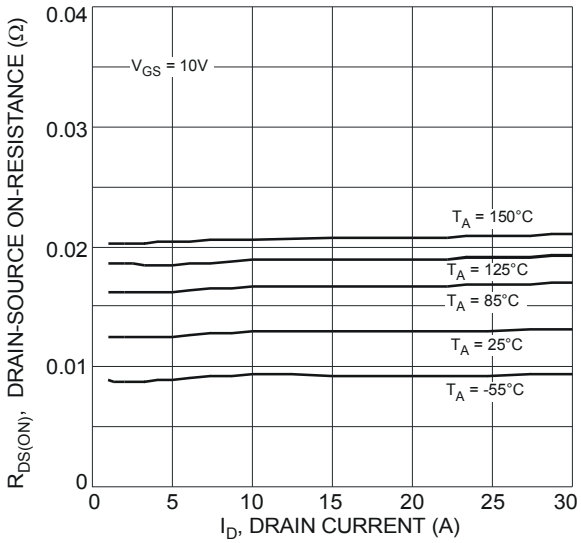

Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

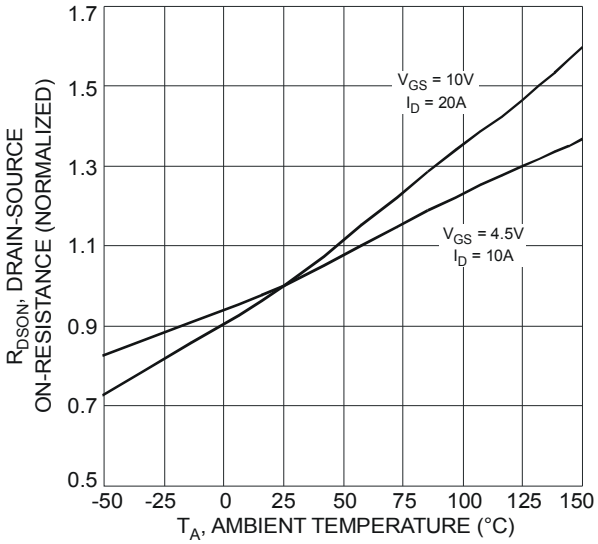

Fig. 5 On-Resistance Variation with Temperature

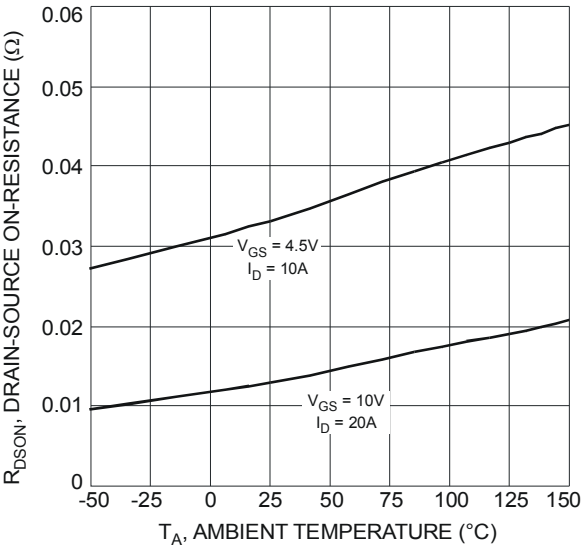

Fig. 6 On-Resistance Variation with Temperature

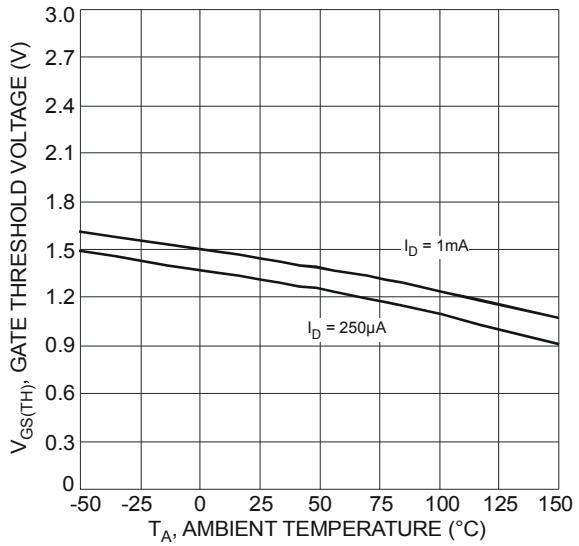

Fig. 7 Gate Threshold Variation vs. Ambient Temperature

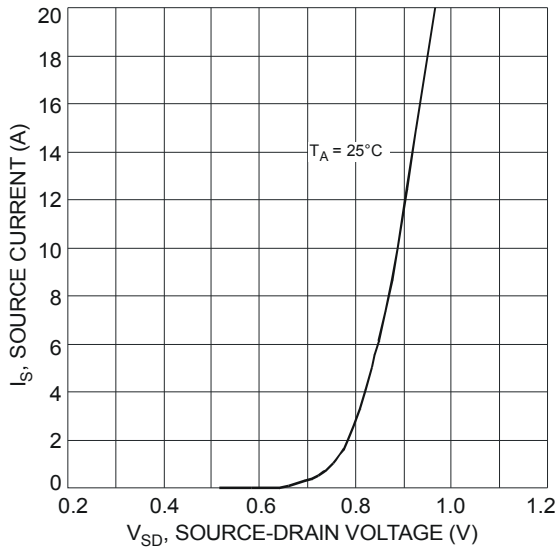

Fig. 8 Diode Forward Voltage vs. Current

NEW PRODUCT

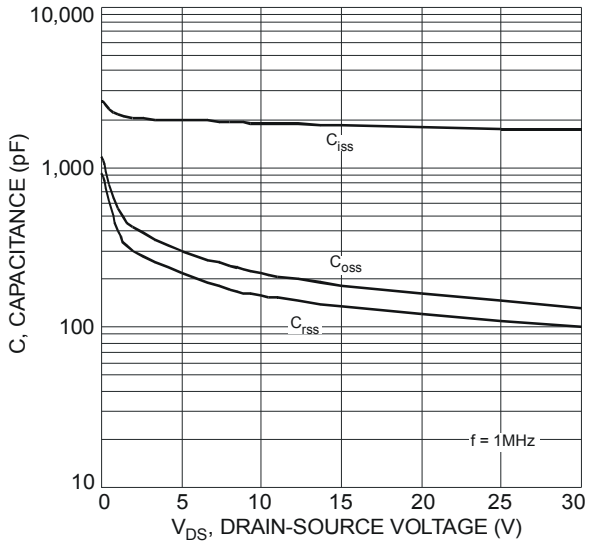

Fig. 9 Typical Total Capacitance

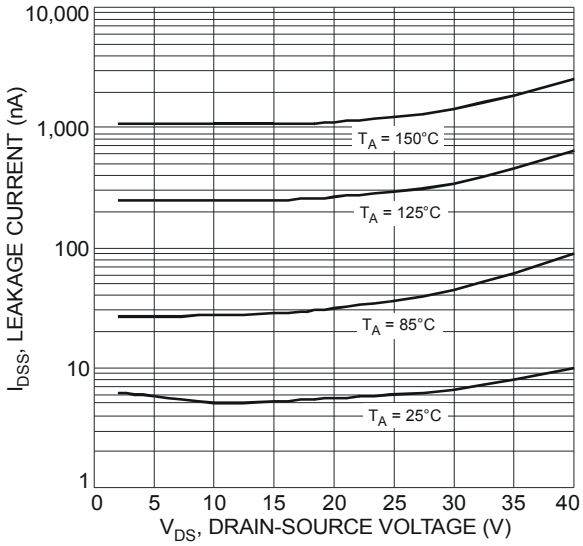

Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

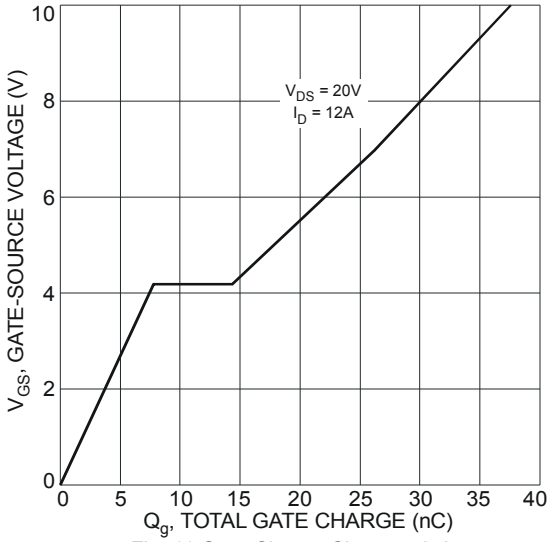

Fig. 11 Gate-Charge Characteristics

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Electrical Characteristics – Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	I_D = -250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	μA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	-1.3	-1.8	V	I_D = -250μA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 15)	$R_{DS\ (ON)}$	—	0.018	0.025	Ω	V_{GS} = -10V, I_D = -3A
			0.030	0.045		V_{GS} = -4.5V, I_D = -3A
Forward Transconductance (Notes 15 & 16)	g_{fs}	—	16.6	—	S	V_{DS} = -5V, I_D = -3A
Diode Forward Voltage (Note 15)	V_{SD}	—	-0.7	-1.0	V	I_S = -1A, V_{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 16)						
Input Capacitance	C_{iss}	—	1643	—	pF	V_{DS} = -20V, V_{GS} = 0V F = 1MHz
Output Capacitance	C_{oss}	—	179	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	128	—	pF	
Gate Resistance	R_g	—	6.43	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (Note 17)	Q_g	—	14.0	—	nC	V_{GS} = -4.5V
Total Gate Charge (Note 17)	Q_g	—	33.7	—	nC	V_{GS} = -10V V_{DS} = -20V I_D = -3A
Gate-Source Charge (Note 17)	Q_{gs}	—	5.5	—	nC	
Gate-Drain Charge (Note 17)	Q_{gd}	—	7.3	—	nC	
Turn-On Delay Time (Note 17)	$t_{D(on)}$	—	6.9	—	ns	V_{DD} = -20V, V_{GS} = -10V I_D = -3A
Turn-On Rise Time (Note 17)	t_r	—	14.7	—	ns	
Turn-Off Delay Time (Note 17)	$t_{D(off)}$	—	53.7	—	ns	
Turn-Off Fall Time (Note 17)	t_f	—	30.9	—	ns	

Notes: 15. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
16. For design aid only, not subject to production testing.
17. Switching characteristics are independent of operating junction temperatures

Typical Characteristics – Q2 P-Channel

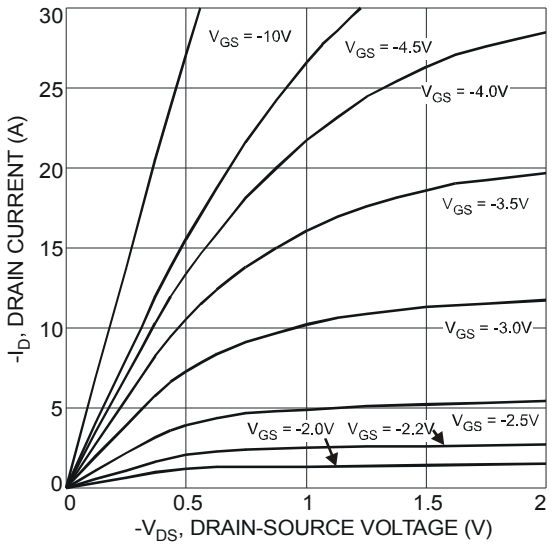

Fig. 13 Typical Output Characteristic

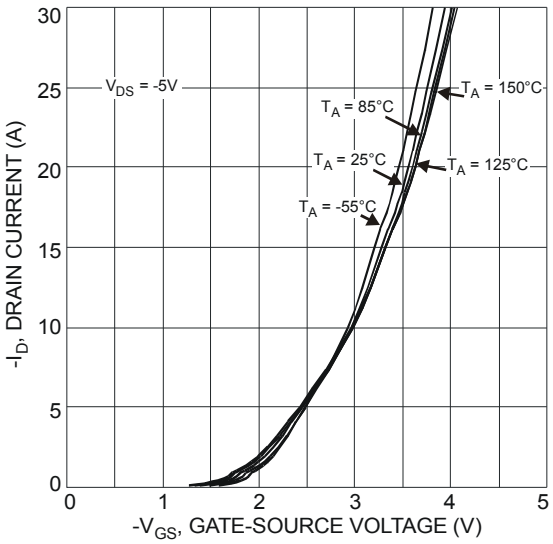

Fig. 14 Typical Transfer Characteristic

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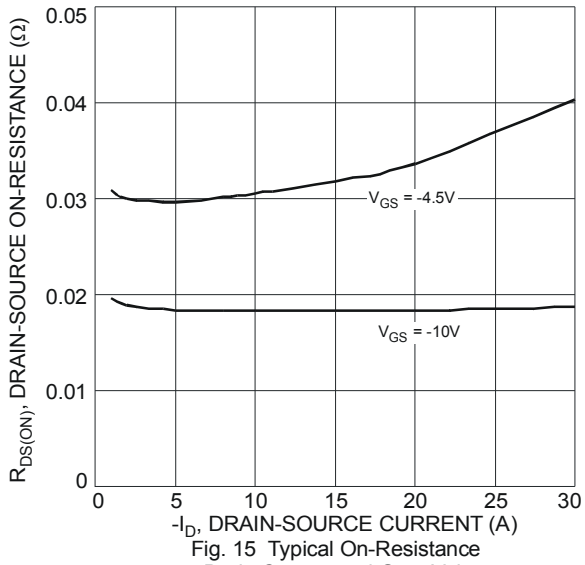


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

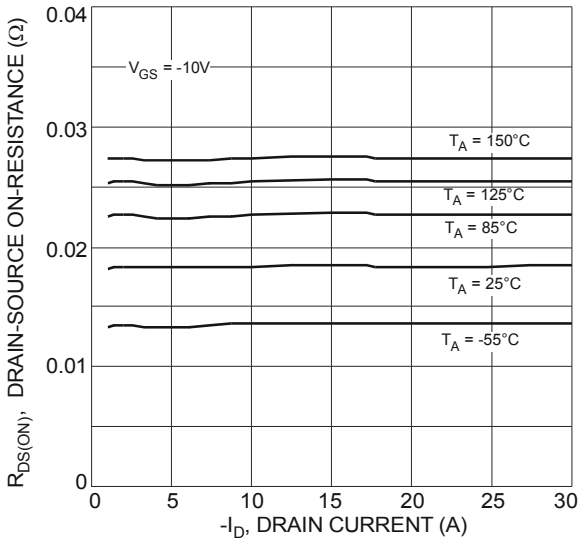


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

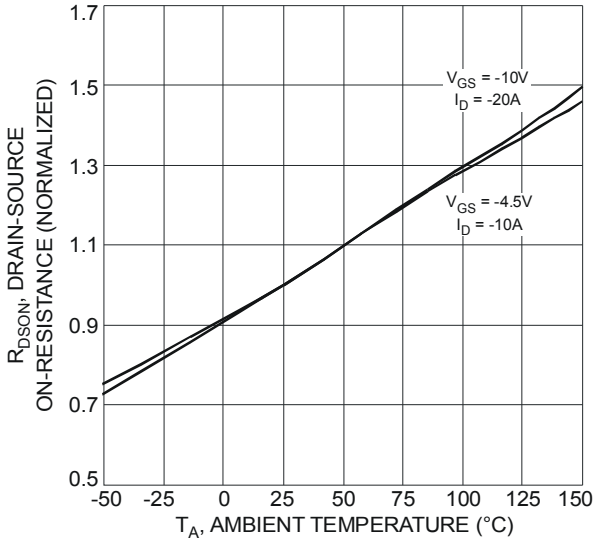


Fig. 17 On-Resistance Variation with Temperature

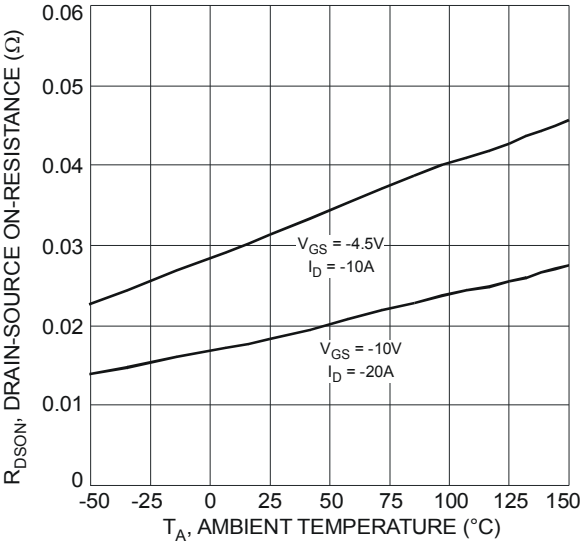


Fig. 18 On-Resistance Variation with Temperature

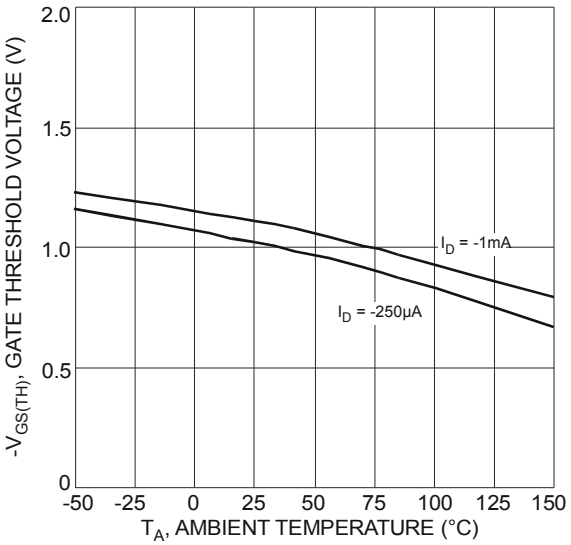


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

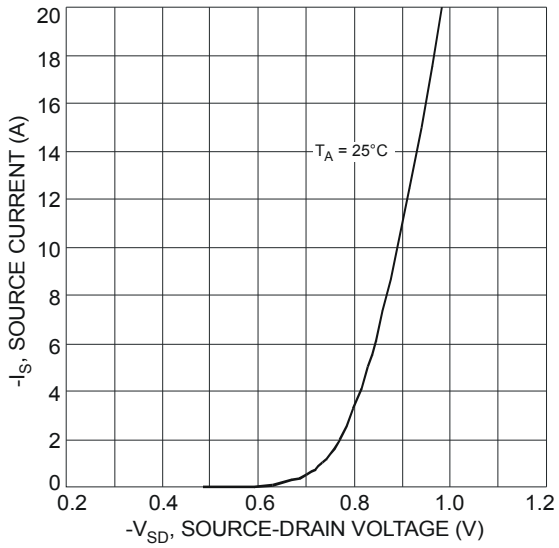


Fig. 20 Diode Forward Voltage vs. Current

NEW PRODUCT

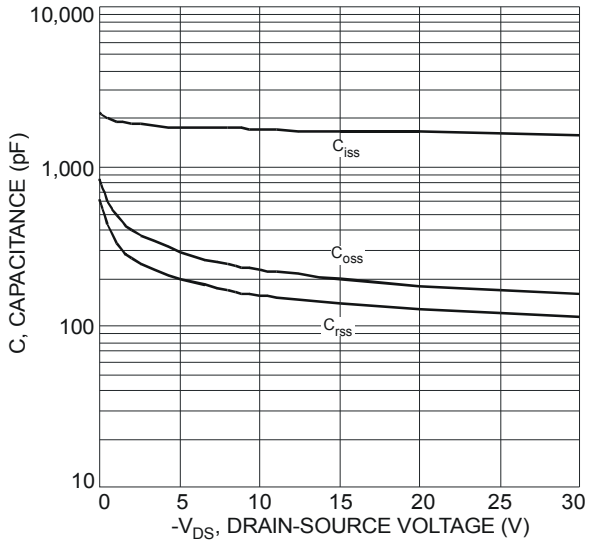


Fig. 21 Typical Total Capacitance

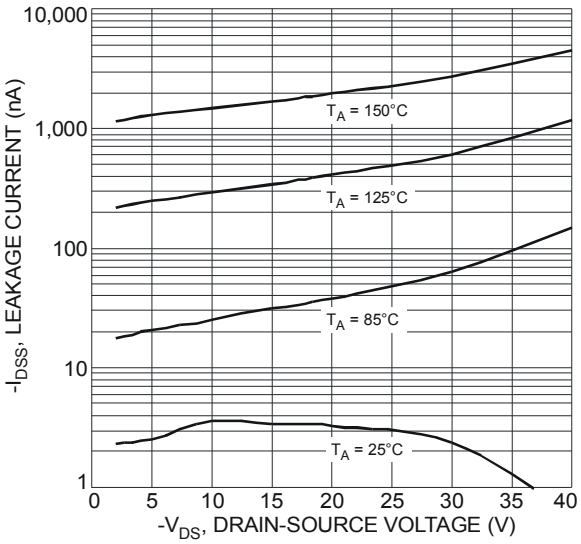


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

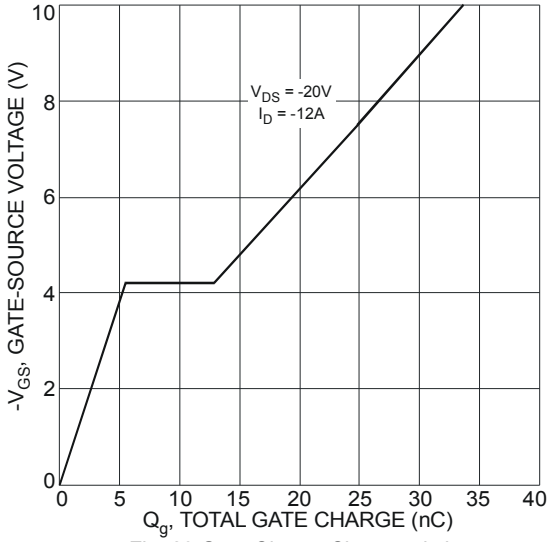
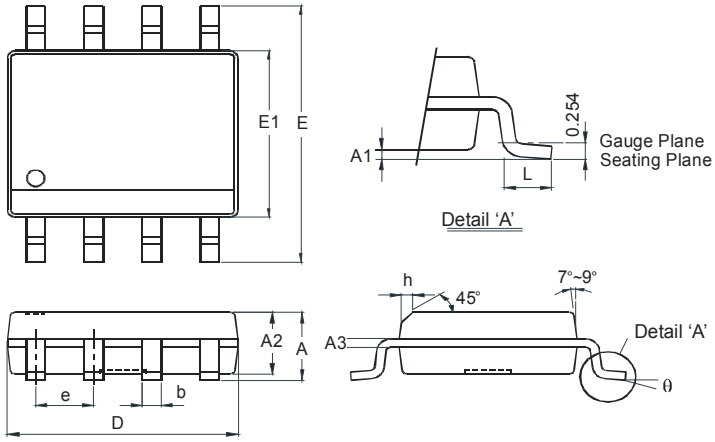


Fig. 23 Gate-Charge Characteristics

NEW PRODUCT

Package Outline Dimensions

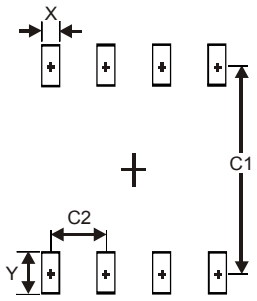
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

NEW PRODUCT

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