BLM7G22S-60PB; BLM7G22S-60PBG

LDMOS 2-stage power MMIC

Rev. 1 — 11 December 2012 Product data sheet

1. Product profile

1.1 General description

The BLM7G22S-60PB(G) is a dual path, 2-stage power MMIC using NXP's state of the art GEN7 LDMOS technology. This device is perfectly suited as general purpose driver in the frequency range from 2100 MHz to 2200 MHz. Available in gull wing or flat lead outline.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq1} = 75 mA; I_{Dq2} = 233 mA.
Test signal: 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; per section unless otherwise specified in a class-AB production circuit.

Test signal	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	2140	28	1.6	31.5	11.3	–43

1.2 Features and benefits

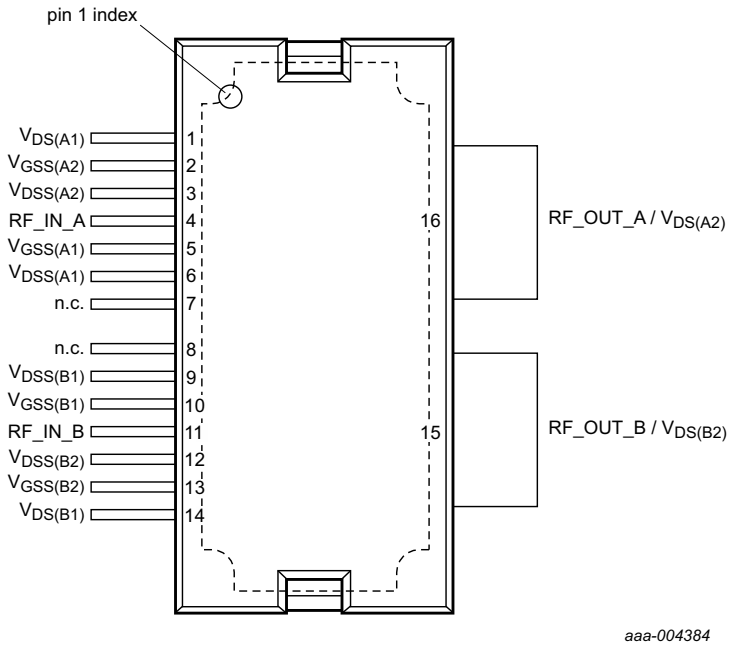
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated current sense
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use (input matched to 50 Ω; output partially matched)
- Designed for broadband operation (frequency 2100 MHz to 2200 MHz)
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

RF power MMIC for W-CDMA base stations in the 2100 MHz to 2200 MHz frequency range.

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of stage A1
$V_{GSS(A2)}$	2	gate sense FET and gate source voltage of stage A2
$V_{DSS(A2)}$	3	drain sense FET source voltage of stage A2
RF_IN_A	4	RF input path A
$V_{GSS(A1)}$	5	gate sense FET and gate source voltage of stage A1
$V_{DSS(A1)}$	6	drain sense FET source voltage of stage A1
n.c.	7	not connected
n.c.	8	not connected
$V_{DSS(B1)}$	9	drain sense FET source voltage of stage B1
$V_{GSS(B1)}$	10	gate sense FET and gate source voltage of stage B1
RF_IN_B	11	RF input path of B
$V_{DSS(B2)}$	12	drain sense FET source voltage of stage B2
$V_{GSS(B2)}$	13	gate sense FET and gate source voltage of stage B2
$V_{DS(B1)}$	14	drain-source voltage of stage B1

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT_A/$V_{DS(A2)}$	15	RF output path A / drain source voltage of stage A2
RF_OUT_B/$V_{DS(B2)}$	16	RF output path B / drain source voltage of stage B2
GND [1]	flange	RF ground

[1] Flange = RF_GROUND.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM7G22S-60PB	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-1
BLM7G22S-60PBG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-1

4. Block diagram

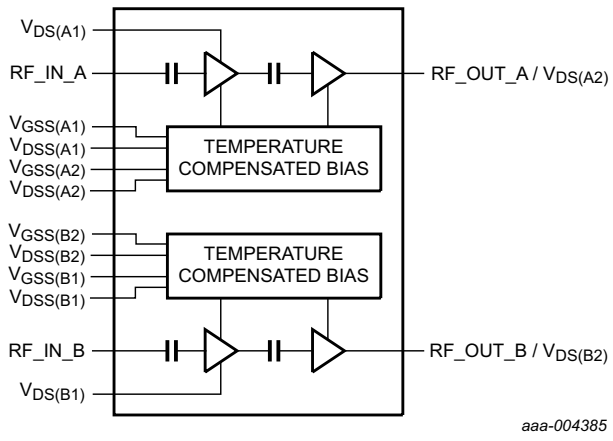


Fig 2. Block diagram of BLM7G22-60PBG

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
$V_{GS(sense)}$	sense gate-source voltage		–0.5	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions		Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; T_{case} = 90 °C; P_L = 3.2 W	[1]	1.1	K/W
		driver stage; T_{case} = 90 °C; P_L = 3.2 W	[1]	3.2	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Final stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.422 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 42 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 253 mA	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	7.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1478 mA	-	2.85	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.48 A	-	350	-	mΩ
I_{Dq}	quiescent drain current	main transistor: V_{DS} = 28 V sense transistor: I_D = 7 mA; V_{DS} = 28 V	208	233	257	mA
Driver stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.116 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 11.6 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 69.6 mA	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	2.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 406 mA	-	0.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 0.4 A	-	2350	-	mΩ
I_{Dq}	quiescent drain current	main transistor: V_{DS} = 28 V sense transistor: I_D = 7 mA; V_{DS} = 28 V	67	75	83	mA

Table 7. RF Characteristics

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 75 mA; I_{Dq2} = 233 mA. Test signal: 2-carrier W-CDMA; 3GPP test model 1; 64 DPCH; clipping at 46 %; PAR = 8.4 dB at 0.01% probability on CCDF per carrier; carrier spacing = 5 MHz; f = 2140 MHz; per section unless otherwise specified, measured in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 1.6 W	29.5	31.5	33.5	dB
η_D	drain efficiency	$P_{L(AV)}$ = 1.6 W	10	11.3	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 1.6 W	-	−17	−10	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 1.6 W	-	−43	−40	dBc

8. Application information

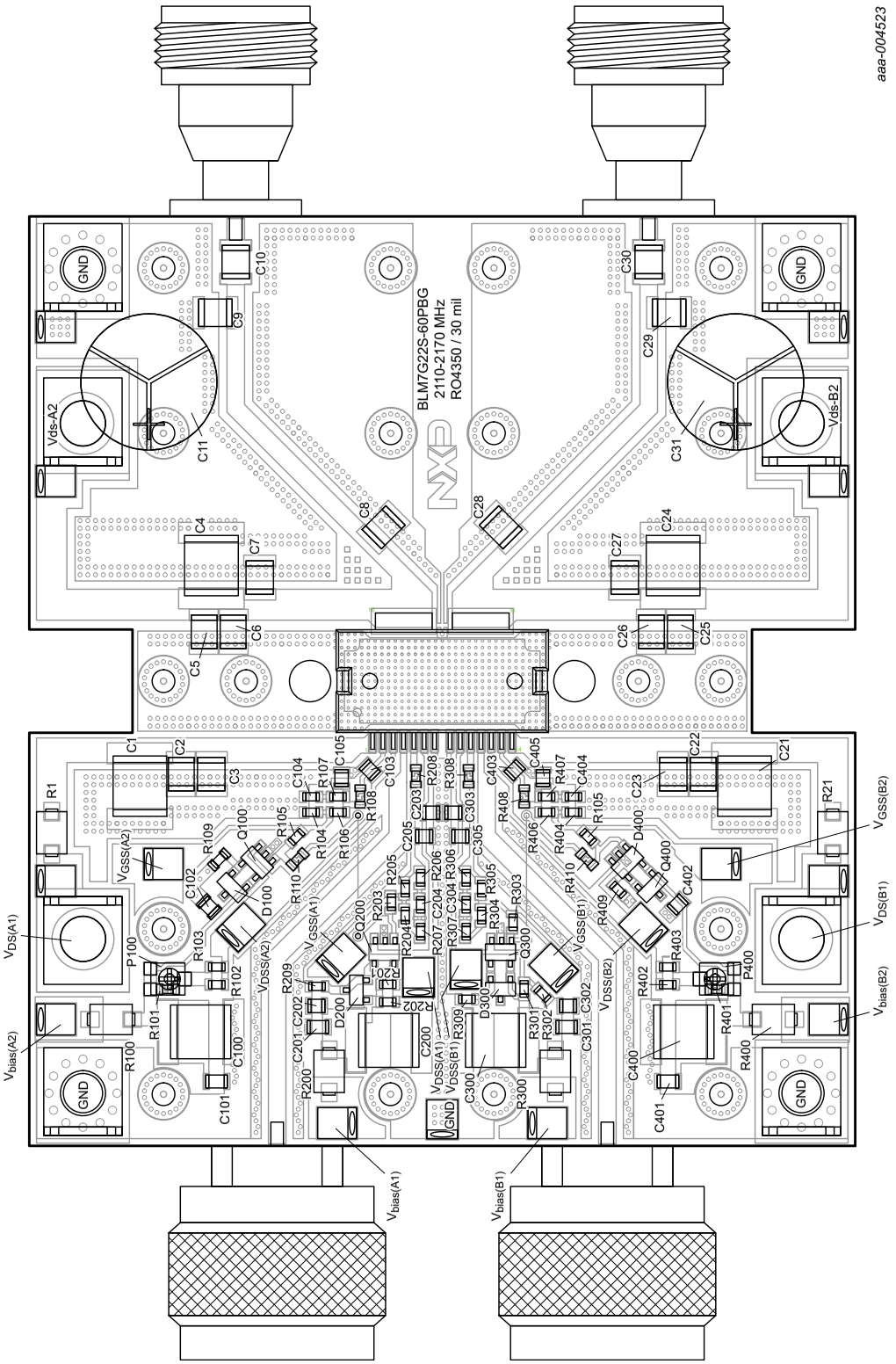
Table 8. List of components

For test circuit see Figure 3.

Component	Description	Value	Remarks
C1, C4, C21, C24, C100, C200, C300, C400	capacitor	10 μF	
C2, C5, C6, C22, C25, C26	capacitor	1 μF	
C3, C7, C10, C23, C27, C30	capacitor	8.2 pF [1]	
C8, C28	capacitor	1.6 pF [1]	
C9, C29	capacitor	0.4 pF [1]	
C11, C31	electrolytic capacitor	470 μF	
C101, C201, C301, C401	capacitor	100 nF	
C102, C103, C105, C202, C203, C205, C302, C303, C305, C402, C403, C405	capacitor	12 pF [2]	
C104, C204, C304, C404	capacitor	4.7 μF	
D100, D200, D300, D400	IC: LM4051	-	
P100, P400	potentiometer	-	do not populate
Q100, Q200, Q300, Q400	IC	-	LM7341
R1, R21	ferrite bead	-	
R100, R200, R300, R400	resistor	4.7 Ω	
R101, R108, R208, R308, R401, R408	resistor	0 Ω	
R102, R402	resistor	360 Ω	1% tolerance
R103, R403	resistor	330 Ω	1% tolerance
R104, R203, R303, R404	resistor	68 kΩ	
R105, R405	resistor	10 kΩ	
R106, R205, R305, R406	resistor	820 Ω	
R107, R206, R306, R407	resistor	47 Ω	
R109, R209, R309, R409	resistor	300 kΩ	
R201, R301	resistor	180 Ω	1% tolerance
R202, R302	resistor	3.6 kΩ	1% tolerance
R204, R304	resistor	9.1 kΩ	
R207, R307	resistor	1 kΩ	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.762 mm.

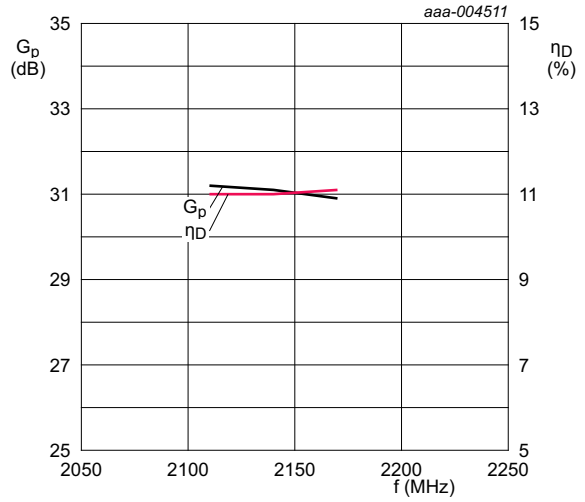
See Table 8 for a list of components.

Fig 3. Component layout for class-AB application circuit with auto-bias

8.1 Performance curves

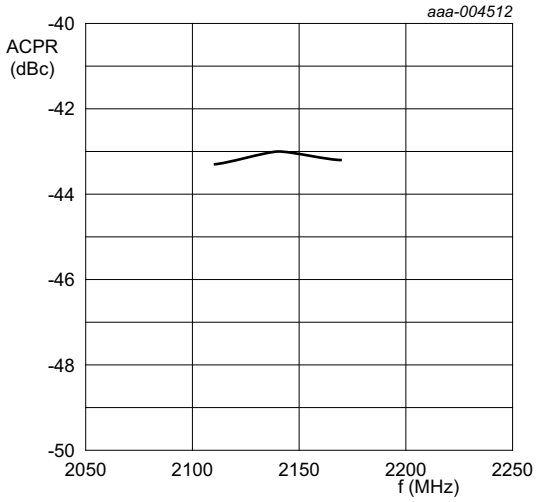
Performance curves are measured per section in a class-AB BLM7G22S-60PBG application circuit with auto-bias.

8.1.1 W-CDMA



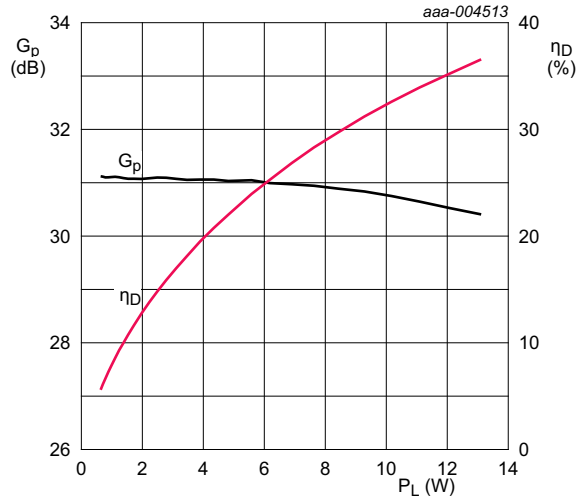
T_{case} = 25 °C; V_{DS} = 28 V; $P_{L(AV)}$ = 1.6 W; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; carrier spacing = 5 MHz.

Fig 4. Power gain and drain efficiency as function of frequency; typical values



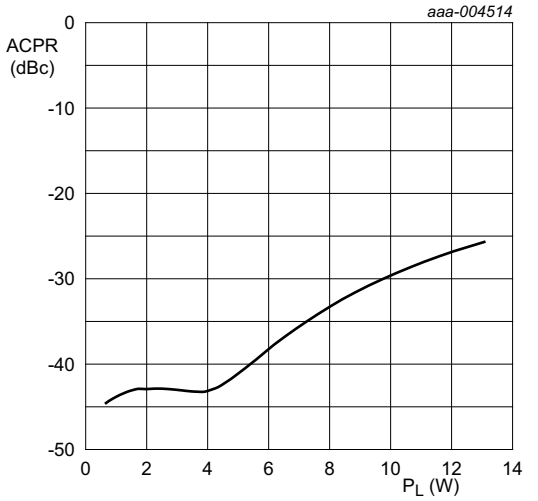
T_{case} = 25 °C; V_{DS} = 28 V; $P_{L(AV)}$ = 1.6 W; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; carrier spacing = 5 MHz.

Fig 5. Adjacent channel power ratio as a function of frequency; typical values



T_{case} = 25 °C; V_{DS} = 28 V; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; carrier spacing = 5 MHz.

Fig 6. Power gain as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; carrier spacing = 5 MHz.

Fig 7. Adjacent channel power ratio as a function of output power; typical values

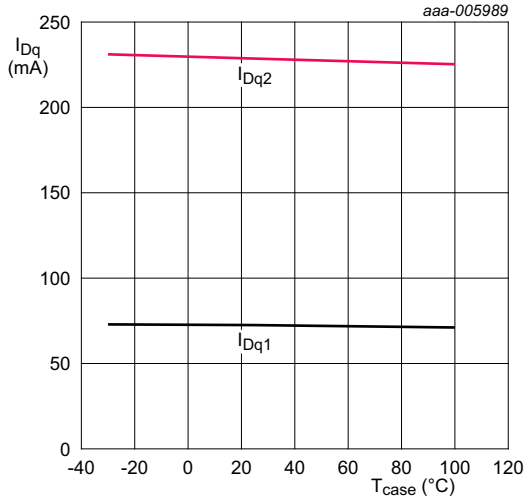
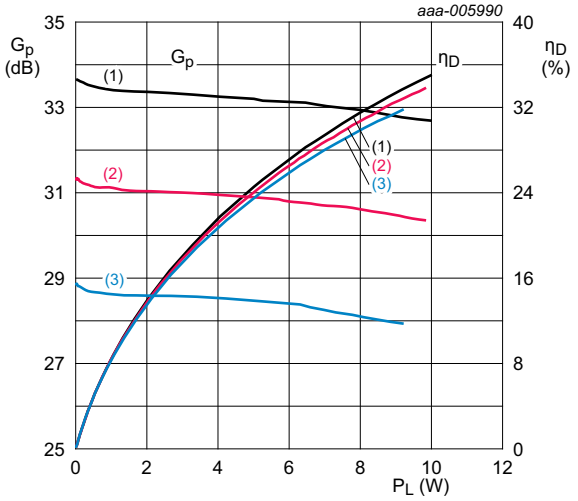


Fig 8. Quiescent drain current as a function of case temperature; typical values



V_{DS} = 28 V; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; carrier spacing = 5 MHz.

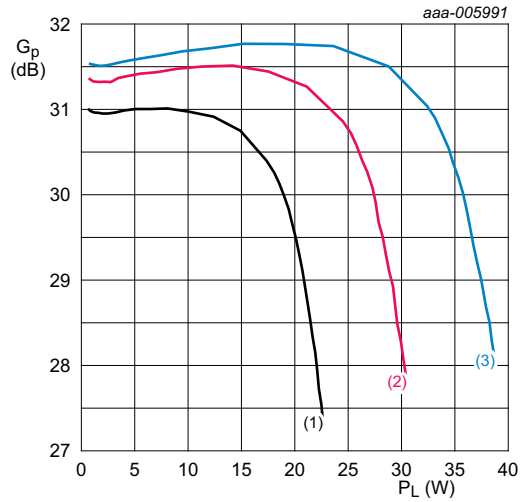
(1) T_{case} = −30 °C

(2) T_{case} = +25 °C

(3) T_{case} = +100 °C

Fig 9. Power gain and drain efficiency as function of output power; typical values

8.1.2 1-Tone pulsed CW



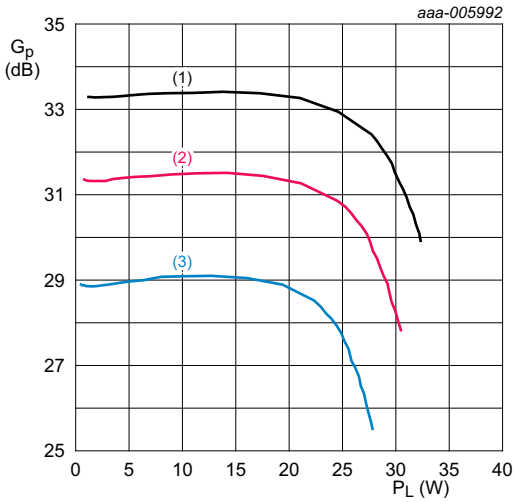
T_{case} = 25 °C; V_{DS} = 28 V; $P_{L(AV)}$ = 1.6 W; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; δ = 10 %; t_p = 100 µs.

(1) V_{DD} = 24 V

(2) V_{DD} = 28 V

(3) V_{DD} = 32 V

Fig 10. Power gain as a function of output power; typical values



V_{DS} = 28 V; $P_{L(AV)}$ = 1.6 W; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; δ = 10 %; t_p = 100 µs.

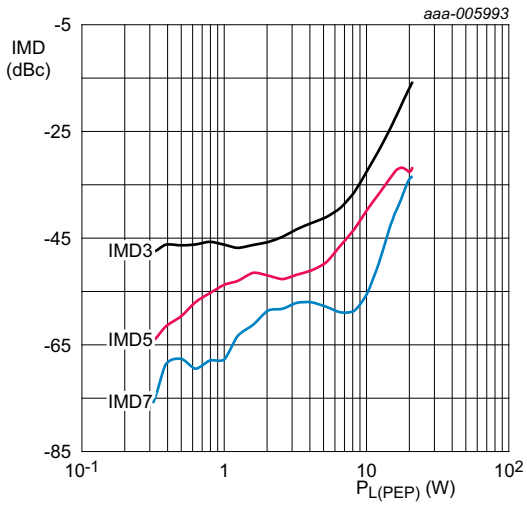
(1) T_{case} = −30 °C

(2) T_{case} = +25 °C

(3) T_{case} = +100 °C

Fig 11. Power gain as a function of output power; typical values

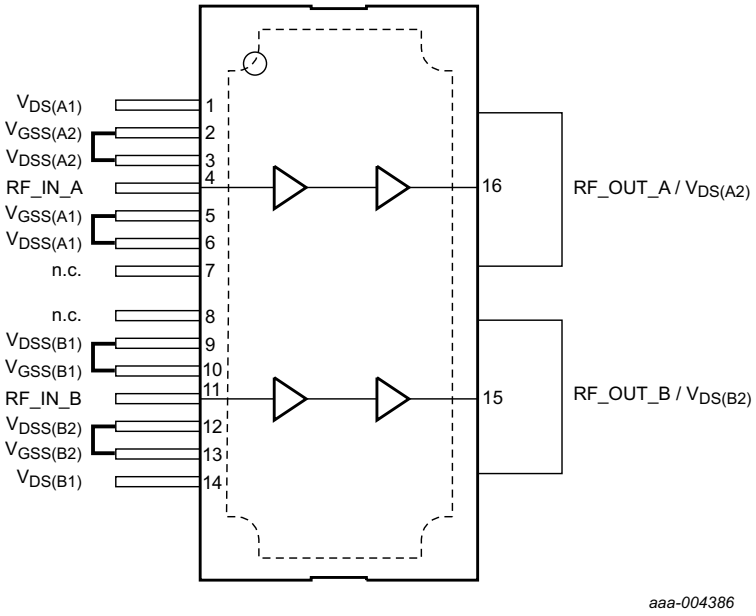
8.1.3 2-Tone CW



T_{case} = 25 °C; V_{DS} = 28 V; f_c = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; tone spacing = 100 kHz.

Fig 12. Intermodulation distortion as a function of peak envelope power load power; typical values

8.2 Application without auto-bias



Connect pins 2 and 3; connect pins 5 and 6; connect pins 9 and 10; connect pins 12 and 13 at board level. The exposed backside of the package is the ground terminal of the device.

Fig 13. Non auto-bias application

9. Test information

9.1 Ruggedness

The BLM7G22S-60PB and BLM7G22S-60PBG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq1} = 75 mA; I_{Dq2} = 233 mA; P_L = 27 W (W-CDMA); f = 2140 MHz.

9.2 Impedance information

Table 9. Typical impedance

Measured load-pull data. Typical values per section unless otherwise specified.

f	Z_S [1]	Z_L [1]
MHz	**Ω**	**Ω**
BLM7G22S-60PB		
2050	58.86 + j21.82	10.54 – j3.20
2110	58.70 + j29.76	10.23 – j2.72
2140	51.80 + j41.56	9.56 – j2.90
2170	47.31 + j44.60	9.10 – j2.80
2230	38.35 + j46.53	8.41 – j2.05
BLM7G22S-60PBG		
2080	55.62 + j18.89	15.89 – j2.28
2110	55.61 + j19.04	14.74 – j2.59
2140	55.60 + j19.12	13.56 – j2.75
2170	55.57 + j19.25	12.38 – j2.75
2200	55.53 + j19.39	11.20 – j2.61
2230	55.48 + j19.55	10.05 – j2.34

[1] Z_S and Z_L defined in Figure 14.

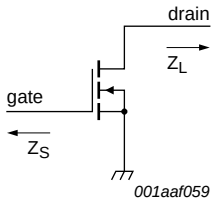
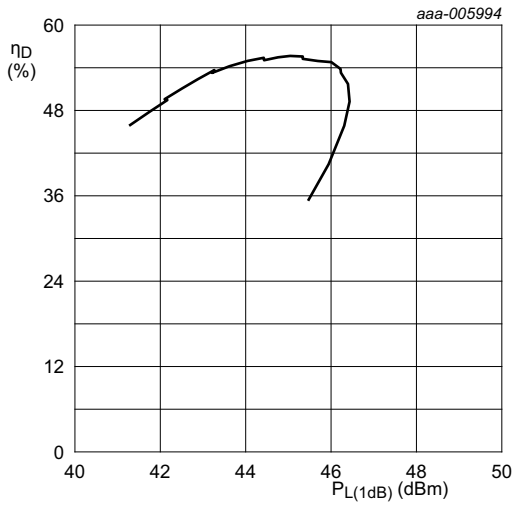


Fig 14. Definition of transistor impedance

9.3 Performance curves

Performance curves are measured per section.

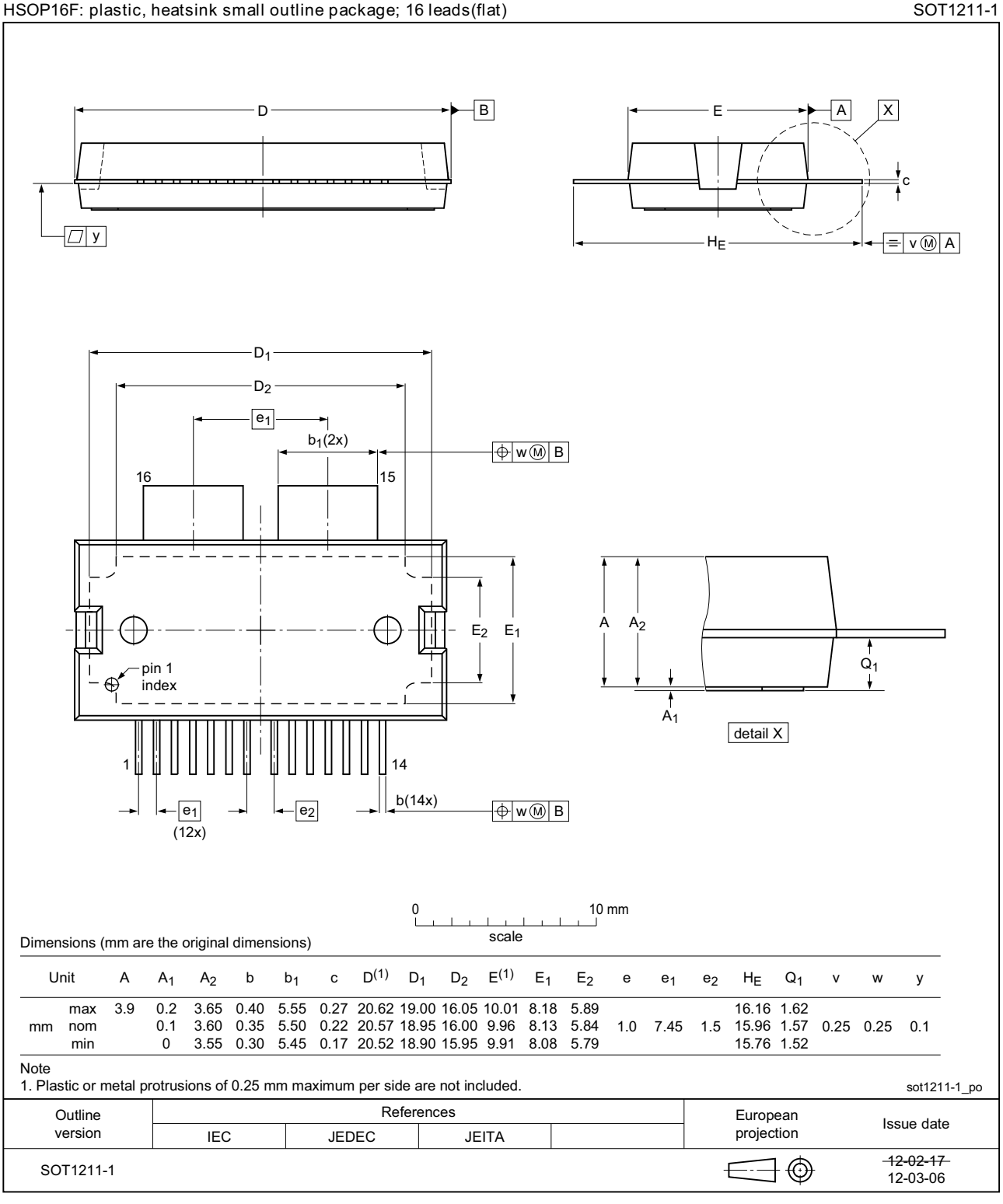


T_{case} = 25 °C; V_{DS} = 28 V; $P_{L(AV)}$ = 1.6 W; f = 2140 MHz; I_{Dq1} = 75 mA; I_{Dq2} = 232 mA; δ = 10 %; t_p = 100 μs.

Fig 15. One-tone pulsed CW drain efficiency at 1 dB gain compression as function of output power at 1 dB gain compression; typical values

10. Package outline

HSOP16F: plastic, heatsink small outline package; 16 leads(flat) SOT1211-1



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	b_1	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	e_1	e_2	H_E	Q_1	v	w	y
mm	max	3.9	0.2	3.65	0.40	5.55	0.27	20.62	19.00	16.05	10.01	8.18	5.89				16.16	1.62			
	nom		0.1	3.60	0.35	5.50	0.22	20.57	18.95	16.00	9.96	8.13	5.84	1.0	7.45	1.5	15.96	1.57	0.25	0.25	0.1
	min		0	3.55	0.30	5.45	0.17	20.52	18.90	15.95	9.91	8.08	5.79				15.76	1.52			

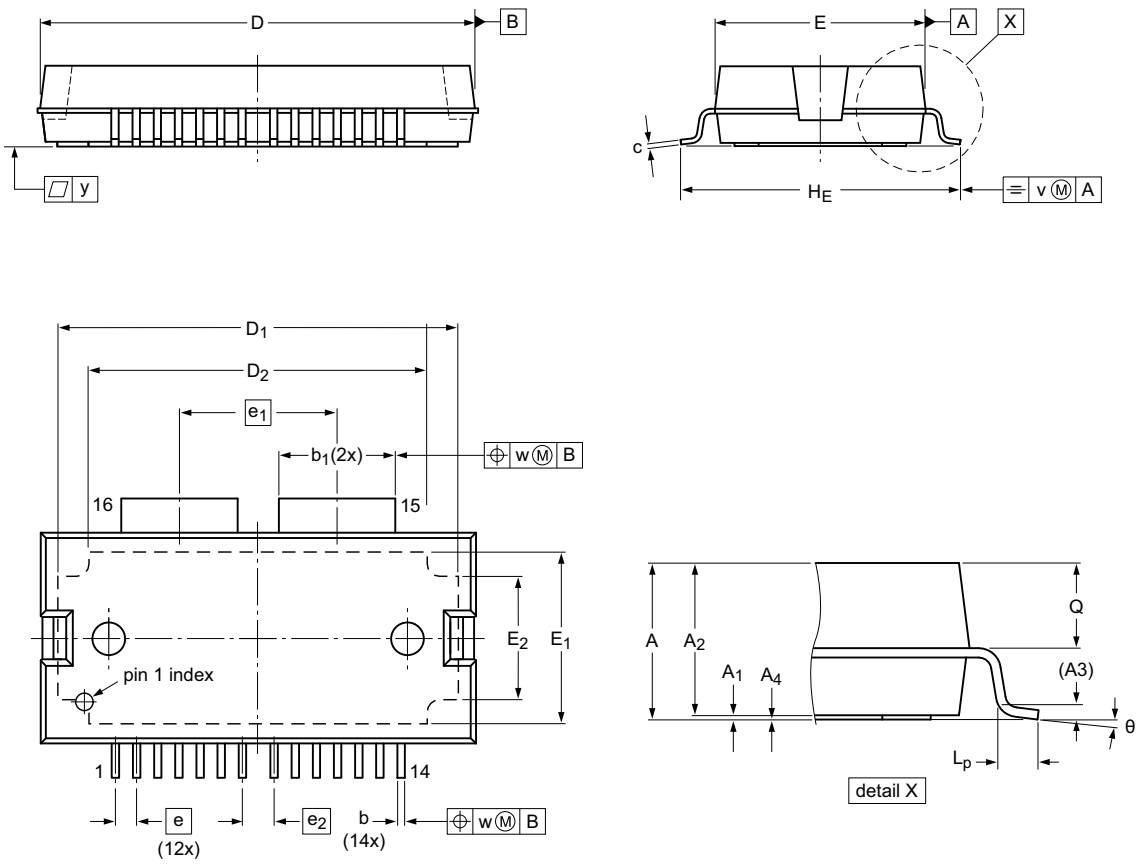
Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1211-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1211-1						~~12-02-17~~ 12-03-06

Fig 16. Package outline SOT1211-1 (HSOP16F)

HSOP16: plastic, heatsink small outline package; 16 leads **SOT1212-1**



w	y	θ
0.25	0.1	7° / 3° / 0°

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	A_4	b	b_1	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	e_1	e_2	H_E	L_p	Q	v
mm	max	3.9	0.2	3.65		0.06	0.40	5.55	0.27	20.62	19.00	16.05	10.01	8.18	5.89				13.5	1.10	2.07	
	nom		0.1	3.60	0.35	0	0.35	5.50	0.22	20.57	18.95	16.00	9.96	8.13	5.84	1.0	7.45	1.5	13.2	0.95	2.02	0.25
	min		0	3.55		-0.02	0.30	5.45	0.17	20.52	18.90	15.95	9.91	8.08	5.79				12.9	0.80	1.97	

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1212-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1212-1						~~12-05-14~~ 12-05-21

Fig 17. Package outline SOT1212-1 (HSOP16)

11. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Waveform
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GEN7	Seventh Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G22S-60PB_7G22S-60PBG v.1	20121211	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

14.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

16. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 December 2012
Document identifier: BLM7G22S-60PB_7G22S-60PBG