AN6295NK

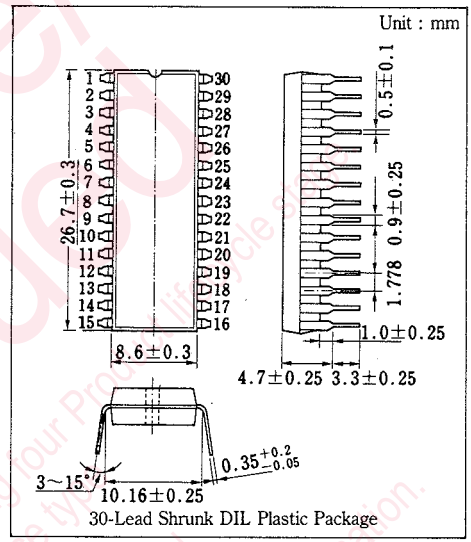
Dual Hi-Fi VTR Peak-Noise-Reduction Circuit

■ Outline

The AN6295NK is an integrated circuit designed for the Hi-Fi VTR noise reduction and responds to the stereo operation with one chip. Its dymanic range is 110dB and its S/N ratio is 80dB or over. It has fewer external parts because it is equipped with a built-in resistance for time constants.

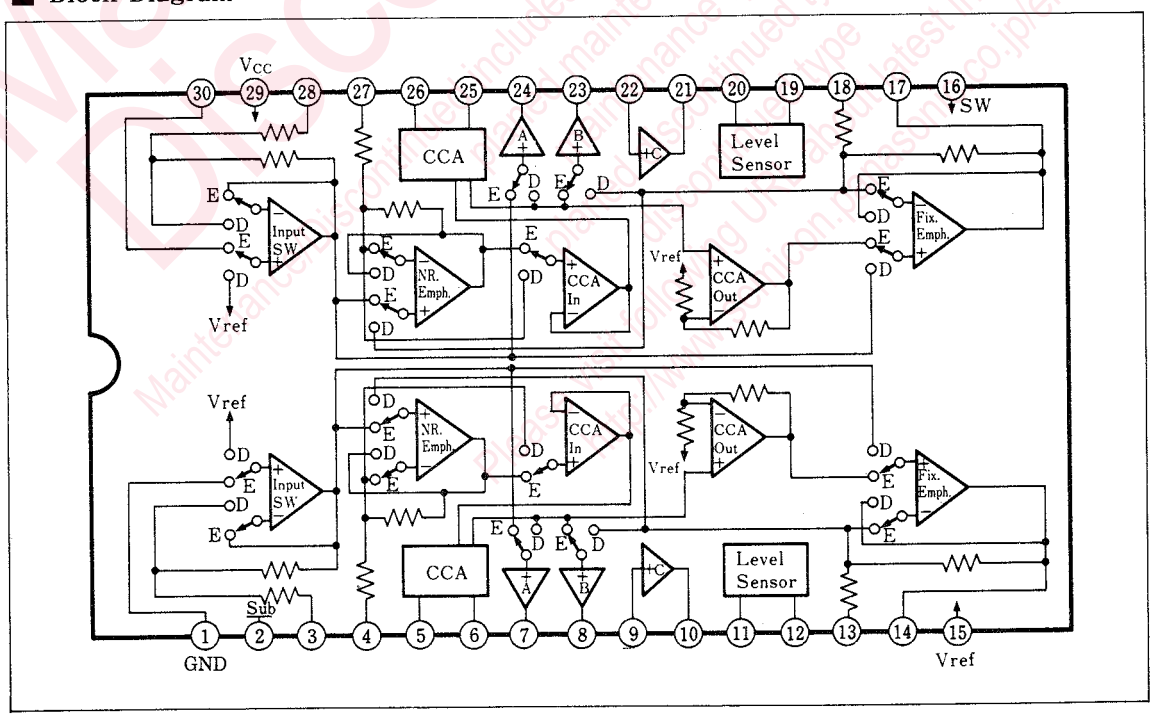
■ Features

- All circuit blocks are included.
- Minimum number of external components
- Wide dynamic range: 110dB



30-Lead Shrunk DIL Plastic Package

■ Block Diagram



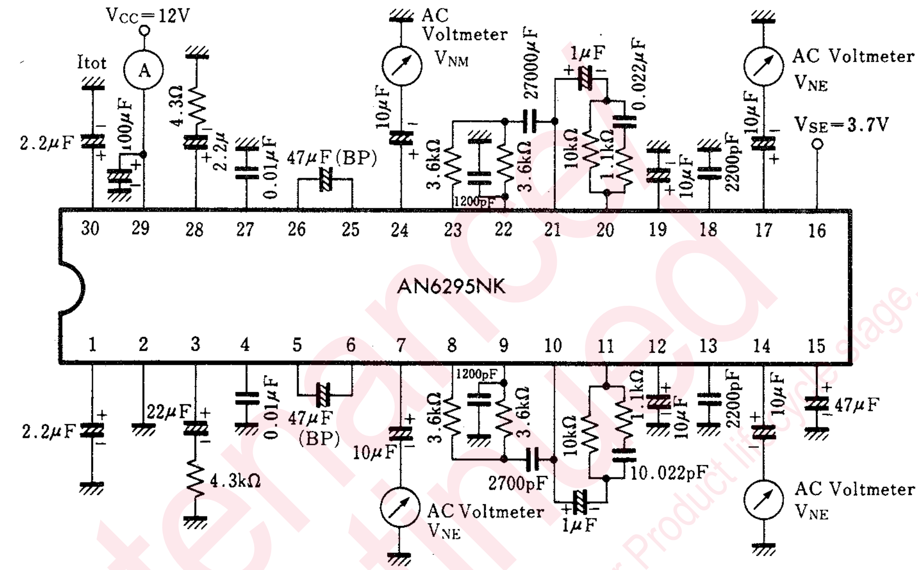
■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	14.4	V
Supply Current	I_{CC}	40	mA
Power Dissipation	P_D	560	mW
Operating Ambient Temperature	T_{opr}	−20~+75	℃
Storage Temperature	T_{stg}	−55~+125	℃

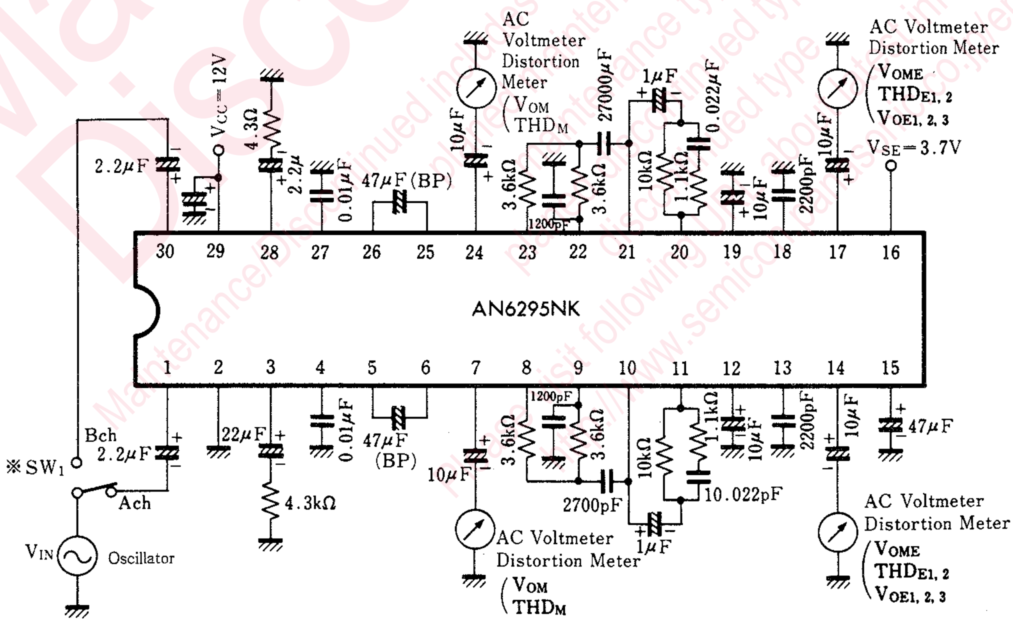
■ Electrical Characteristics (Vcc=12V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Current	I_{CQ}	1	Encord, Input: GND		17	23	mA
Encode Holding Voltage	V_{SE}			3.7			V
Decode Holding Voltage	V_{SD}					1.1	V
Encode Maximum Output Voltage	V_{OME}	2	f=1kHz, THD=3%	0	2		dBV
Decode Maximum Output Voltage	V_{OMD}	4	f=1kHz, THD=3%	0	5		dBV
Encode Harmonic Distortion−1	THD_{E1}	2	V_{IN}=1kHz, −22kBV		0.25	0.4	%
Encode Harmonic Distortion− 2	THD_{E2}	2	V_{IN}=10kHz, −22dBV		0.8	1	%
Decode Harmonic Distortion− 1	THD_{D1}	4	V_{IN}=1kHz, −15dBV		0.15	0.3	%
Decode Harmonic Distortion-- 2	THD_{D2}	4	V_{IN}=1kHz, −10.5dBV		0.6	1	%
Encode Noise Output Voltage	V_{NE}	1	Input: GND, DIN AUDIO		−54	−50	dBV
Decode Noise Output Voltage	V_{ND}	3	Input: GND, DIN AUDIO		−104	−100	dBV
Encode Output Voltage− 1	V_{OE1}	2	V_{IN}=1kHz, −22dBV	−14	−12	−10	dBV
Encode Output Voltage− 2	V_{OE2}	2	V_{IN}=1kHz, −62dBV	−36	−33	−30	dBV
Encode Output Voltage− 3	V_{OE3}	2	V_{IN}=1kHz, −82dBV	−47	−43	−41	dBV
Decode Output Voltage− 1	V_{OD1}	4	V_{IN}=1kHz, −15dBV	−24	−22	−20	dBV
Decode Output Voltage− 2	V_{OD2}	4	V_{IN}=1kHz, −35dBV	−63	−62	−57	dBV
Dncode Output Voltage− 3	V_{OD3}	4	V_{IN}=1kHz, −54dBV	−84	−82	−76	dBV
Encode Monitor Output Voltage	V_{OM}	2	V_{IN}=1kHz, −22dBV	−23.5	−22	−20.5	dBV
Encode Monitor Output Distortion	THD_M	2	V_{IN}=1kHz, −22dBV		0.03	0.1	%
Encode Monitor Output Noise Voltage	V_{NM}	2	Input: GND, DIN AUDIO		−104	−100	dBV
Encode Crosstalk	CT_E	5	V_{IN}=1kHz, −5dBV to Encode Input		−49	−46	dBV
Decode Crosstalk	CT_D	6	V_{IN}=1kHz, −15dBV		−75	−70	dBV
Encode Channel Balance	CB_E	2	V_{IN}=1kHz, −22dBV	−1.5	0	1.5	dB
Decode Channel Balance	CB_D	4	V_{IN}=1kHz, −15dBV	−2	0	2	dB
Encode Channel Separation	SEP_E	7	V_{IN}=1kHz, −22dBV		−53	−48	dBV
Decode Channel Separation	SEP_D	8	V_{IN}=1kHz, −15dBV		−95	−85	dBV
Operating Supply Voltage	V_{opr}			11.5	12	12.5	V
Encode Input Impedance	Z_{INE}	9	f=1kHz		30		kΩ
Decode Input Impedance	Z_{IND}	10	f=1kHz		5		kΩ
Encode Frequency Characteristic	V_{OE} (10k/1k)	11	V_{IN}=−20dBV, f=Ratio of 1kHz to 10kHz	3.2	4.2	5.2	dB
Decode Frequency Characteristic	V_{OD} (10k/1k)	12	V_{IN}=−15dBV, f=Ratio of 1kHz to 10kHz	−10.7	−8.7	−6.7	dB

Test Circuit 1 (I_{CQ}, V_{NE})

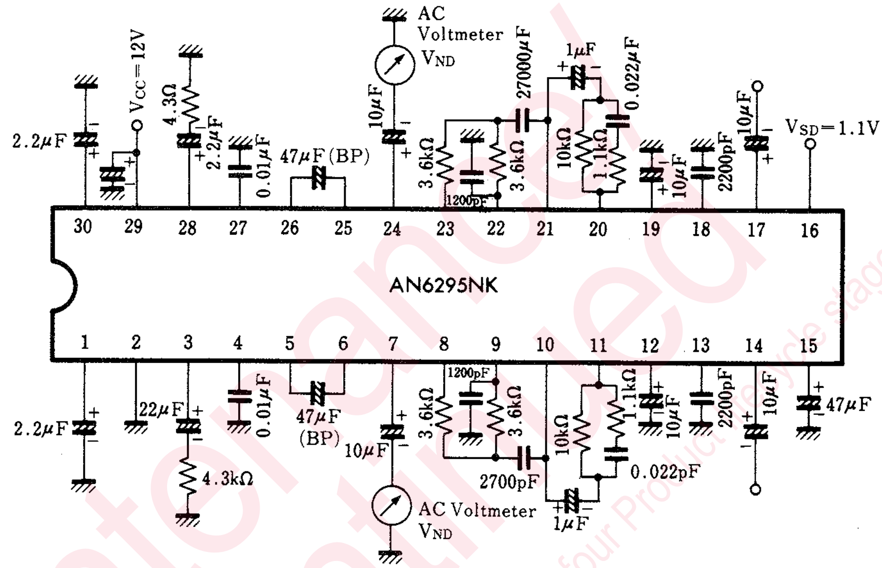


Test Circuit 2 (V_{OME}, THD_{E1}, THD_{E2}, V_{OE1}, V_{OE2}, V_{OE3}, V_{OM}, THD_M, V_{NM}, CB_E)

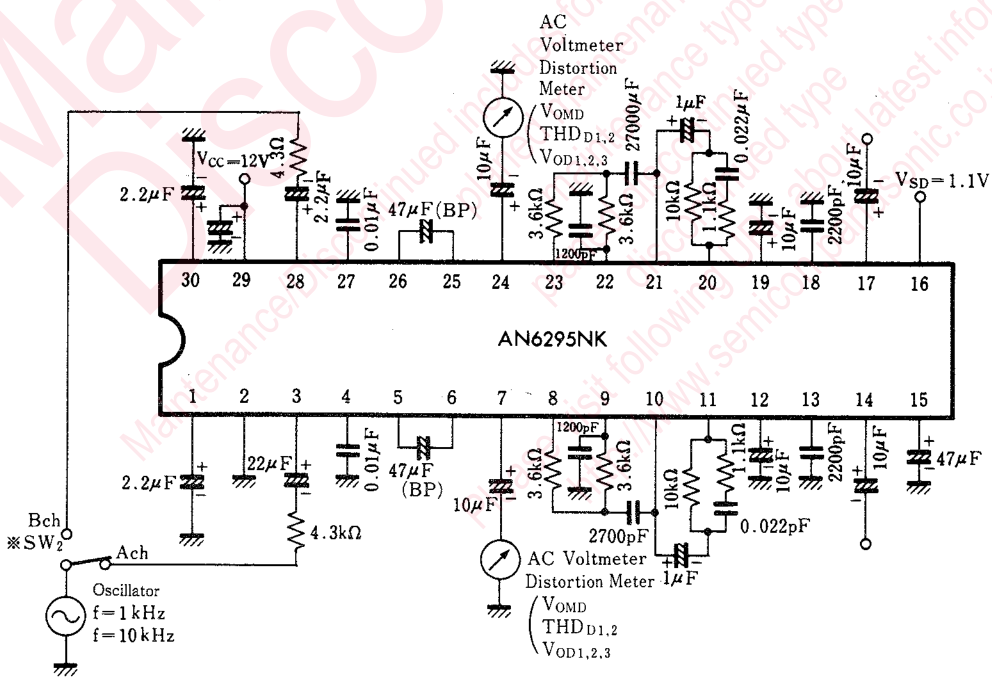


※SW1 is set at A when Ach is measured and B when Bch is measured.

Test Circuit 3 (V_{ND})

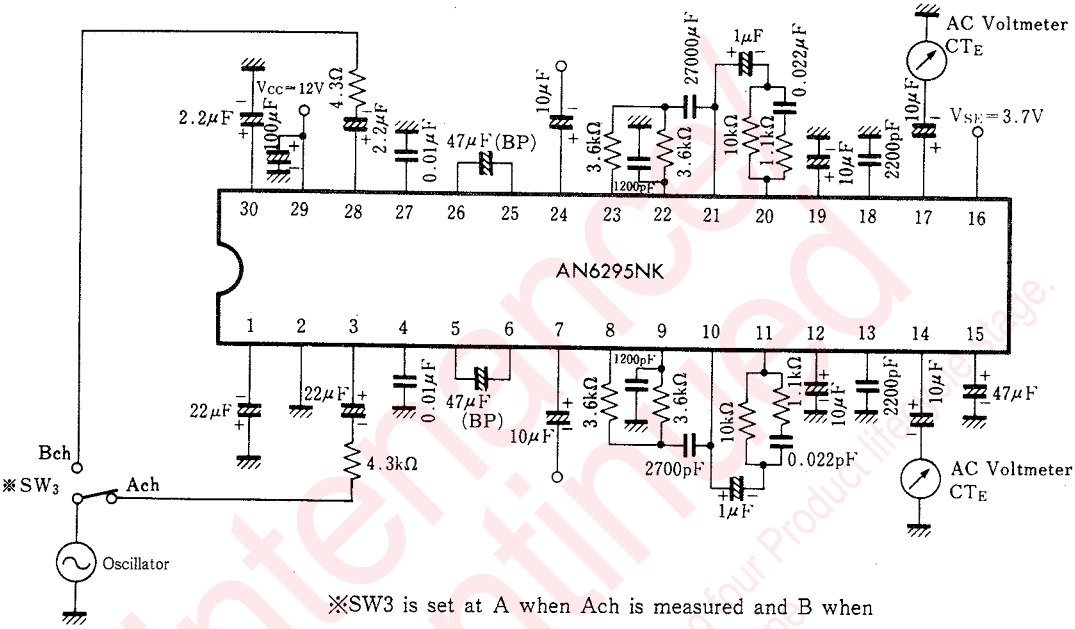


Test Circuit 4 (V_{OMD}, THD_1, THD_2, V_{OD1}, V_{OD2}, V_{OD3}, CB_D)



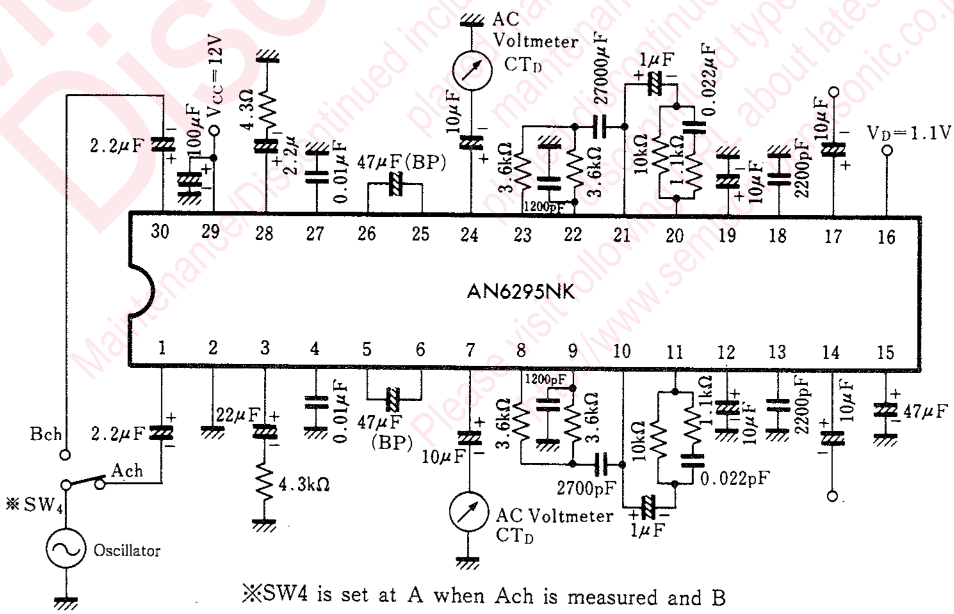
※SW2 is set at A when Ach is measured and B when Bch is measured.

Test Circuit 5(CT_E)



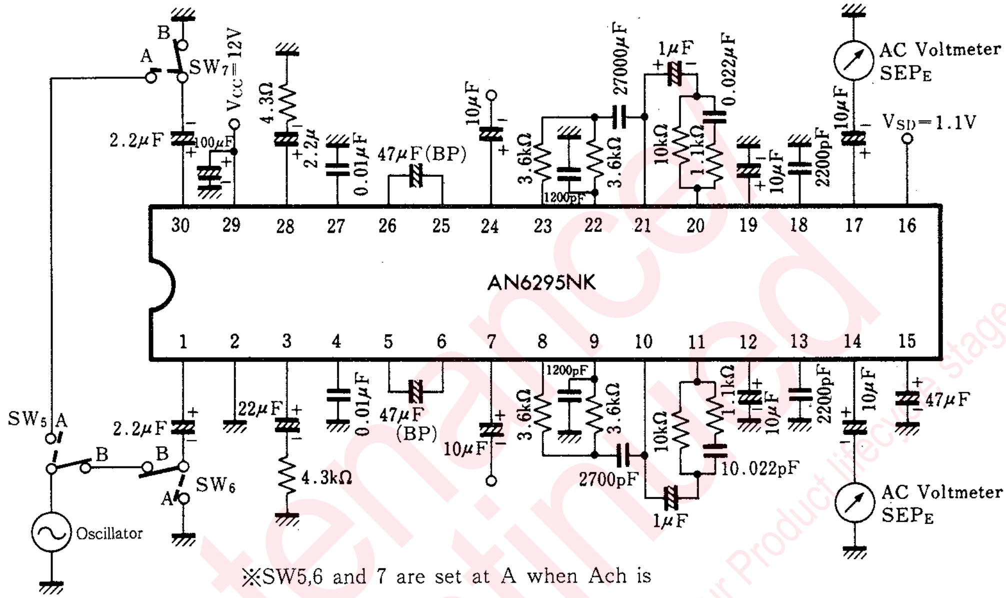
※SW3 is set at A when Ach is measured and B when Bch is measured.

Test Circuit 6(CT_D)



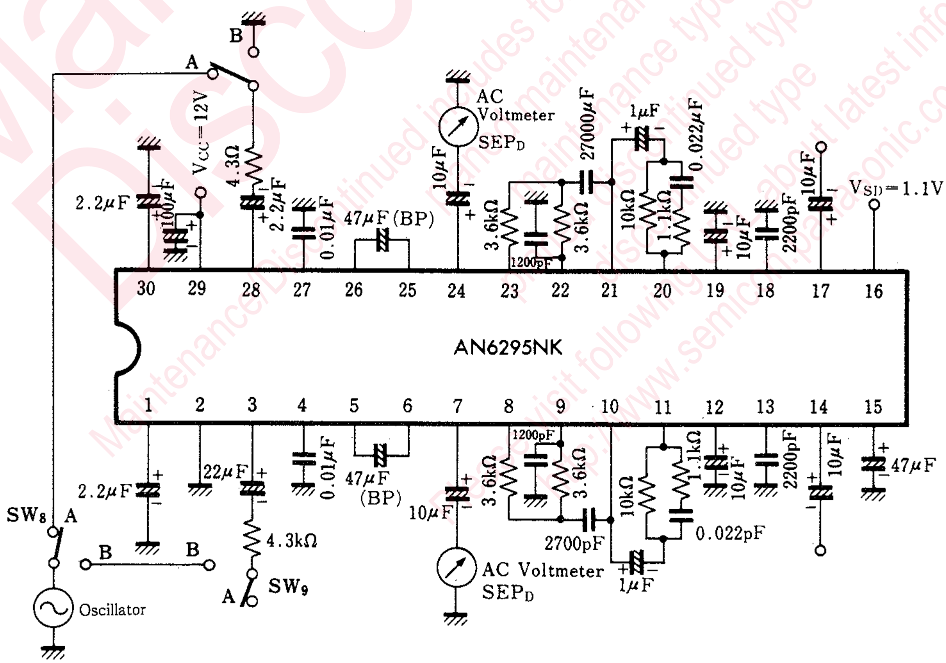
※SW4 is set at A when Ach is measured and B when Bch is measured.

Test Circuit 7 (SEP_E)



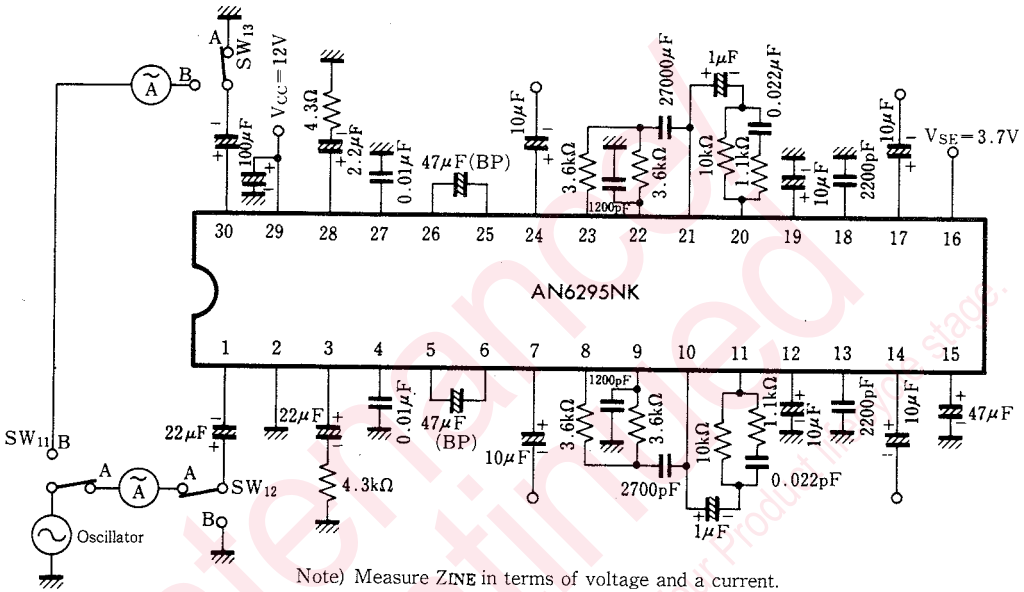
※SW5,6 and 7 are set at A when Ach is measured and B when Bch is measured.

Test Circuit 8 (SEP_D)



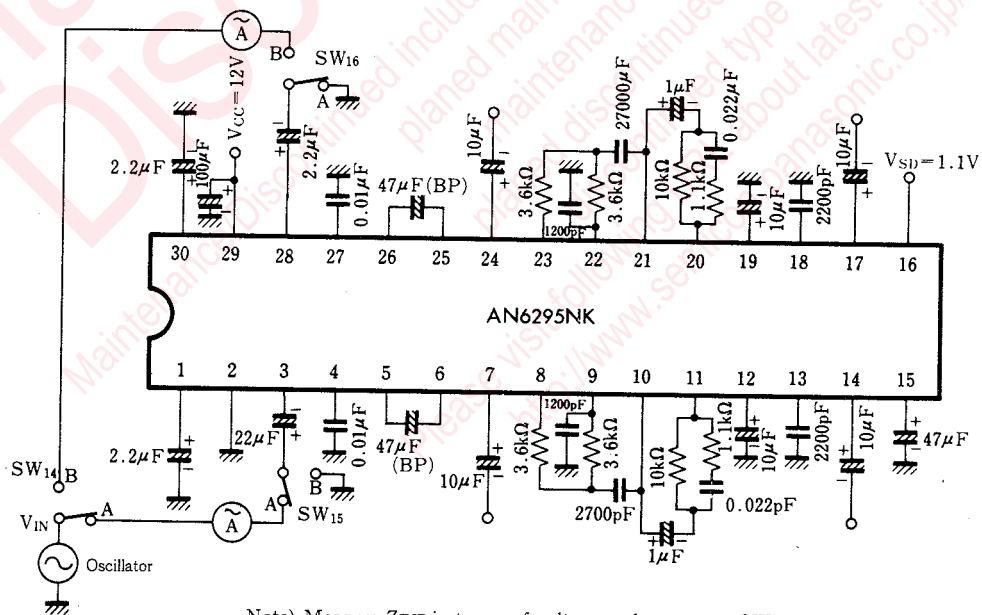
※SW8,9 and 10 are set at A when Ach is measured and B when Bch is measured.

Test Circuit 9 (Z_{INE})



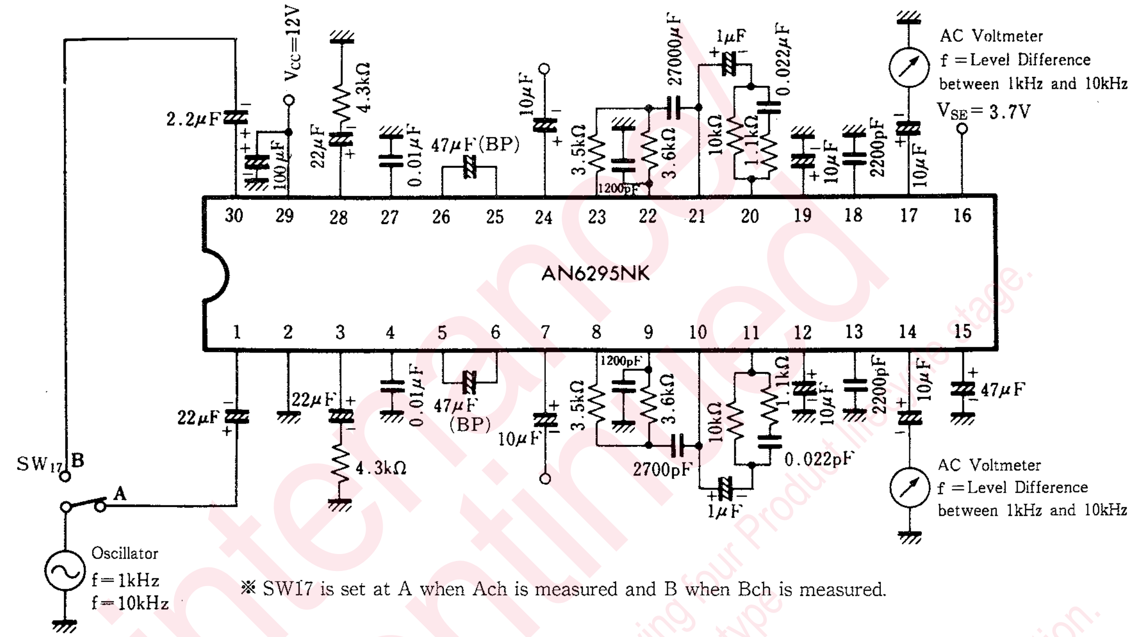
Note) Measure Z_{INE} in terms of voltage and a current.
SW11, 12, and 13 are set at A when Ach is measured and B when Bch is measured.

Test Circuit 10 (Z_{IND})



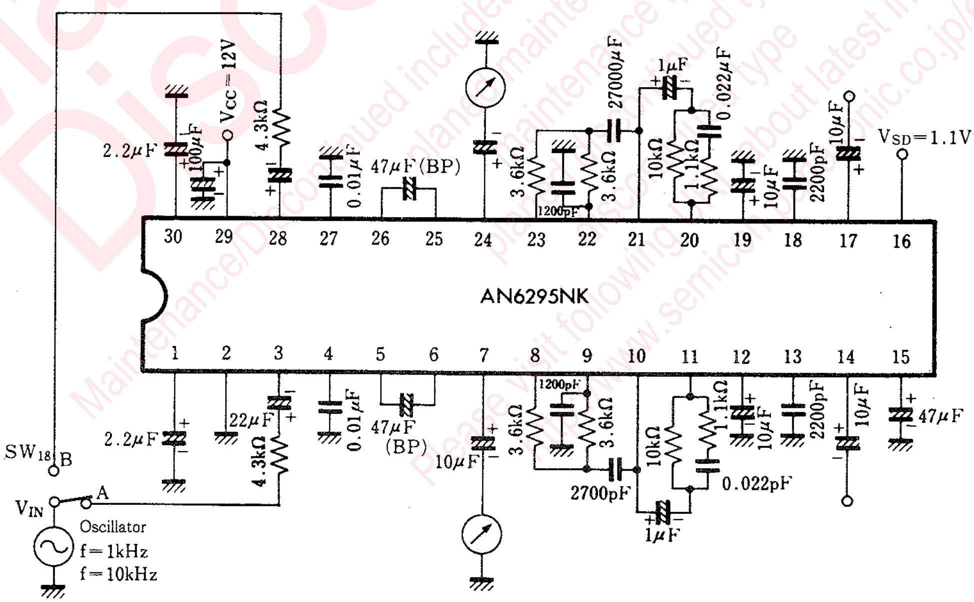
Note) Measure Z_{IND} in terms of voltage and a current. SW14, 15 and 16 are set at A when Ach is measured and B when Bch is measured.

Test Circuit 11 (V_{OE} (10k/1k))



※ SW17 is set at A when Ach is measured and B when Bch is measured.

Test Circuit 12 (V_{OD} (10k/1k))

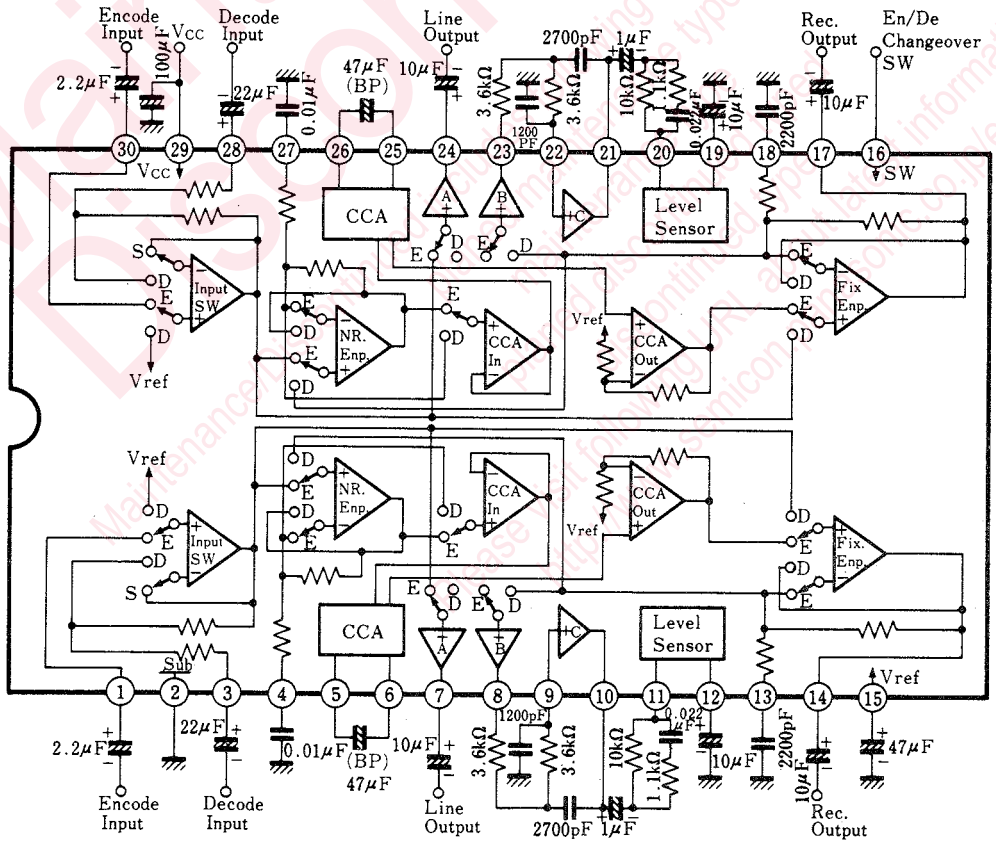


※SW18 is set at A when Ach is measured and B when Bch is measured.
Note) The percentage of errors of the capacitance for time constants must be within ±2%.

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Encode Input (Ach)	16	E_n/D_e Changeover SW
2	GND	17	Rec Output (Bch)
3	Decode Input (Ach)	18	Output Emphasis (Bch)
4	NR Emphasis (Ach)	19	Timing Capacitor (Bch)
5	CCA Gain Cell Output (Ach)	20	Level Sensor Input (Bch)
6	CCA Amp. Input (Ach)	21	Filter Amp. Output (Bch)
7	Line Output (Ach)	22	Filter Amp. Input (Bch)
8	Buffer Amp. Output (Ach)	23	Filter Amp. Output (Bch)
9	Filter Amp. Input (Ach)	24	Line Output (Bch)
10	Filter Amp. Output (Ach)	25	CCA Amp. Input (Bch)
11	Level Sensor Input (Ach)	26	CCA Gain Cell Output (Bch)
12	Timing Emphasis (Ach)	27	NR Emphasis (Bch)
13	Output Emphasis (Ach)	28	Decode Input (Bch)
14	Rec Output (Ach)	29	V_{CC}
15	Reference Voltage	30	Encode Input (Bch)

■ Application Circuit



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