

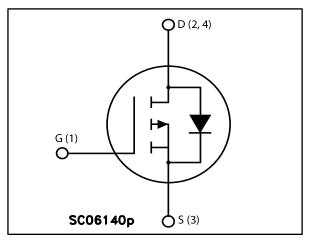
STL42P4LLF6

P-channel 40 V, 0.016 Ω typ., 10 A STripFET[™] VI DeepGATE[™] Power MOSFET in a PowerFLAT[™] 5x6 package

Datasheet - target specification

PowerFLAT™5x6

Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	ID	Ртот
STL42P4LLF6	40 V	0.022 Ω	10 A	4.8 W

- R_{DS(on)}* Q_gindustry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET[™] DeepGATE[™] technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL42P4LLF6	42P4LLF6	PowerFLAT [™]	Tape and
		5x6	reel

For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

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This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V _{GS}	Gate-source voltage	± 20	V
ا _D ⁽¹⁾	Drain current (continuous) at $T_C = 25 \ ^\circ C$	42	А
ا _D ⁽¹⁾	Drain current (continuous) at $T_c = 100 \ ^\circ C$	29	
۱ _D ⁽²⁾	Drain current (continuous) at $T_{pcb} = 25 \text{ °C}$	10	
۱ _D ⁽²⁾	Drain current (continuous) at T _{pcb} = 100 °C	7.5	А
I _D ⁽¹⁾⁽³⁾	Drain current (pulsed)	168	А
I _{DM} ⁽²⁾⁽³⁾	⁽²⁾⁽³⁾ Drain current (pulsed)		А
Ртот ⁽¹⁾	Total dissipation at $T_c = 25 \ ^{\circ}C$	75	W
Ртот ⁽²⁾	$T^{(2)}$ Total dissipation at $T_{pcb} = 25 \text{ °C}$		W
	Derating factor		W/°C
T _{stg}	Storage temperature	- 55 to 175	°C
Tj	Max. operating junction temperature	150	°C

Notes:

 $^{(1)}\mbox{The}$ value is rated according to $R_{\mbox{thj-c}}$

 $^{(2)}\mbox{This}$ value is rated according to $R_{\mbox{thj-pcb}}$

 $\ensuremath{^{(3)}}\ensuremath{\mathsf{Pulse}}$ width is limited by safe operating area

Table 3: Thermal data

Symbol	Parameter		Unit
R _{thj-case}	Thermal resistance junction-case max	2.00	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb, single operation	31.3	°C/W

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, steady state



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.



2 Electrical characteristics

(T _C= 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS}=0,\ I_D=250\ \mu A$	40			V
I _{DSS}	Zero gate voltage	$V_{GS} = 0, V_{DS} = 40 V$			1	μA
	drain current	$V_{DS} = 40 \text{ V}, \text{ T}_{C} = 125 ^{\circ}\text{C}$			10	
I _{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20 V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1			V
R _{DS(on)}	Static drain-source	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$		0.016	0.022	Ω
	on-resistance	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.025	0.035	Ω

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance	$V_{DS} = 32 V$, f = 1 MHz, $V_{GS} = 0$	-	2300	-	pF
Coss	Output capacitance		-	325	-	pF
Crss	Reverse transfer capacitance		-	120	-	pF
Qg	Total gate charge	$V_{DD} = 32$ V, ID = 10 A, $V_{GS} = 4.5$ V	-	22	-	nC
Q _{gs}	Gate-source charge		-	TBD	-	nC
Q _{gd}	Gate-drain charge		-	TBD	-	nC

Table 5: Dynamic

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 32 V, I_D = 5 A,$	-	TBD	-	ns
tr	Rise time	R_{G} = 4.7 Ω , V_{GS} = 10 V	-	TBD	-	ns
t _{d(off)}	Turn-off delay time		-	TBD	-	ns
t _f	Fall time		-	TBD	-	ns



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.



Table	7:	Source	drain	diode
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Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		10	А
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		40	А
V _{SD} ⁽²⁾	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.1	V
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs	-	TBD		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 16 V, T _j = 150 °C	-	TBD		nC
I _{RRM}	Reverse recovery current		-	TBD		А

Notes:

 $^{(1)}\mbox{Pulse}$ width limited by safe operating area

 $^{(2)}\text{Pulsed:}$ pulse duration = 300 µs, duty cycle 1.5 %



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.



3 Test circuits

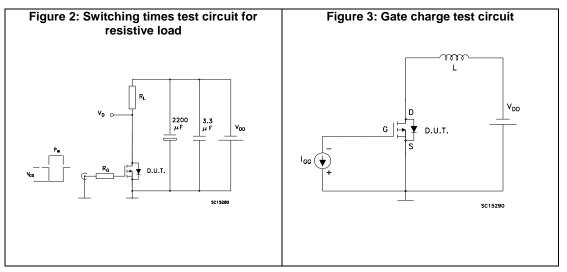
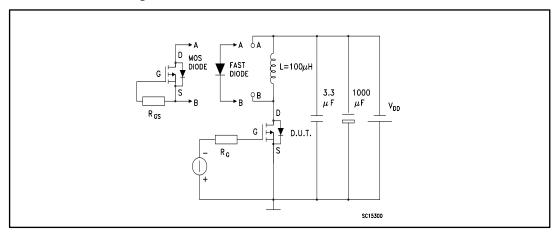


Figure 4: Source-drain diode forward characteristics





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 **PowerFLAT 5x6 type S-R package mechanical data**

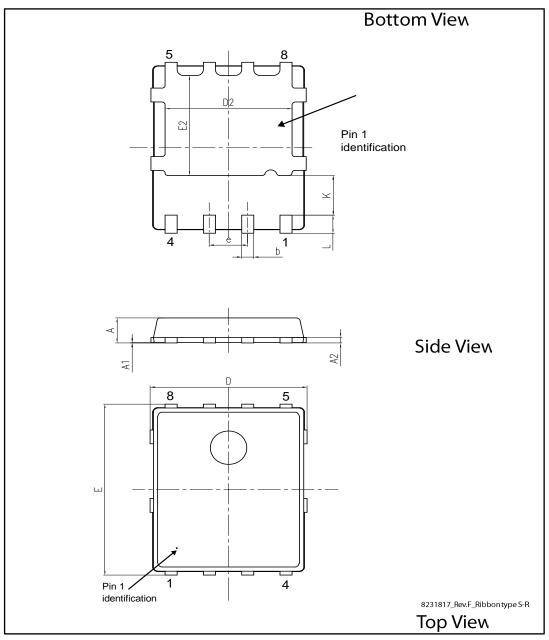


Figure 5: PowerFLAT™ 5x6 type S-R drawing

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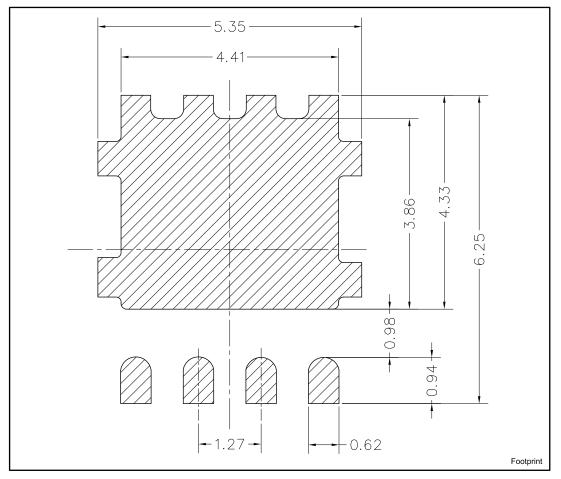


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Table 8: PowerFLAT 5x6 type S-R r	nechanical data
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D			
Dim.		mm	
	Min.	Тур.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
е		1.27	
L	0.60		0.80
К	1.275		1.575





5 Packaging mechanical data

5.1 PowerFLAT[™] 5x6 packaging mechanical data

Figure 7: PowerFLAT™ 5x6 tape (dimensions are in millimeters)

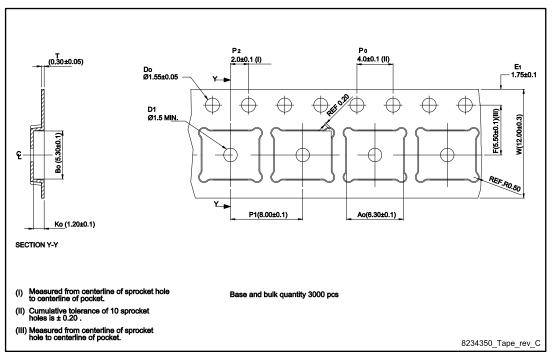
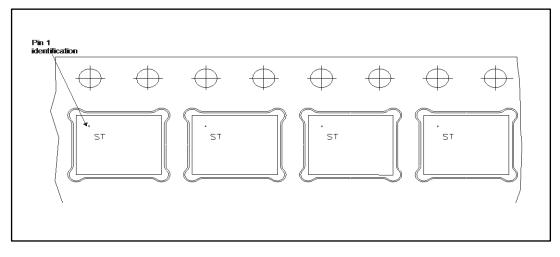
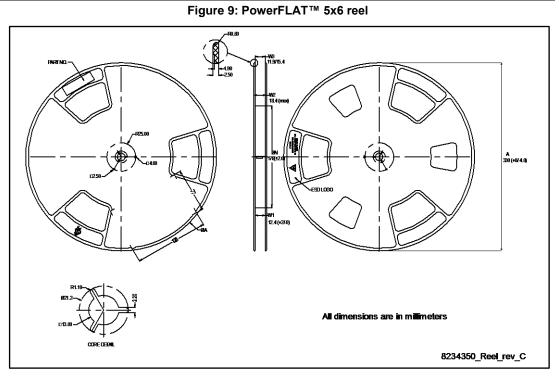


Figure 8: PowerFLAT™ 5x6 package orientation in carrier tape







6 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Jan-2014	1	First release.



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