

PUA3122 (PU3122)

Silicon NPN triple diffusion planar type darlington

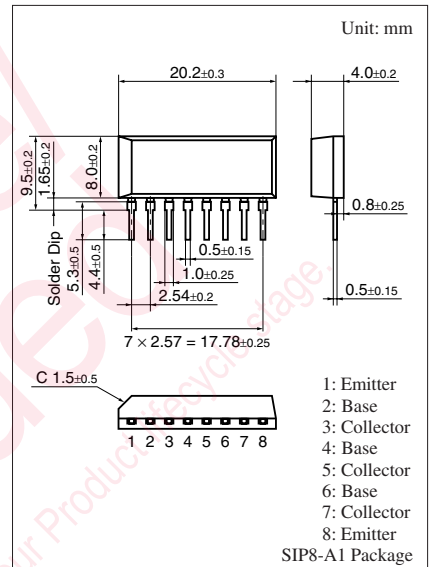
For power amplification

■ Features

- Built-in zener diode (30 V) between collector and base
- Small variation in withstand pressure
- Large energy handling capability
- High-speed switching
- NPN 3 elements

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	30 ± 5	V
Collector-emitter voltage (Base open)	V_{CEO}	30 ± 5	V
Emitter-base voltage (Collector open)	V_{EBO}	5	V
Collector current	I_C	4	A
Peak collector current	I_{CP}	8	A
Collector power dissipation	P_C	15	W
	$T_a = 25^\circ\text{C}$	2.4	
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$



■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

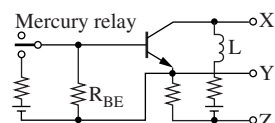
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = 5 \text{ mA}, I_B = 0$	25		35	V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 25 \text{ V}, I_E = 0$			100	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = 5 \text{ V}, I_C = 0$			2	mA
Forward current transfer ratio	h_{FE1}	$V_{CE} = 3 \text{ V}, I_C = 0.5 \text{ A}$	1000			—
	h_{FE2}^{*1}	$V_{CE} = 3 \text{ V}, I_C = 3 \text{ A}$	1000		10000	
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 3 \text{ A}, I_B = 12 \text{ mA}$			2.0	V
		$I_C = 5 \text{ A}, I_B = 20 \text{ mA}$			4.0	
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 3 \text{ A}, I_B = 12 \text{ mA}$			2.5	V
Transition frequency	f_T	$V_{CE} = 10 \text{ V}, I_C = 0.5 \text{ A}, f = 1 \text{ MHz}$		20		MHz
Turn-on time	t_{on}	$I_C = 3 \text{ A}$		0.3		μs
Storage time	t_{stg}	$I_{B1} = 12 \text{ mA}, I_{B2} = -12 \text{ mA}$		3.0		μs
Fall time	t_f	$V_{CC} = 20 \text{ V}$		1.0		μs
Energy handling capability ^{*2}	$E_{s/b}$	$I_C = 2 \text{ A}, L = 100 \text{ mH}, R_{BE} = 100 \Omega$	200			mJ

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: Rank classification

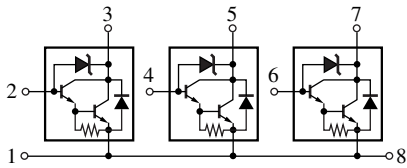
Rank	Free	P	Q
h_{FE}	1000 to 10000	2000 to 10000	1000 to 5000

*2: $E_{s/b}$ test circuit

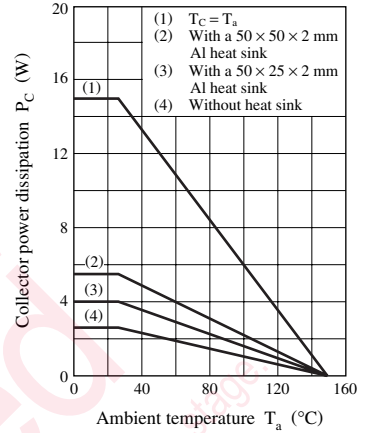


Note) The part number in the parenthesis shows conventional part number.

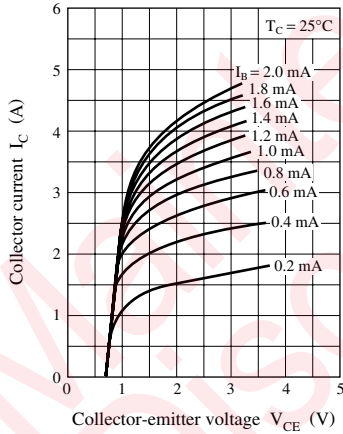
Internal Connection



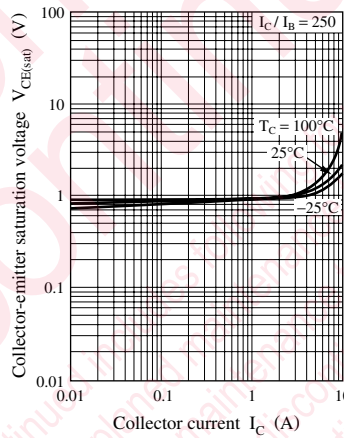
$P_C - T_a$



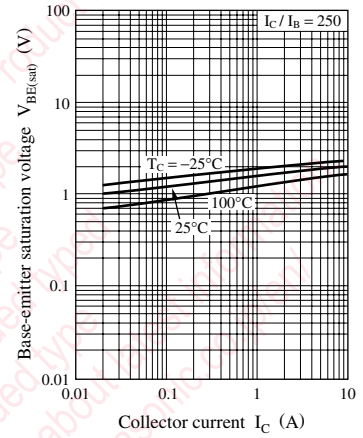
$I_C - V_{CE}$



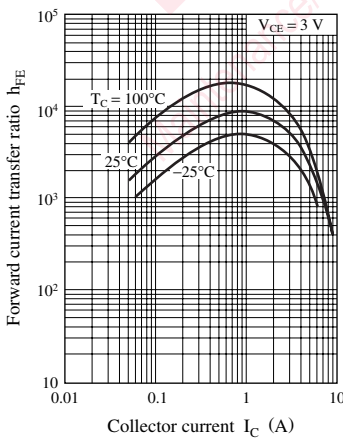
$V_{CE(sat)} - I_C$



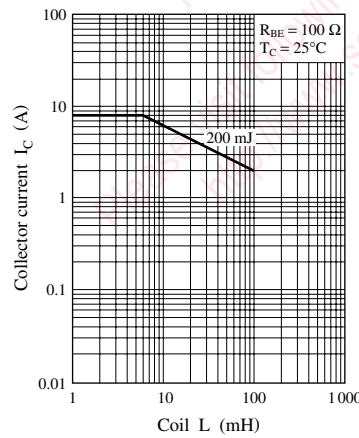
$V_{BE(sat)} - I_C$



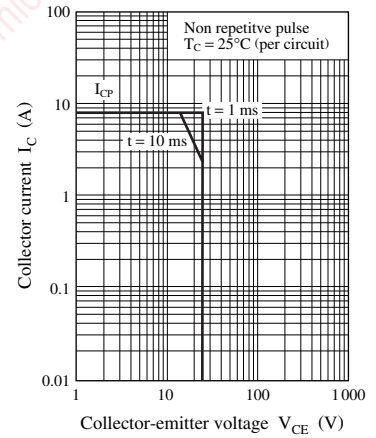
$h_{FE} - I_C$



Guidance load characteristic



Safe operation area



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