Fast CMOS Multilevel Pipeline Registers

Product Features:

- PI29FCT520T and PI29FCT521T are pinout and function compatible with IDT29FCT520/521, QS29FCT520/521 and AMD's Am29520/521
- Four 8-bit high-speed registers
- Hold, Transfer, and load instructions
- Dual two-level or single four-level pipeline operation
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive
  I_{OL} = 48 mA
- Extremely low static power (1 mW, typ.)
- Industrial operating temperature range: –40°C to +85°C
- FCT (2xxxT) has a 25Ω series resistor.
- Packages available:
  – 24-pin 300 mil wide plastic DIP (P24)
  – 24-pin 150 mil wide plastic QSOP (Q24)
  – 24-pin 150 mil wide plastic TQSOP (R24)
  – 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

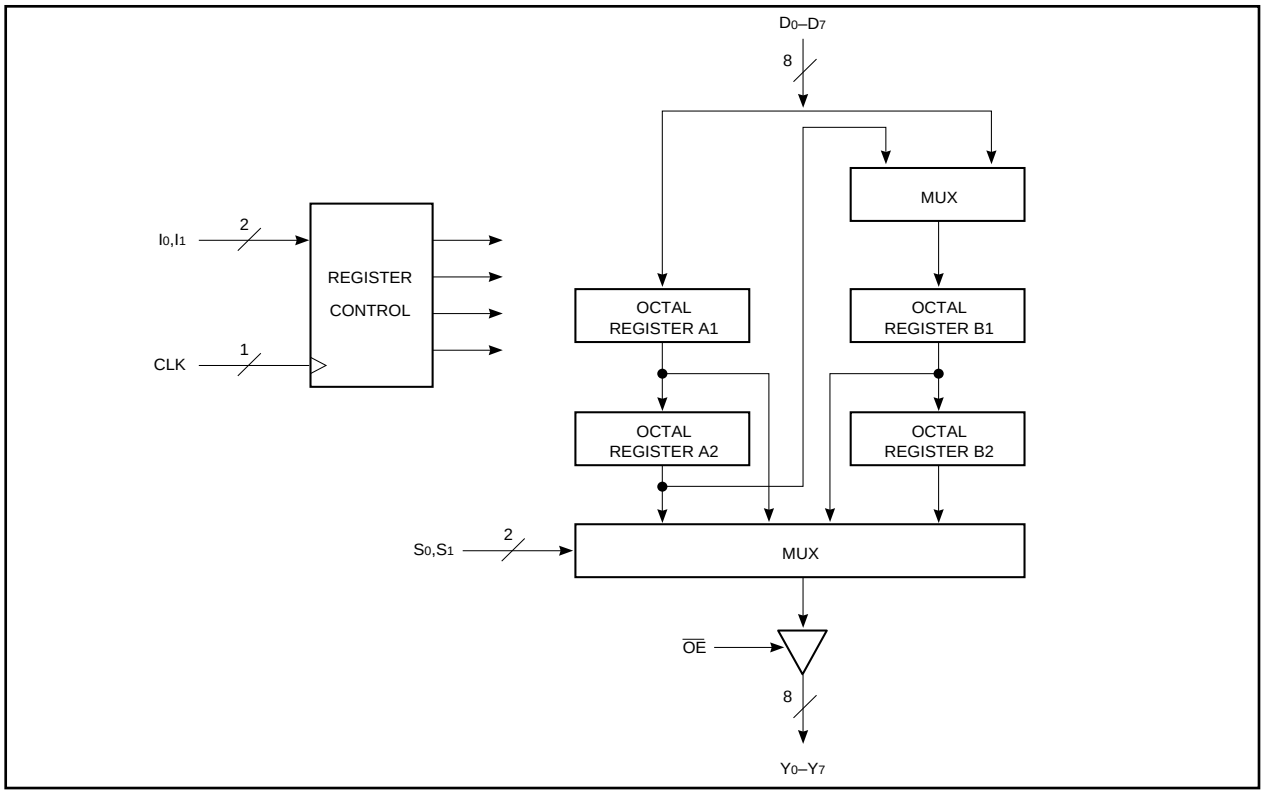
Pericom Semiconductor's PI29FCT series of logic circuits are pro-duced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI29FCT520T/2520T and PI29FCT521T are multilevel pipeline registers containing four 8-bit positive triggered registers which can be configured as a dual 2-level or a single 4-level pipeline. These products are designed for use as temporary storage or for storage delays in pipelined systems.

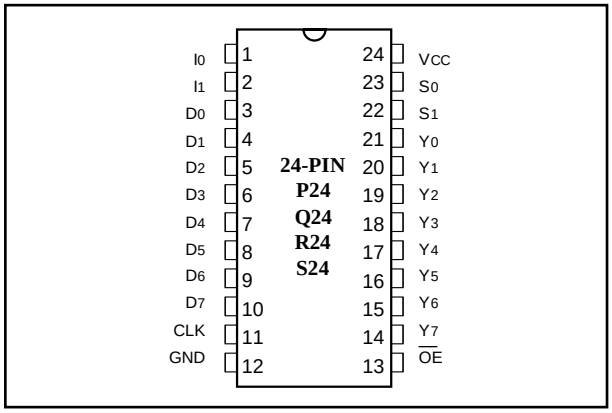
The PI29FCT521T differs from the PI29FCT520T/2520T only in the way data is loaded into and between registers in the dual 2-level operation. When data is entered into the first level (I = 2 or I = 1) of the PI29FCT520T/2520T, the existing data in the first level is moved to the second level. In the PI29FCT521T, these instructions simply overwrite the data in the first level. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0) causing the first level to change. In either part, I = 3 shift instruction puts the registers on hold.

Device models available upon request.

Logic Block Diagram



Product Pin Configuration



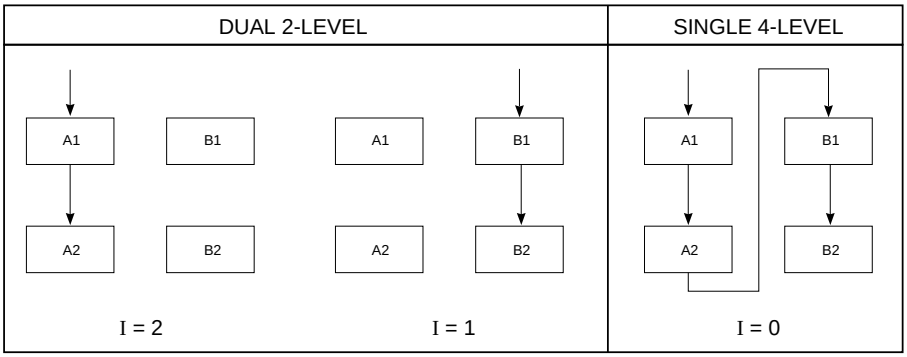
Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW) for 3-State Output Port
CLK	Clock Input. Enter data into registers on LOW-to-HIGH transistions
I0,I1	Instruction Inputs
S0,S1	Multiplexer Select. Inputs either register A1, A2, B1, or B2 data to be avaialbe at the output ports
Dx	Register Inputs
Yx	Register Outputs
GND	Ground
V_{CC}	Power

Register Selection

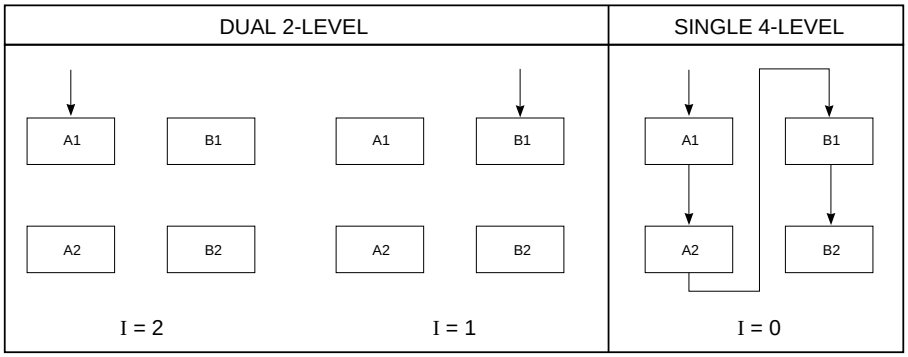
S1	S0	Register
0	0	B2
0	1	B1
1	0	A2
1	1	A1

PI29FCT520/T2520T Data Loading



NOTE: I = 3 FOR HOLD

PI29FCT521T Data Loading



NOTE: I = 3 FOR HOLD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.3	0.50	V
			I_{OL} = 12 mA (25Ω series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = GND V_{IN} = V_{CC}		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle	V_{IN} = GND V_{IN} = V_{CC}		1.5	3.5[5]	mA
		$\overline{OE}$ = GND One Bit Toggling f_I = 5 MH 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND		2.0	5.5[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle	V_{IN} = GND V_{IN} = V_{CC}		3.8	7.3[5]	
		$\overline{OE}$ = GND Eight Bits Toggling f_I = 5 MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND		6.0	16.3[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); all other inputs at VCC or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply characteristics.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guAranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

PI29FCT520T/2520T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT520AT/2520AT Com. Min	FCT520AT/2520AT Com. Max	FCT520BT/2520BT Com. Min	FCT520BT/2520BT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay CLK to Yx	C_L = 50 pF R_L = 500Ω	2.0	14.0	2.0	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay S0 or S1 to Yx		2.0	13.0	2.0	7.5	ns
t_{SU}	Setup Time HIGH or LOW Dx to CLK		5.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW Dx to CLK		2.0	—	2.0	—	ns
t_{SU}	Setup Time HIGH or LOW I0 or I1 to CLK		5.0	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yx		1.5	12.0	1.5	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Yx		1.5	15.0	1.5	7.5	ns
t_W	Clock Pulse Width[3] HIGH or LOW		7.0	—	5.5	—	ns

PI29FCT521T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT521AT Com. Min	FCT521AT Com. Max	FCT521BT Com. Min	FCT521BT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay CLK to Yx	C_L = 50 pF R_L = 500Ω	2.0	14.0	2.0	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay S0 or S1 to Yx		2.0	13.0	2.0	7.5	ns
t_{SU}	Setup Time HIGH or LOW Dx to CLK		5.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW Dx to CLK		2.0	—	2.0	—	ns
t_{SU}	Setup Time HIGH or LOW I0 or I1 to CLK		5.0	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yx		1.5	12.0	1.5	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Yx		1.5	15.0	1.5	7.5	ns
t_W	Clock Pulse Width[3] HIGH or LOW		7.0	—	5.5	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.