

The PE4141 is an ultra-high linearity passive broadband

operates with differential signals at all ports (RF, LO, IF),

capable of operation up to 1.0 GHz. This quad array

as digital controls, RF and IF port as single-ended or differential inputs/outputs. The PE4141 switches the

Quad MOSFET array with high dynamic range performance

allowing an analog multiplexer to be built that uses LO ports

differential input to the differential output at the LO switching

rate. Packaged in an 8-lead MSOP package, the PE4141 is

The PE4141 is manufactured on Peregrine's UltraCMOS™

process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance

of GaAs with the economy and integration of conventional

ideal for highly magnetic environments such as Magnetic

Product Description

Resonance Imaging (MRI).

Figure 1. Functional Diagram

CMOS.

LO2 0-

LO1 아

RF1 O-RF2 O-

Product Specification

PE4141

Ultra-linear UltraCMOS™ Broadband Quad MOSFET Array

Features

- Ultimate Quad MOSFET array
- Very high linearity
- Low magnetic
- Ideal for mixer applications
- Up/down conversion
- Low conversion loss
- High LO Isolation
- 8-lead MSOP package ideal for magnetic environments

Applications

The PE4141 is ideally suited for broadband analog multiplexer design in:

- Medical instrumentation
- Magnetic Resonance Imaging (MRI)
- Data acquisition and ADC/DAC muxing
- RF modulation/demodulation
- Precision instrumentation
- Analog or digital video switch matrices

Figure 2. Package Type

8-lead MSOP



Table 1. AC and DC Electrical Specifications @ +25 °C

Range ¹		DC		1.0	GHz
	V _{GS} = +3V, I _{DS} = 40 mA	260	320	380	mV
Match			12	40	mV
	V _{DS} = 0.1V; per ASTM F617-00		-100		mV
istance	V _{GS} = +3V, I _{DS} = 40 mA	6.5	7.75	9.5	Ω
5	Match sistance	V _{DS} = 0.1V; per ASTM F617-00	V_{DS} = 0.1V; per ASTM F617-00 sistance V_{GS} = +3V, I_{DS} = 40 mA 6.5	$V_{DS} = 0.1V$; per ASTM F617-00 -100 sistance $V_{GS} = +3V$, $I_{DS} = 40$ mA 6.5 7.75	$V_{DS} = 0.1V$; per ASTM F617-00 -100 sistance $V_{GS} = +3V$, $I_{DS} = 40$ mA 6.5 7.75 9.5

O IF1

O IF2

Document No. 70-0268-04 | www.psemi.com

©2010-11 Peregrine Semiconductor Corp. All rights reserved.



Figure 3. Pin Configuration (Top View)

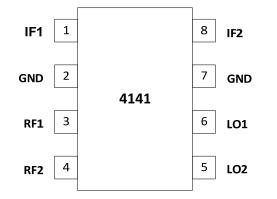


Table 2. Pin Descriptions

Pin No.	Pin Name	Description	
1	IF1	IF Output Connection (Drain)	
2	GND	Ground	
3	RF1	RF Input Connection (Source)	
4	RF2	RF Input Connection (Source)	
5	LO2	LO Input Connection (Gate)	
6	LO1	LO Input Connection (Gate)	
7	GND	Ground	
8	IF2	IF Output Connection (Drain)	

Table 3. Absolute Maximum Ratings

Symbol	Parameters/ Conditions	Min	Max	Units
T _{ST}	Storage temperature range	-65	150	°C
T _{OP}	Operating temperature range	0	70	°C
V _{DC + AC}	Maximum DC plus peak AC voltage across Drain- Source		±3.3	v
V _{DC+AC}	Maximum DC plus peak AC voltage across Gate- Drain or Gate-Source		±4.2	v
V_{ESD}	ESD Sensitive Device		100	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

This MOSFET device has minimally protected inputs and is highly susceptible to ESD damage. When handling this UltraCMOS[™] device, observe the same precautions that you would use with other ESD-sensitive devices.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS[™] devices are immune to latch-up.

Device Description

The performance level of this MOSFET array is made possible by the very high linearity afforded by Peregrine's UltraCMOS[™] process. The 8-lead MSOP package is suitable for highly magnetic applications including Magnetic Resonance Imaging (MRI.)

The PE4141 is an ideal MOSFET array core for a wide range of MOSFET array products, including module level solutions that incorporate baluns or other single-ended matching structures enabling three-port operation.

Marking

Packaged devices are marked with part number "4141", date code and lot code.



Evaluation Kit Figure 4. Evaluation Board Layout

Peregrine Specification 101-0157-00A

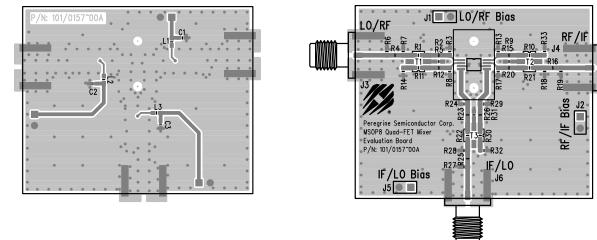
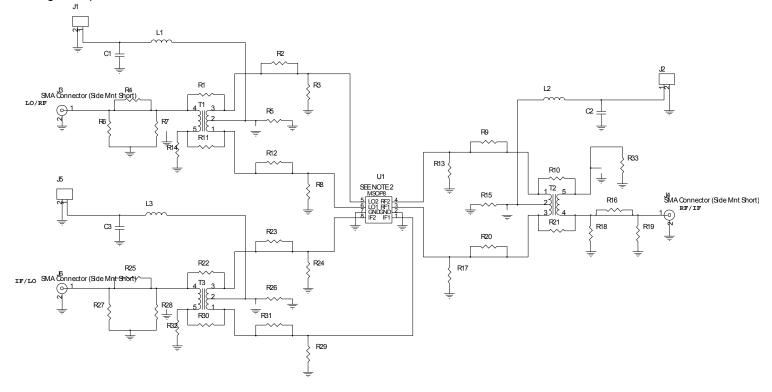


Figure 5. Evaluation Board Schematic

Peregrine Specification 102-0512-01



©2010-11 Peregrine Semiconductor Corp. All rights reserved.



Figure 6. Package Drawing

8-lead MSOP

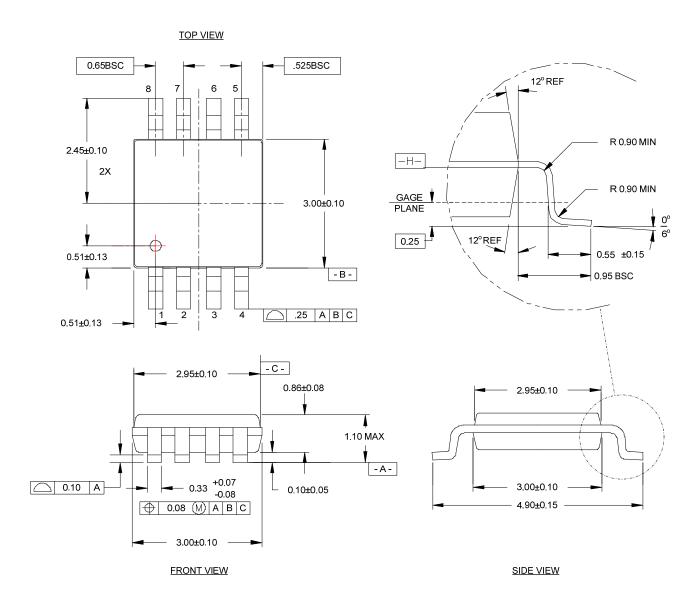




Figure 7. Tape and Reel Specification

8-lead MSOP

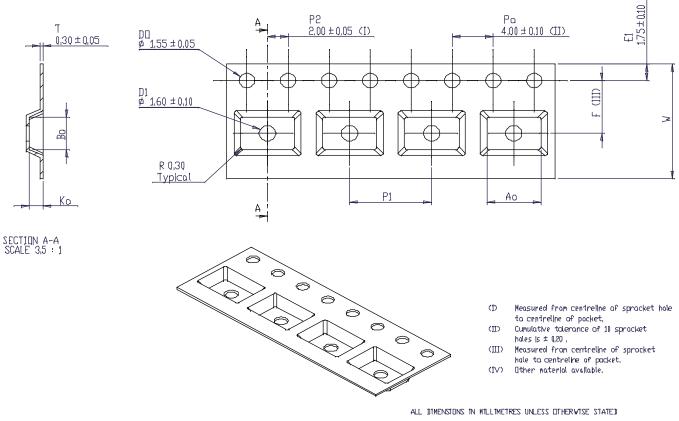


Table 4. Dimensions

Dimension	MSOP-8	
Ao	5.30 ± 0.1	
Bo	3.40 ± 0.1	
Ko	1.40 ± 0.1	
F	5.50 ± 0.05	
P ₁	8 ± 0.1	
W	12 ± 0.3	

Table 5. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4141-51	4141	PE4141G-08MSOP	Green 8-lead MSOP	Bulk or tape cut from reel
4141-52	4141	PE4141G-08MSOP-2000C	Green 8-lead MSOP	2000 units / T&R
4141-00	4141	PE4141-08MSOP-EK	Evaluation Kit	1 / Box

Sales Contact and Information

For Sales and contact information please visit <u>www.psemi.com</u>.

<u>Advance Information</u>: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. <u>Preliminary Specification</u>: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. <u>Product Specification</u>: The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo and UTSi are registered trademarks and UltraCMOS, HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.

Document No. 70-0268-04 | www.psemi.com

©2010-11 Peregrine Semiconductor Corp. All rights reserved.