

# MC100EP40

## 3.3V / 5V ECL Differential Phase-Frequency Detector

The MC100EP40 is a three-state phase-frequency detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. Advanced design significantly reduces the dead zone of the detector. For proper operation, the input edge rate of the R and V inputs should be less than 5 ns. The device is designed to work with a 3.3 V / 5 V power supply.

When Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

When Reference (R) and Feedback (FB) inputs are 80 ps or less in phase difference, the Phase Lock Detect pin will indicate lock by a high state ( $V_{OH}$ ). The  $V_{TX}$  ( $V_{TR}$ ,  $\overline{V_{TR}}$ ,  $V_{TFB}$ ,  $\overline{V_{TFB}}$ ) pins offer an internal termination network for 50  $\Omega$  line impedance environment shown in Figure 2. An external sinking supply of  $V_{CC}-2 V$  is required on  $V_{TX}$  pin(s). If you short the two differential  $V_{TR}$  and  $\overline{V_{TR}}$  (or  $V_{TFB}$  and  $\overline{V_{TFB}}$ ) together, you provide a 100  $\Omega$  termination resistance that is compatible with LVDS signal receiver termination. For more information on termination of logic devices, see AND8020.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu F$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

For more information on Phase Lock Loop operation, refer to AND8040.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

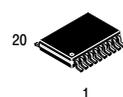
- Maximum Frequency > 2 GHz Typical
- Fully Differential
- Advanced High Band Output Swing of 400 mV
- Theoretical Gain = 1.11
- $T_{rise}$  97 ps Typical,  $F_{fall}$  70 ps Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0 V$  to  $5.5 V$  with  $V_{EE} = 0 V$
- NECL Mode Operating Range:  $V_{CC} = 0 V$  with  $V_{EE} = -3.0 V$  to  $-5.5 V$
- 50  $\Omega$  Internal Termination Resistor



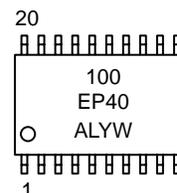
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### MARKING DIAGRAM



TSSOP-20  
DT SUFFIX  
CASE 948E



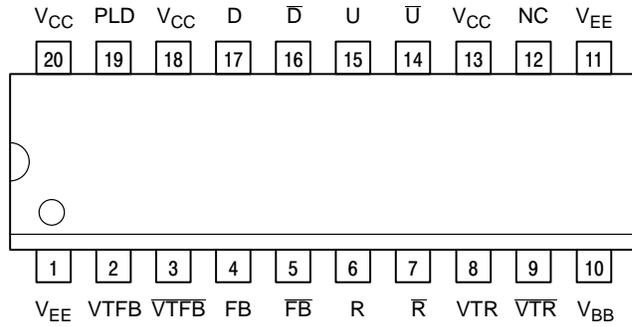
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC100EP40DT	TSSOP-20	75 Units/Rail
MC100EP40DTR2	TSSOP-20	2500 Tape & Reel

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

## PIN DESCRIPTION

PIN	FUNCTION
U, $\bar{U}$	ECL Up Differential Outputs
D, $\bar{D}$	ECL Down Differential Outputs
FB, $\bar{FB}$	ECL Feedback Differential Inputs
R, $\bar{R}$	ECL Reference Differential Inputs
PLD	ECL Phase Lock Detect Function
VTR	ECL Internal Termination for R
$\bar{VTR}$	ECL Internal Termination for $\bar{R}$
VTFB	ECL Internal Termination for FB
$\bar{VTFB}$	ECL Internal Termination for $\bar{FB}$
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
NC	No Connect

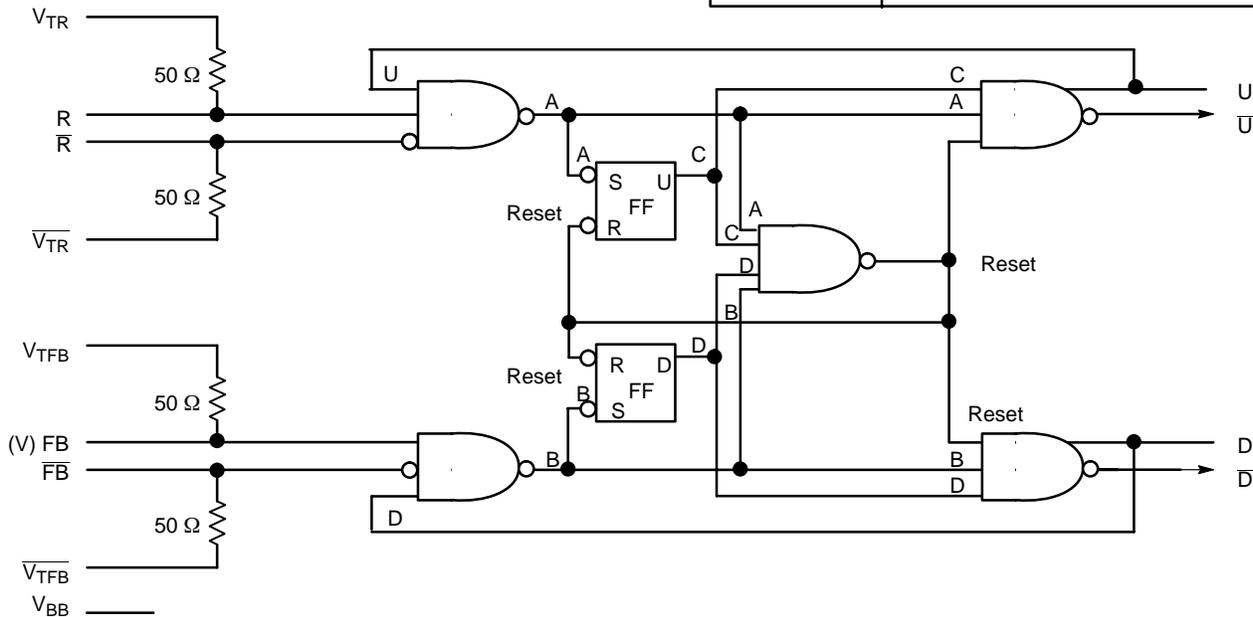


Figure 2. Logic Diagram

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 400 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	699 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

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## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 -6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	140 100	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	20 TSSOP	23 to 41	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

## 100EP DC CHARACTERISTICS, PECL V<sub>CC</sub> = 3.3 V, V<sub>EE</sub> = 0 V (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current	100	128	160	100	130	160	110	140	170	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 4) U, $\bar{U}$ , B, $\bar{B}$ PLD	2225 1355	2350 1480	2475 1605	2275 1355	2400 1480	2525 1605	2300 1355	2425 1480	2550 1605	mV
V <sub>OL</sub>	Output LOW Voltage (Note 4)	1775	1900	2025	1800	1925	2050	1825	1950	2075	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V <sub>BB</sub>	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	$\frac{D}{\bar{D}}$ 0.5 -150			0.5 -150			0.5 -150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

3. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.3 V to -2.2 V.

4. All loading with 50 ohms to V<sub>CC</sub>-2.0 volts.

5. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

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## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current (Note 7)	100	128	160	100	130	160	110	140	170	mA
$V_{OH}$	Output HIGH Voltage (Note 8)	3925	4050	4175	3975	4100	4225	4000	4125	4250	mV
$V_{OL}$	Output LOW Voltage (Note 8) U, $\bar{U}$ , B, $\bar{B}$ PLD	3475 3055	3600 3180	3725 3305	3500 3055	3625 3180	3750 3305	3525 3055	3650 3180	3775 3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
$V_{BB}$	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 9)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current D $\bar{D}$	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
7. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ ,  $5\ \Omega$  to  $10\ \Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC}-V_{EE}$  operation at  $\leq 3.3\text{ V}$ .
8. All loading with 50 ohms to  $V_{CC}-2.0$  volts.
9.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ ; $V_{EE} = -5.5\text{ V}$ to $-3.0\text{ V}$ (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current (Note 11)	100	128	160	100	130	160	110	140	170	mA
$V_{OH}$	Output HIGH Voltage (Note 12)	-1075	-950	-825	-1025	-900	-775	-1000	-875	-750	mV
$V_{OL}$	Output LOW Voltage (Note 12) U, $\bar{U}$ , B, $\bar{B}$ PLD	-1525 -1945	-1400 -1820	-1275 -1695	-1500 -1945	-1375 -1820	-1250 -1945	-1475 -1945	-1350 -1820	-1225 -1945	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{BB}$	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current D $\bar{D}$	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

10. Input and output parameters vary 1:1 with  $V_{CC}$ .
11. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ ,  $5\ \Omega$  to  $10\ \Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC}-V_{EE}$  operation at  $\leq 3.3\text{ V}$ .
12. All loading with 50 ohms to  $V_{CC}-2.0$  volts.
13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V to } -5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 3. $F_{max}/JITTER$ )		> 2			> 2			> 2		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential FB to D/U R to D/U	400	525	700	410	550	750	450	575	775	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter (See Figure 3. $F_{max}/JITTER$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$V_{PP}$	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) Q, $\bar{Q}$	60	85	130	75	110	150	80	120	160	ps

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to  $V_{CC}-2.0\text{ V}$ .

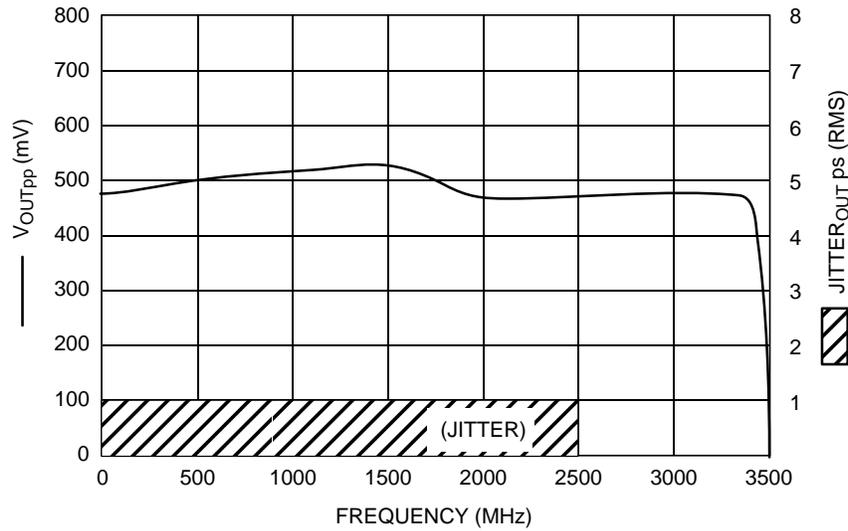


Figure 3.  $F_{max}/Jitter$

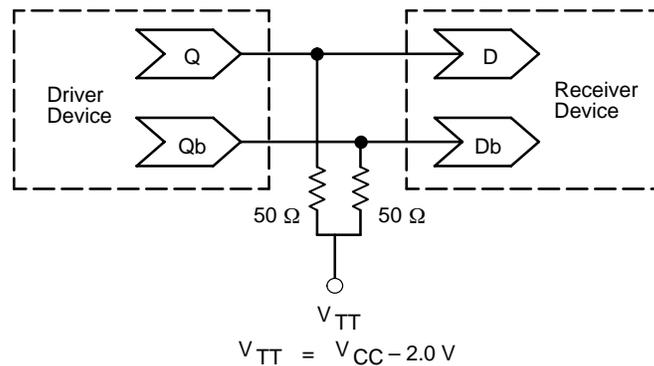


Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

## Resource Reference of Application Notes

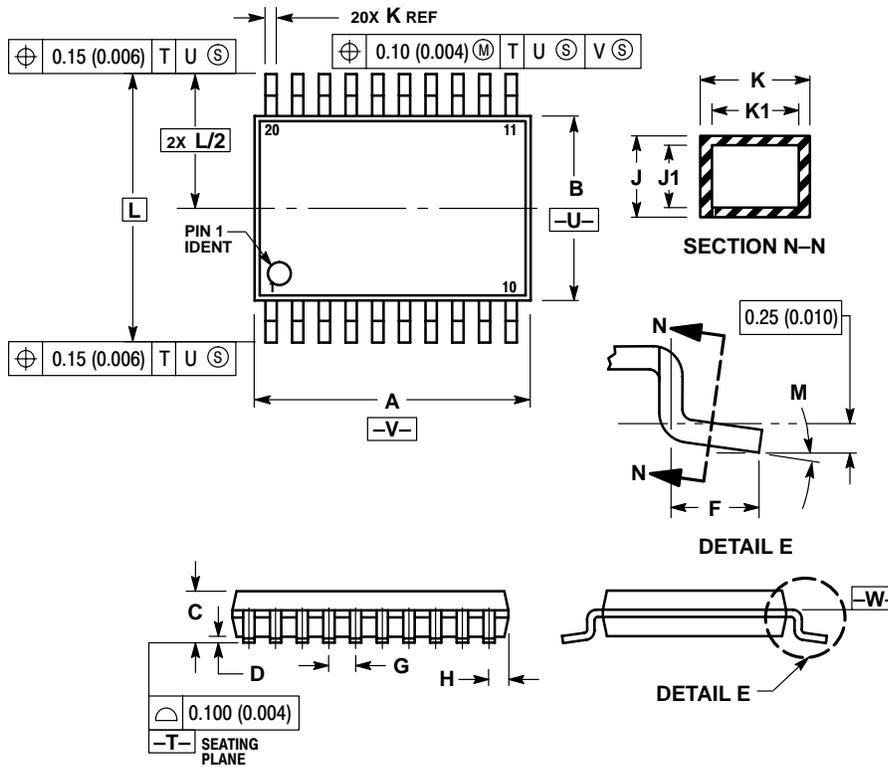
- AN1404** – ECLinPS Circuit Performance at Non–Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire–OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices
- AND8040** – Phase Lock Loop Operation

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

# MC100EP40

## PACKAGE DIMENSIONS

TSSOP-20  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948E-02  
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC100EP40

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