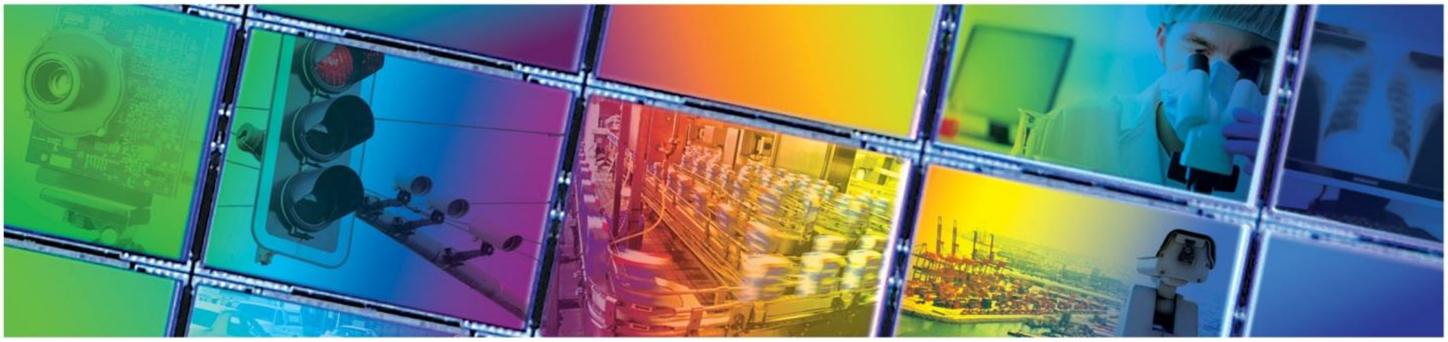
ON Semiconductor®

KAI-10100 IMAGE SENSOR

3648 (H) X 2760 (V) INTERLINE CCD IMAGE SENSOR



JUNE 4, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0027

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KAI-10100 Image Sensor

DESCRIPTION

The KAI-10100 Image Sensor is a 10 million pixel, 22.5mm diagonal (Four Thirds format) high performance color interline transfer CCD image sensor. Advanced 4.75 micron square pixels provide outstanding sensitivity and dynamic range, and overflow protection is provided in each pixel through the use of a vertical overflow drain.

The sensor employs a 4-field interlaced design for full resolution readout, or can be read as a progressive scan device using 1x2, 2x2, or 4x4 color binning modes. Use of these color binning modes provides significantly improved sensitivity and faster readout rates, making this sensor ideal for both Scientific and Photographic applications.

FEATURES

- High resolution with low noise
- High sensitivity and dynamic range
- On-sensor color binning for enhanced sensitivity and frame rate
- Electronic shutter

APPLICATIONS

- Intelligent Transportation Systems
- Photography
- Scientific

Parameter	Typical Value
Architecture	Interline CCD; Interlaced or Progressive Scan
Total Number of Pixels	3868 (H) x 2892 (V) = 11.1 M
Number of Effective Pixels	3776 (H) x 2856 (V) = 10.8 M
Number of Active Pixels	3760 (H) x 2840 (V) = 10.7 M
Pixel Size	4.75 µm (H) x 4.75 µm (V)
Active Image Size	17.86 mm (H) x 13.49 mm (V) 22.5 mm (diagonal)
Aspect Ratio	4:3
Number of Outputs	2
Output Sensitivity	32 µV/e
Saturation Signal	25,000 electrons
Quantum Efficiency R (630 nm), G (550 nm), B (470 nm)	32%, 42%, 40%
Total Noise	10 electrons
Dark Current (T= 40 °C)	0.06 nA/cm^2
Dark Current Doubling Temperature	7.5 °C
Dynamic Range	64 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	> 100X
Image Lag	5 e$^-$
Maximum Data Rate	30 MHz
Frame Rate Full Resolution (FA mode) 1x2 bin (3760 x 1420) (FB2 mode) 2x2 bin (1880 x 1420) (FB4 mode) 4x4 bin (940 x 710) (FD16 mode)	 5 fps 10 fps 10 fps 19 fps
Package	32-pin, CERDIP, 0.070” pin spacing
Cover Glass	Clear

All parameters above are specified at T = 20 °C, unless otherwise noted

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H2106	KAI-10100-CXC-CB-XA	Color (Bayer RGB), Special Microlens, CERDIP Package sidebrazed pins, Clear Cover Glass (no coatings), Standard Grade	KAI-10100-CXC (Lot Number)
4H2107	KAI-10100-CXC-CB-XE	Color (Bayer RGB), Special Microlens, CERDIP Package sidebrazed pins, Clear Cover Glass (no coatings), Engineering Grade	

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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E-mail: info@truesenseimaging.com

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Device Description

ARCHITECTURE

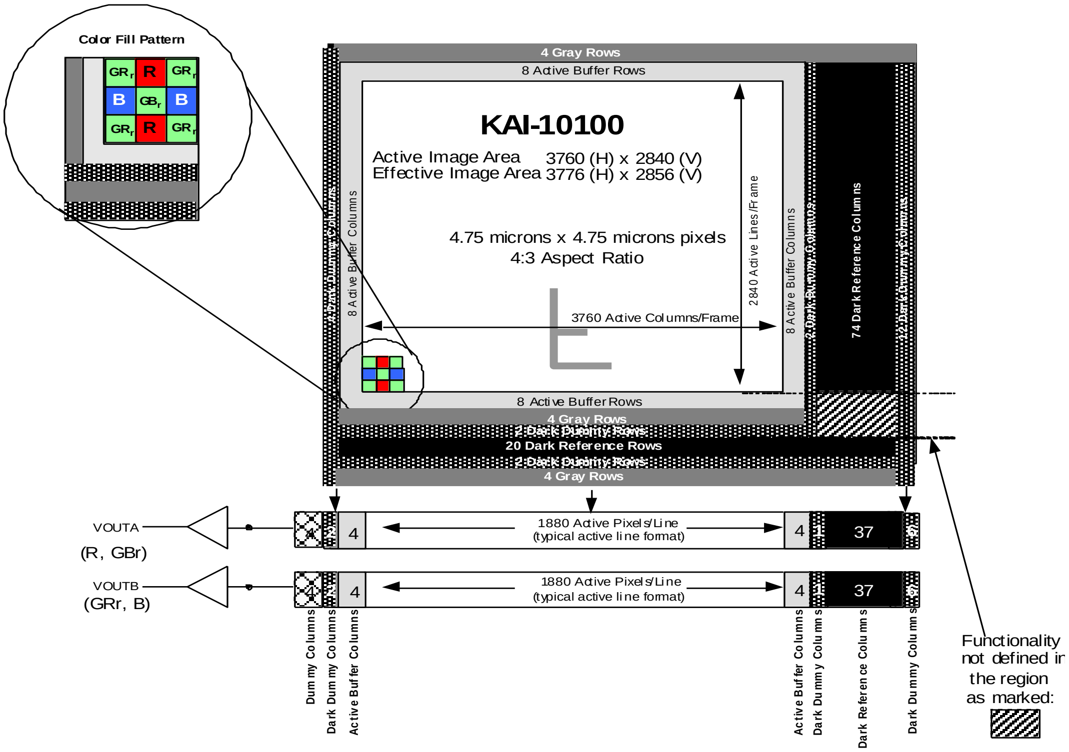


Figure 1: Block Diagram

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region are light shielded pixels that include 74 trailing dark pixels on every line. There are also 20 full dark lines at the start of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference. Surrounding each dark reference region are two columns (or rows) that are also light shielded pixels. These columns (or rows) may have some light leakage effects from surrounding pixels and therefore, should not be used as a dark reference.

The regions labeled gray are a combination of light shielded pixels and light sensitive pixels. These pixels should not be used as a dark reference. For every 5 columns in the gray region 4 columns are covered by lightshield and 1 column is open. These open columns are covered with blue color filter.

Eight buffer pixels contain a RGB mosaic color pattern. This region is classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Pixel

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Vertical to Horizontal Transfer

When the Vx timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped and HTG input must be High. H2 must be stopped in the high state while H1, H3, H4 and H4L must be stopped in the low state. The HCCD clocking may begin 15.6 nS after the falling edge of the HTG. Charge is transferred from the last V1 phase of the even column VCCD into HCCDA, while the charge from the last V1 phase of the odd columns is transferred into HCCDB.

Horizontal Register to Floating Diffusion

There are 2 HCCD's, each has a total of 1938 pixels. The EVEN vertical shift registers (columns) are shifted into HCCDA and the ODD vertical shift registers are shifted into HCCDB. At the beginning of each HCCD register there are 4 Dummy pixels, these pixels receive no charge from the vertical shift registers. The first 4 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 2 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 4 clock cycles will contain active buffer column signal. The image data is found in the next 1880 clock cycles which contain photo-electrons. Following the image data there will be another 4 buffer columns and 1 Dark Dummy column. Finally, there are 37 dark reference columns followed by the 6 more dark dummy columns. When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (Vx), and HTG should be not be pulsed. This prevents unwanted noise from being introduced

HORIZONTAL REGISTER

Output Structure

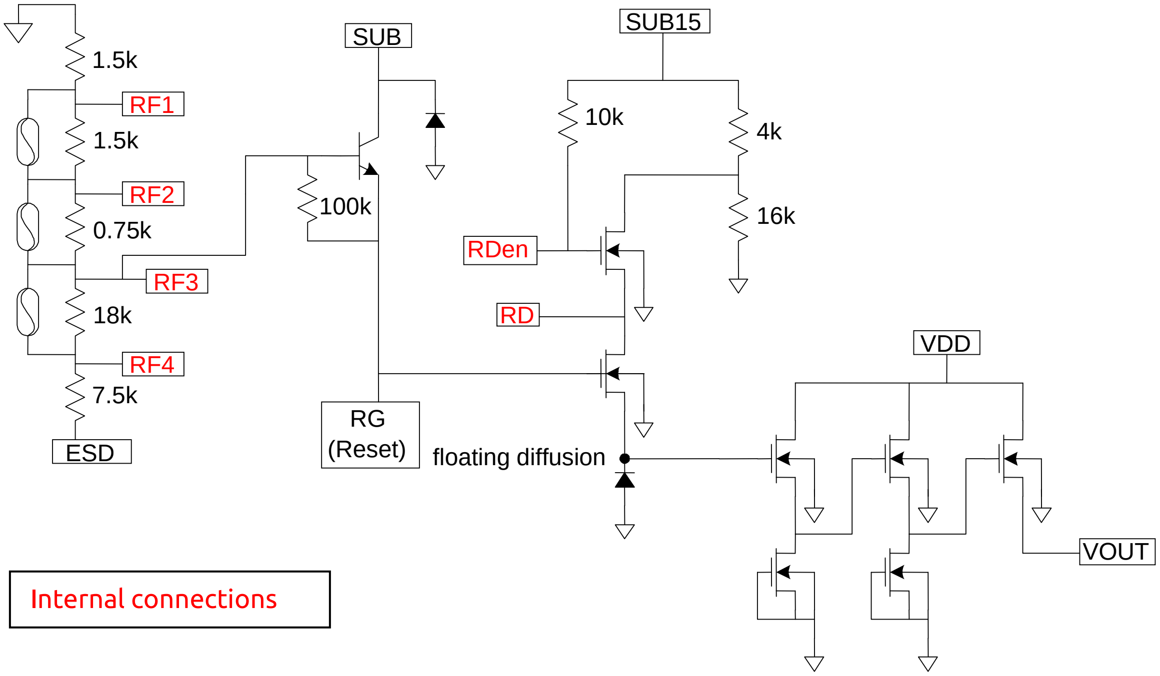


Figure 2: Output Architecture (each output)

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta Vfd = \Delta Q/Cfd$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron (μV/e^-). The dual parallel horizontal CCDs are presented a new line during the horizontal retrace period. H1, H3, H4 and H4L are held low while the vertical registers transfer the next line to the horizontal. H2 and HTG are held high. HTG shifts low then H1 taken high.

This shifts the charge in the Horizontal Registers forward one phase so the charge packets in the A and B registers are now aligned. Both horizontal CCD's then transport each line, pixel by pixel, to the A and B output structures by clocking the H1 and H2 pins alternately with the H3 and H4 pins in a complementary fashion. A separate connection to the last H4 phase (H4L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H4L a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier. After the signal has been sampled off chip, the reset clock (RG) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD), which is set on-chip.

RECOMMENDED CIRCUITS

Output Gate Bypass

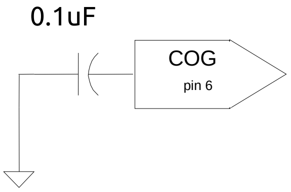


Figure 3: COG Circuit

Output Load

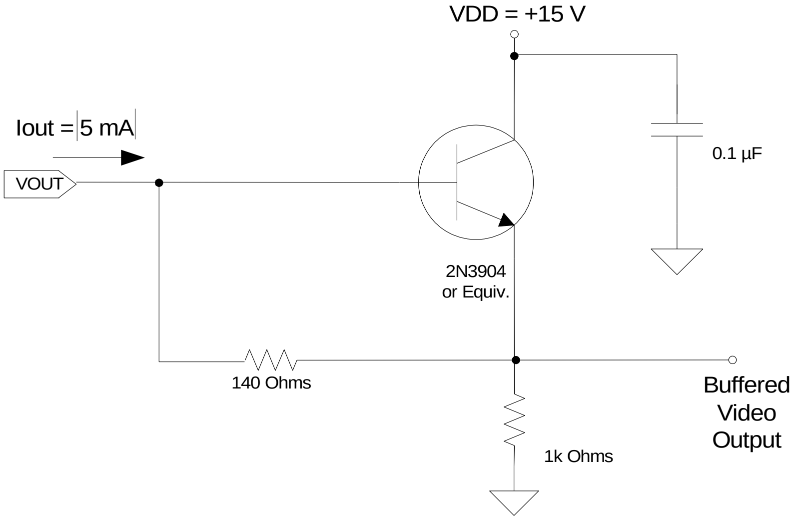


Figure 4: Recommended Output Structure Load Diagram.

Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

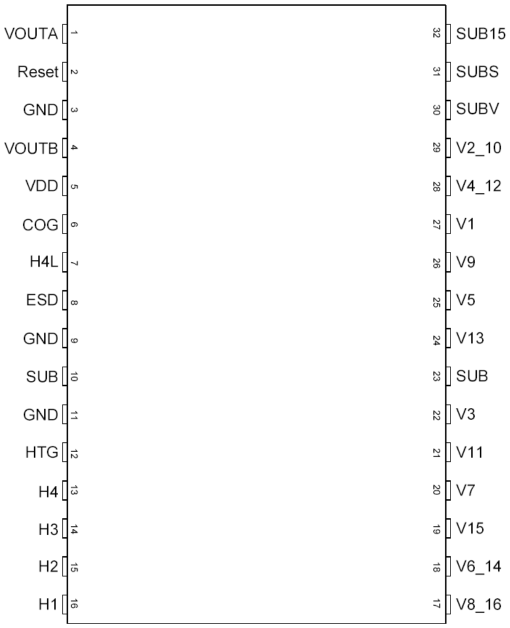


Figure 5: Pinout Diagram

Pin	Name	Description
1	VOUTA	Video Output A
2	RG	Reset Gate
3	GND	Ground
4	VOUTB	Video Output B
5	VDD	Amplifier Supply
6	COG	OG Bypass Capacitor
7	H4L	Last HCCD gate, same as H4
8	ESD	ESD circuit disable input
9	GND	Ground
10	SUB	Sensor Substrate Clock Input
11	GND	Ground
12	HTG	HCCD Transfer Gate
13	H4	HCCD Gate 4
14	H3	HCCD Gate 3
15	H2	HCCD Gate 2
16	H1	HCCD Gate 1

Pin	Name	Description
32	SUB15	Sub Voltage Reference Supply
31	SUBS	Sub Voltage Reference Still
30	SUBV	Sub Voltage Reference Video
29	V2-10	VCCD Gates 2 and 10
28	V4-12	VCCD Gates 4 and 12
27	V1	VCCD Gate 1
26	V9	VCCD Gate 9
25	V5	VCCD Gate 5
24	V13	VCCD Gate 13
23	SUB	Sensor Substrate Clock Input
22	V3	VCCD Gate 3
21	V11	VCCD Gate 11
20	V7	VCCD Gate 7
19	V15	VCCD Gate 15
18	V6-14	VCCD Gates 6 and 14
17	V8-16	VCCD Gates 8 and 16

Imaging Performance

TYPICAL OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Integration time (33msec) + Field Readout Time (treadout)	93 msec – field 1 153 msec – field 2 213 msec – field 3 273 msec – field 4	
Integration time (tint)	33 msec	Specified between the end of the electrical shutter pulse and the flush.
Horizontal clock frequency	30 MHz	
Light source (LED)	Red Green Blue Orange	
Mode	Eelectronic shutter – integrate – flush –f1 transfer read, f2 transfer read, readout cycles	
Temperature	20 °C (except where noted)	

SPECIFICATIONS

(FA mode, unless specified) KAI-10100-CXB Color with Microlens

Description		Symbol	Min.	Nom.	Max.	Units	Specified Temperature	Notes	Sample Plan[7]
Maximum Photoresponse Nonlinearity		NL	n/a	8		%		1, 2	Design
Maximum Gain Difference Between Outputs		ΔG	n/a	2		%		1, 2	Design
Max. Signal Error due to Nonlinearity Dif.		ΔNL	n/a	3		%		1, 2	Design
Horizontal CCD Charge Capacity		HNe		70		ke$^-$			Design
Vertical CCD Charge Capacity		VNe	TBD	50		ke$^-$			Die
Photodiode Charge Capacity		PNe	22.5	25		ke$^-$			Die
Horizontal CCD Charge Transfer Efficiency		HCTE	0.99999		n/a				Design
Vertical CCD Charge Transfer Efficiency		VCTE	0.99999		n/a				Design
Photodiode Dark Current		Ipd	n/a	3	50	e/p/s	40		Die
Photodiode Dark Current		Ipd	n/a	.06		nA/cm^2	40		Die
Vertical CCD Dark Current		Ivd	n/a	115	450	e/p/s	40		Die
Image Lag		Lag	n/a	5		e$^-$			Design
Blooming Suppression		Xab	100						Design
Vertical Smear		Smr	n/a	-85	-75	dB		6	Design
Total Noise		n_{e-T}		10		e$^-$rms		3	Design
Dynamic Range		DR		64		dB		4	Design
Output Amplifier DC Offset		V_{odc}	6.5	7.5	9.3	V			Die
Output Amplifier Bandwidth		F_{-3db}	88	140	176	MHz		5	Die
Output Amplifier Impedance		R_{OUT}	100	160	200	Ohms			Die
Output Amplifier Sensitivity		ΔV/ΔN		32		μV/e$^-$			Design
Peak Quantum Efficiency	Red Green Blue	QE_{max}		32 42 40	n/a n/a n/a	%			Design
Peak Quantum Efficiency Wavelength	Red Green Blue	λQE_{max}		630 550 470	n/a n/a n/a	nm			Design

Notes:

1. Value is over the range of 10% to 90% of photodiode saturation.
2. Value is for the sensor operated without binning.
3. Includes system electronics noise, dark pattern noise and dark current shot noise at 30 MHz.
4. Uses 20LOG(PNe/n_{e-T}).
5. Last stage only, C_{load}=10 pF. Then $f_{-3db} = (1 / (2\pi * R_{out} * C_{load}))$.
6. FB2 Timing Mode (1 x 2 Binning).
7. “Die” indicates a parameter that is measured on every sensor during the production testing. “Design” designates a parameter that is quantified during the design verification activity.

Typical Performance Curves

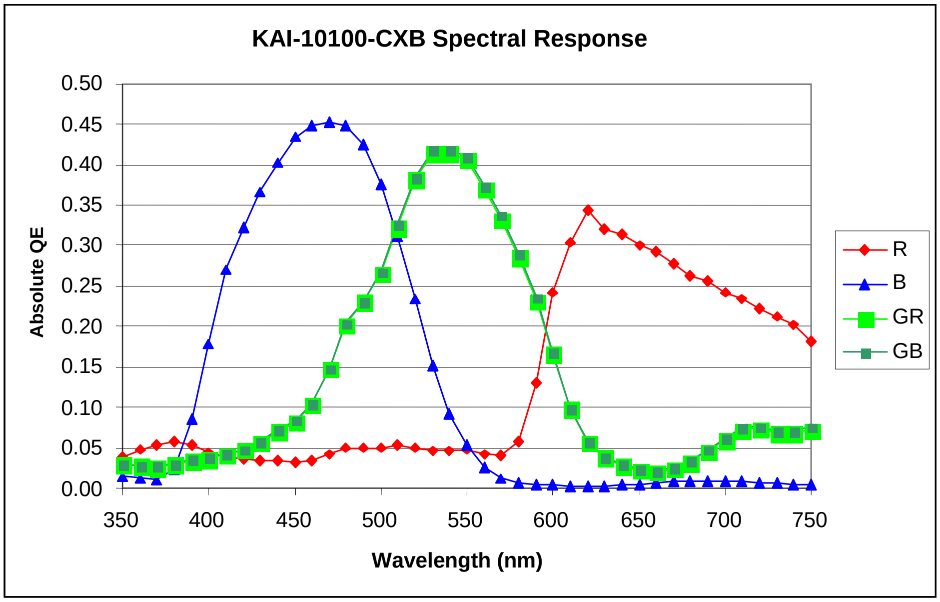


Figure 6: Typical Spectral Response– Clear Cover Glass

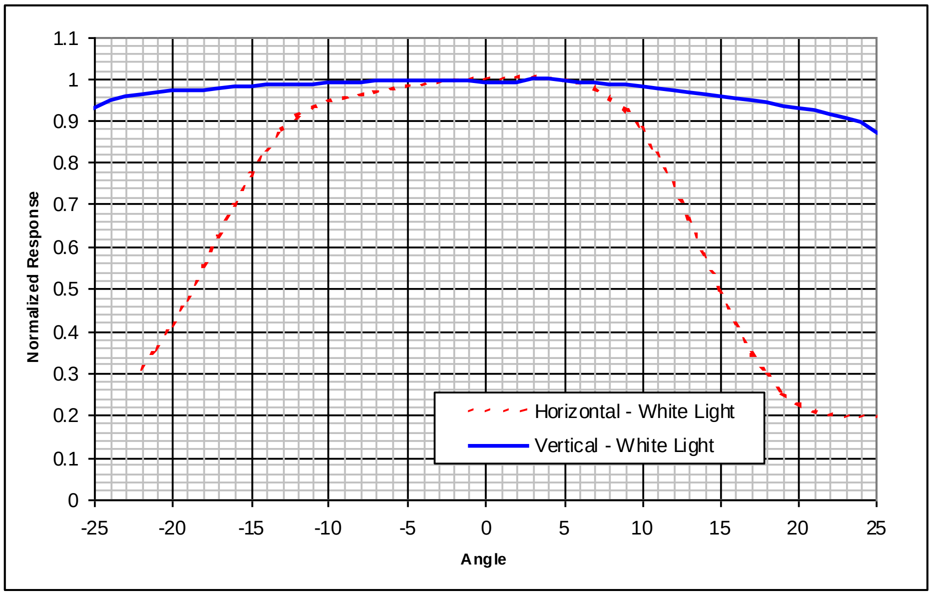


Figure 7: Typical Angular Response – Clear Cover Glass

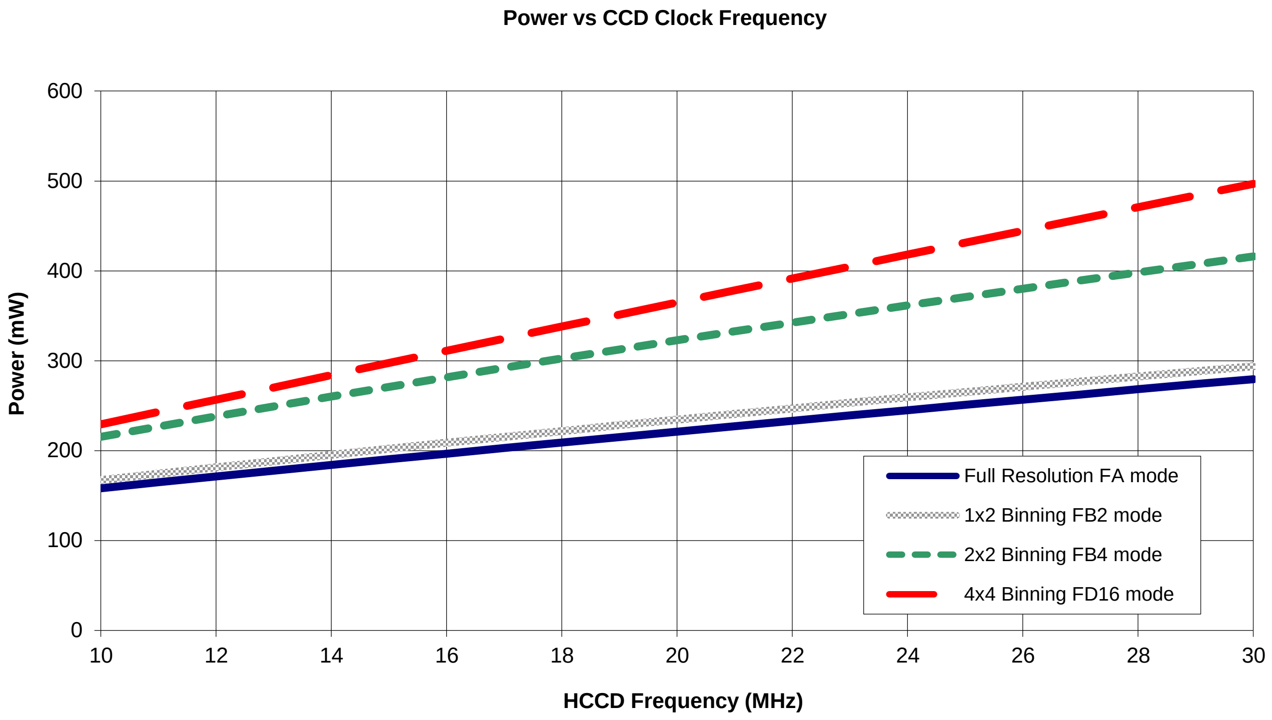


Figure 8: Power vs. Clock Rate

Defect Definitions

OPERATIONAL CONDITIONS

All Defect tests performed using the following conditions:

Description	Condition - Unless otherwise noted	Notes
Temperature	20 °C	
Integration time (tint)	33 msec	
Timing Mode	FA	

SPECIFICATIONS

Description	Definition	Standard Grade	Notes	Sample Plan
Major dark field defective pixel	Defect ≥ 200 mV	2000	1	die
Major bright field defective pixel	Defect ≥ 15 %		1	die
Minor dark field defective pixel	Defect ≥ 30 mV	2000	1	die
Cluster defect	A group of 2 to "N" contiguous major defective pixels	20 N=20	1	die
Column defect	A group of more than 20 contiguous major defective pixels along a single column	40	1	die

Notes:

1. Tested at 20 °C.

Test Definitions

TEST REGIONS OF INTEREST

Active Area ROI:	Pixel (1, 1) to Pixel (3760, 2840)
Center 210 by 210 ROI:	Pixel (1775, 1315) to Pixel (1985, 1525)

Only the active pixels are used for performance and defect tests.

OVERCLOCKING

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 9 for a pictorial representation of the regions.

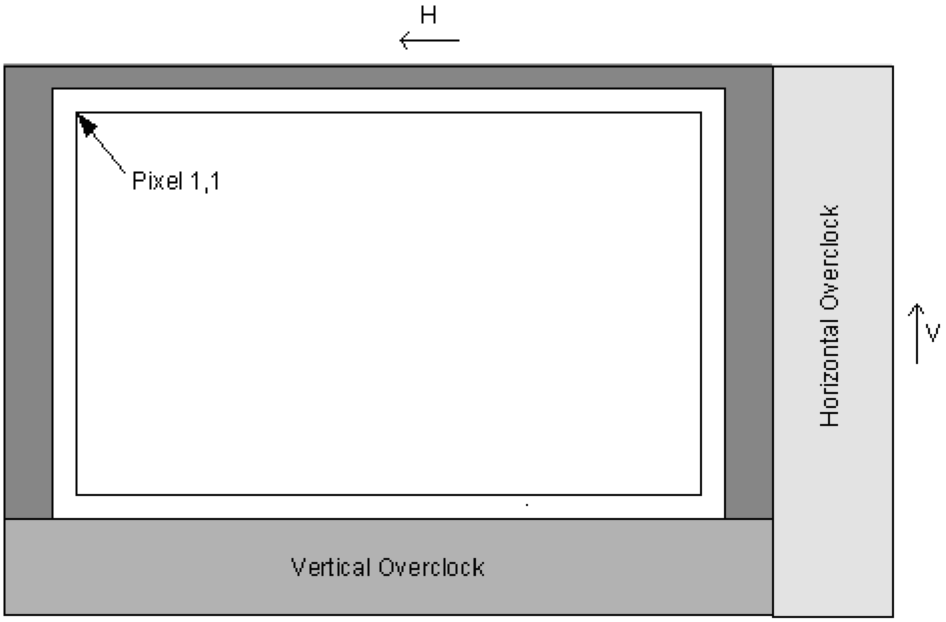


Figure 9: Overclock Regions of Interest

TESTS

Dark field defect test

This test is performed under dark field conditions. The sensor is partitioned into 252 sub regions of interest, each of which is 210 by 210 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the "Defect Definitions" section.

Bright field defect test

This test is performed with the imager illuminated to a level such that the output is at approximately Green: 700 mV (22,000 e^-), Red & Blue: 450 mV (14,000 e^-). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 28,000 electrons (900 mV). The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

Dark defect threshold = 200 mV (major defects); 30 mV (minor defects)

Bright defect threshold = any pixel that deviates more than 15% of average of surrounding pixels in a 210 X 210 ROI

Average Green = 700 mV Upper = 805 mV Lower = 695 mV
Average Red & Blue = 450 mV Upper = 517.5 mV Lower = 382.5 mV

The sensor is then partitioned into 252 sub regions of interest, each of which is 210 by 210 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 700 mV (22,000 electrons).
- Dark defect threshold: 700mV * 15% = 105 mV (Limit 695 mV to 805 mV).
- Bright defect threshold: 200mV * 15% = mV.
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 210, 210.
    - Median of this region of interest is found to be 700 mV.
    - Any pixel in this region of interest that is ≥ (700+105 mV) 805 mV in intensity will be marked defective.
    - Any pixel in this region of interest that is ≤ (700-105 mV) 695 mV in intensity will be marked defective.
- All remaining 251 sub regions of interest are analyzed for defective pixels in the same manner.

Operation

ABSOLUTE MAXIMUM RATINGS

Device Pin	Minimum	Maximum	Units	Notes
VDD, VOUT, SUB15, SUBS, SUBV	-0.4	17.5	V	
V1, V3, V5, V7, V9, V11, V13, V15	VESD -0.4	VESD +24	V	
V2_10, V4_12, V6_14, V8_16	VESD -0.4	VESD +14	V	
H1, H2, H3, H4, H4L, HTG, RG, COG	VESD-0.4	VESD +14	V	
ESD	-10	0	V	
SUB	-0.4	47.4	V	1

Notes:

1. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

POWER-UP SEQUENCE

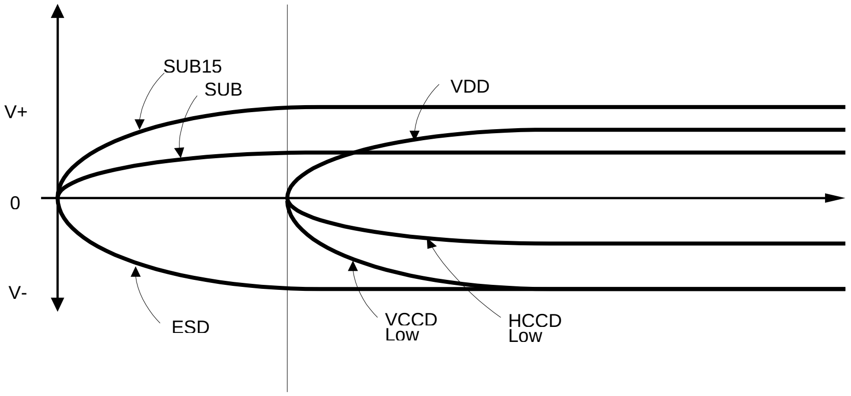


Figure 10: Power-up Sequence Diagram

Power up ESD, SUB, and SUB15 in any order first.

Once the ESD voltage is stable and SUB is above 3 V all other biases can be turned on in any order.

SUBV and SUBS should only drive high impedance circuitry.

The image sensor can be protected from an accidental improper ESD voltage setting by current limiting the SUB voltage to less than 10 mA (that is the 4.7k resistor).

Do not pulse the electronic shutter until ESD is stable.

SUB, SUB15, and VDD must always be greater than GND.

ESD must always be less than GND.

Placing diodes between SUB, SUB15, VDD and ESD pins and GND will protect the sensor from accidental overshoot of VDD, SUB and ESD during power-on or power-off.

The VCCD clock waveform must not have a negative overshoot more than 0.5 V below the ESD voltage.

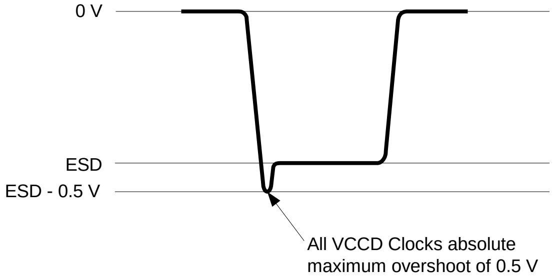


Figure 11: Diagram of vertical clock overshoot to be avoided

ALTERNATE POWER UP SEQUENCE

If VDD is to be powered up at the same time as SUB15 and SUB then VDD must be less than 10 V until SUB is greater than 3 V.

*** VDD cannot be +15 V when SUB is 0V ***

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Amplifier Supply	VDD	14.5	15.0	15.5	V		
Substrate, Supply	SUB15	14.65	15.0	15.35	V		
Substrate, Input	SUB	-0.1	SUBS, SUBV,15V	Nominal + ES	V	<200 mA	4, 5, 7
Output Gate	COG	N/A, not supplied by user					3
Video Output Current	IOUT		-5		mA		1
VnL- VESD difference		-0.2	0	0.2			2, 6
Reset Gate	RG	-0.2	0	0.2			2

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier. See Figure 8.
2. VESD should tie directly to Vertical Low (VL) clock driver bias level.
3. Voltage is set by image sensor and will be between GND and –4 V. Connect to ground via a bypass capacitor with recommended value as shown.
4. Peak AC current will be much higher due to the 4.3nF load of the substrate. Substrate input level (1 of 4) is set to support the timing mode; (FA = SUBS, FBx = SUBV, FD16 = 15V).
5. ES is the electrical shutter voltage. See AC Operating Conditions, clock levels, for the definition.
6. Suffix “n” refers to all Vertical clock pins; V2-10, V4-12, V1, V9, V5, V13, V3, V11, V7, V15, V6-14, V8-16. For any vertical clock, the low level cannot exceed these values.
7. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

SUPPLIED VOLTAGE LEVELS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Substrate, Outputs	SUBV, SUBS	7.45	10.47	13.39	V		1

Note:

1. Voltage level defined by individual device on-chip circuitry.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Notes
Vertical Clock Low Level	VnL	Low	-9.0	-8.75	-8.5	V	1,3
Vertical Clock Mid-Level	VnM	Mid	-0.1	0.0	0.1	V	1,3
Vertical Clock High Level	VnH	High	12.75	13	13.25	V	1,3
Horizontal Clock Low Level	HL	Low	-4.3	-4.1	-3.9	V	1
Horizontal Clock High Level	HH	High	-0.1	0.0	1	V	1
Electronic Shutter PULSE AMPLITUDE	ES		30	32	34	V	1,2,4
RG amplitude	RGA	-	3.1	3.3	4.3	V	
HTG High	HTH	High	3.9	4.1	4.3	V	1
HTG Low	HTL	Low	-4.7	-4.1	-4.3	V	

Notes:

1. All pins draw less than 10mA DC current. Capacitance values relative to SUB (substrate).
2. The electronic shutter level is referenced to SUB (typically).
3. Suffix “n” refers to all Vertical clock pins; V2-10, V4-12, V1, V9, V5, V13, V3, V11, V7, V15, V6-14, V8-16
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Clock Capacitance

Clock	Capacitance	Units
V1	6.5	nF
V3	6.5	nF
V5	6.5	nF
V7	6.5	nF
V9	6.5	nF
V11	6.5	nF
V13	6.5	nF
V15	6.5	nF
V2_V10	13	nF
V4_V12	13	nF
V6_V14	13	nF
V8_V16	13	nF
H1	85	pF
H2	85	pF
H3	85	pF
H4	85	pF
HTG	30	pF
H4L	10	pF
Reset	10	pF
Sub	4.3	nF

Timing

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
HCCD Clock Period	T_H	33	-	-	ns	
HCCD Delay	T_{HD}	-	15.6	-	nS	1
HTG Pulse Time	T_{HTG}	-	8	-	μs	2
VCCD Transfer time	T_{VCCD}	-	2.0	-	μs	3
VCCD Pedestal time	T_{3P}	-	2	-	μs	4
Photodiode Transfer time	T_{V3rd}	5.0	6	-	μs	4
VCCD Delay	T_{3D}	-	4	-	μs	4
Reset Pulse time	T_R	-	2.0	-	ns	
Shutter Pulse time	T_S	-	7	-	μs	5
Shutter Pulse delay	T_{SD}	-	15.6	-		
Vertical Clock Edge Alignment	T_{VE}	0.0	-	100	ns	
Vodd Rise Time	t_{V1r}	0.5	0.75	1.0	us	
Veven Rise Time	t_{V2r}	0.5	0.75	1.0	us	
Vodd Fall Time	t_{V1f}	0.5	0.75	1.0	us	
Veven Fall Time	t_{V2f}	0.5	0.75	1.0	us	
Vodd Pulse Width	t_{V1w}	2.0	-	-	us	
Veven Pulse Width	t_{V2w}	2.0	-	-	us	
H1, H2 Rise Time	t_{H1r}	-	-	4	ns	
H3, H4 Rise Time	t_{H2r}	-	-	4	ns	
H1, H2 Fall Time	t_{H1f}	-	-	4	ns	
H3, H4 Fall Time	t_{H2f}	-	-	4	ns	
H1, H2 Rise Time, FF mode	t_{H1r}	-	-	6	ns	
H3, H4 Rise Time, FF mode	t_{H2r}	-	-	6	ns	
H1, H2 Fall Time, FF mode	t_{H1f}	-	-	6	ns	
H3, H4 Fall Time, FF mode	t_{H2f}	-	-	6	ns	
HTG, H1 alignment Rise Time	$t_{HT,1r}$	0			ns	
HTG, H1 alignment Fall Time	$t_{HT,1f}$	13			ns	
H1, H2 – H3, H4 Pulse Width	t_{H1w}, t_{H3w}		16.5		ns	
H4L Rise Time	t_{H1Lr}			2	ns	
H4L Fall Time	t_{H1Lf}			2	ns	
H4L Pulse Width	t_{H1Lw}		16.5		ns	
RG Rise Time	t_{RGr}	-		2	ns	
RG Fall Time	t_{RGf}	-		2	ns	
RG Pulse Width	t_{RGw}	-	2	-	ns	
ES Pulse Width	t_{ESw}	-		20	ns	

Notes:

1. Last HCLK to HTG rise.
2. See timing sequence VE.
3. VCCD to HCCD transfer pulse, see timing sequence VE, VG, VN.
4. Photodiode to VCCD transfer sequence see sequence VA, VB, VC, VD, VF.
5. Electronic shutter timing see timing sequence VG.

Timing Modes

Timing Mode	Sensor Output			Binning		30 MHz fps	Vertical			Notes
	X	Y	Megapixel	X	Y		Sequences	Pixel	Purpose	
FA	3760	2840	10.68	1	1	4.67	VA, VB, VC, VD, VE	4.75 x 4.75	Full Resolution 4 field Interlaced	1
FB2	3760	1420	5.34	1	2	10.07	VF, VG	4.75 x 9.5	Progressive Scan	2
FB4	1880	1420	2.67	2	2	10.07	VF, VN	9.5 x 9.5	Progressive Scan	2
FD16	940	710	.67	4	4	19.01	VH, VI	19 x 19	Progressive Scan	3

Notes:

1. Substrate input level for FA mode = SUBS. Nominal linear photodiode capacity 22.5 Ke^-.
2. Substrate input level for FBx mode = SUBV. Nominal linear photodiode capacity 20.0 Ke^-.
3. Substrate input level for FD16 mode = 15V. Nominal linear photodiode capacity 10 Ke^-.

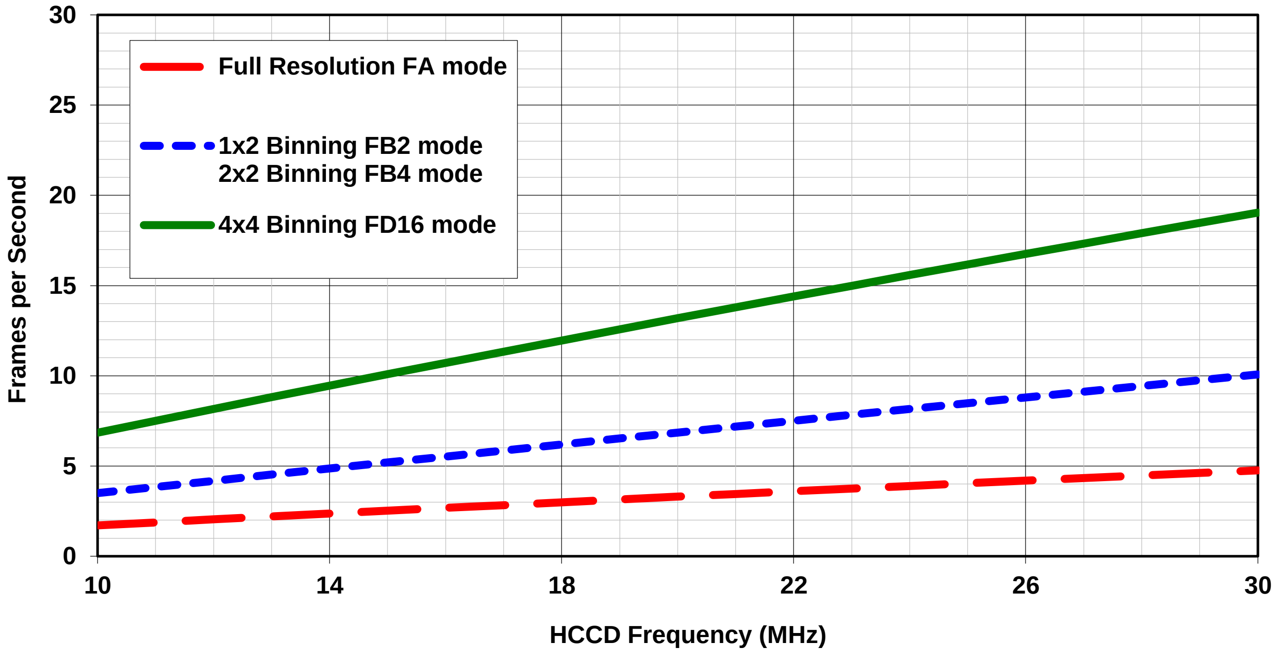


Figure 12: Frame Rates

FULL RESOLUTION INTERLACED READOUT (FA MODE)

Flow Chart FA

This is the 10 Mp full resolution mode. The image is read out four field interlaced.

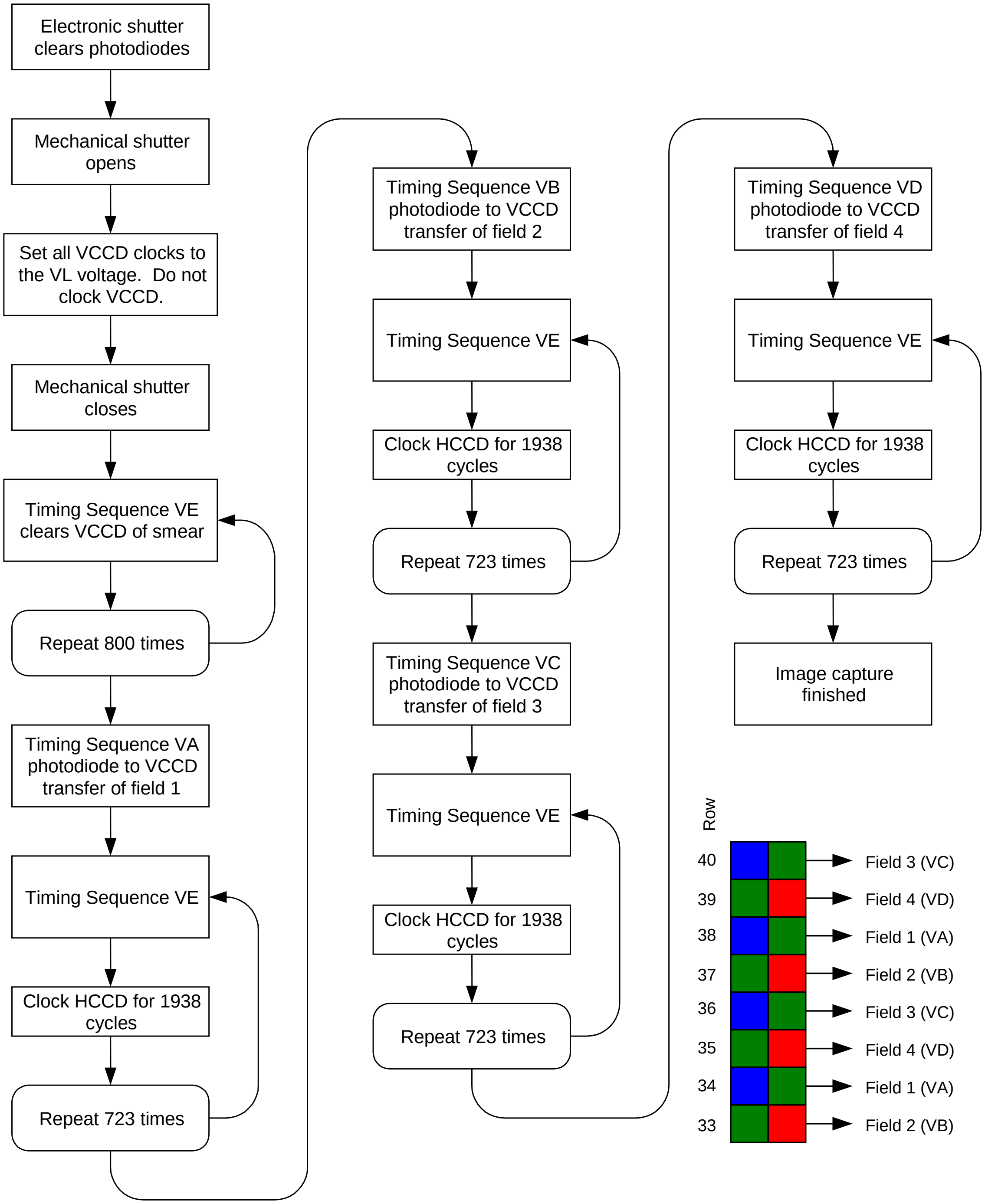


Figure 13: FA Mode -Timing Flow

FA Mode Pixel Order

Field	Rows	Vertical Sequence	HCCD A Color	HCCD B Color
1	2, 6, 10 …	VA	Green	Blue
2	1, 5, 9 …	VB	Red	Green
3	4, 8, 12 …	VC	Green	Blue
4	3, 7, 11 …	VD	Red	Green

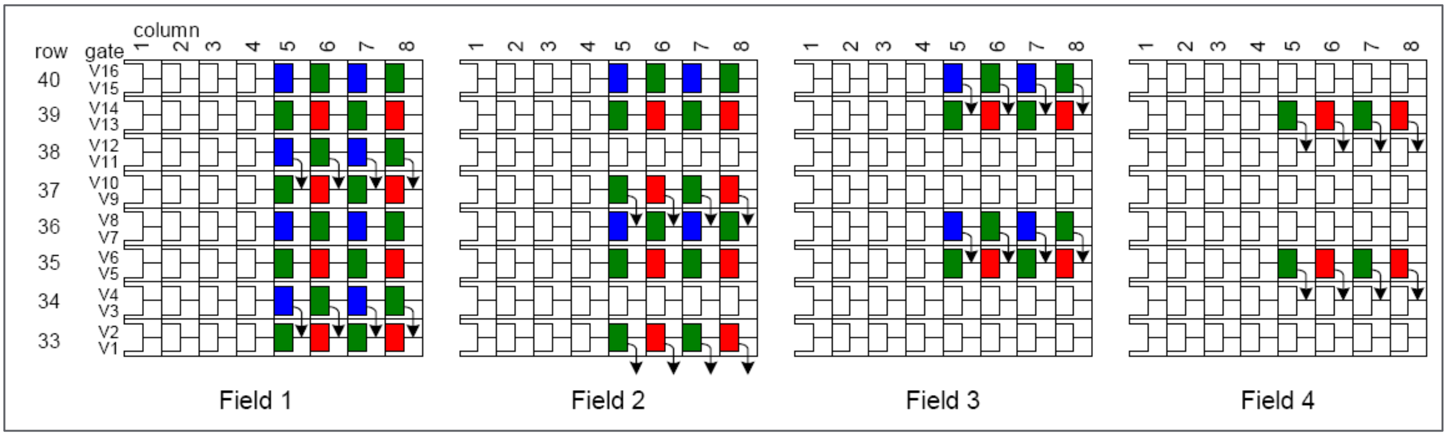


Figure 14: FA Mode –Pixel Order Diagram

FA Frame Rate

$$\frac{10^6}{T_{VA}+T_{VB}+T_{VC}+T_{VD}+T_{MS}+\left(N_F+N_L\right)\left(8T_{VCCD}+\frac{(N_C+2)}{f}\right)}$$

$T_{MS} =$ Total time for mechanical shutter to open and close

$N_F =$ Number of lines to flush VCCD after shutter closes (800)

$N_L =$ Number of lines to read out of the image sensor (2892)

$N_C =$ Number of clock cycles in one line (1938)

$T_{VCCD} =$ VCCD transfer time (1.0 μs)

$f =$ HCCD clock frequency (MHz)

$T_{VA}+T_{VB}+T_{VC}+T_{VD}$ = Total time of sequences VA+VB+VC+VD = 80 μs

FA Clocking Overview

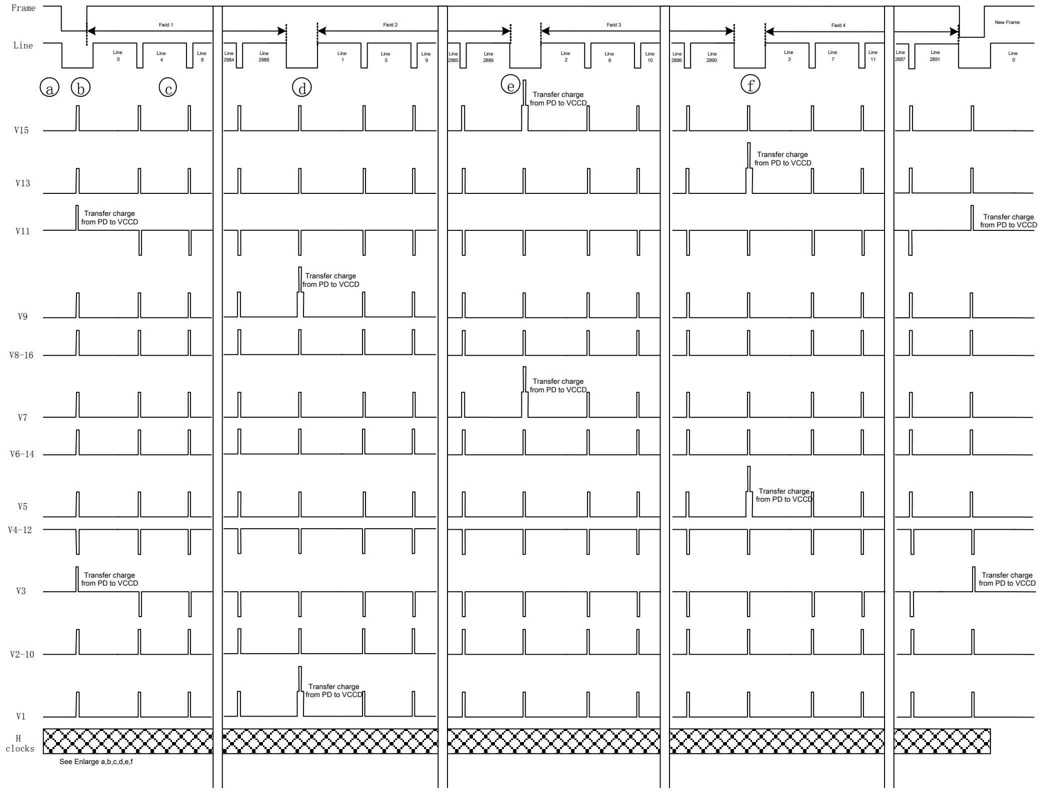


Figure 15: FA Timing Overview

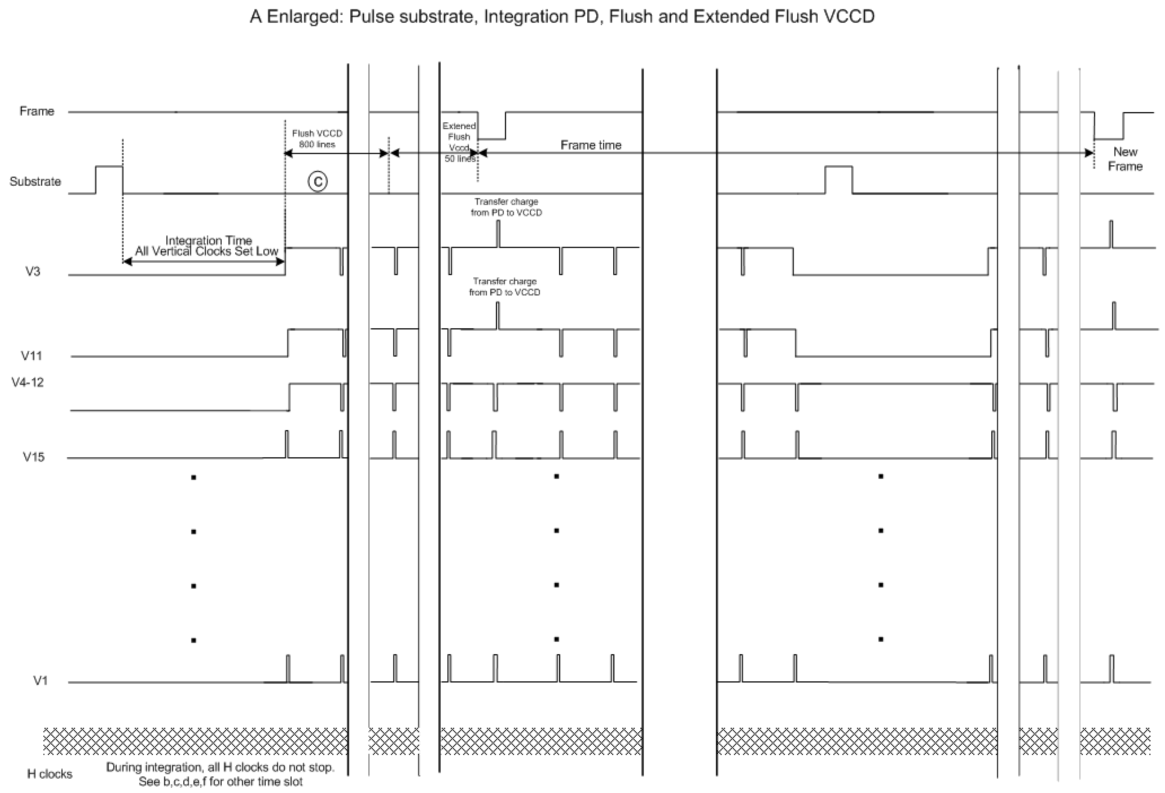


Figure 16: FA Integration Timing Overview

PROGRESSIVE SCAN 1X2 BINNING READOUT (FB2 MODE)

Flow Chart FB2

This is the ½ resolution mode. The image is read out progressive scan. The primary use of this mode is for low light photography at higher frame rate.

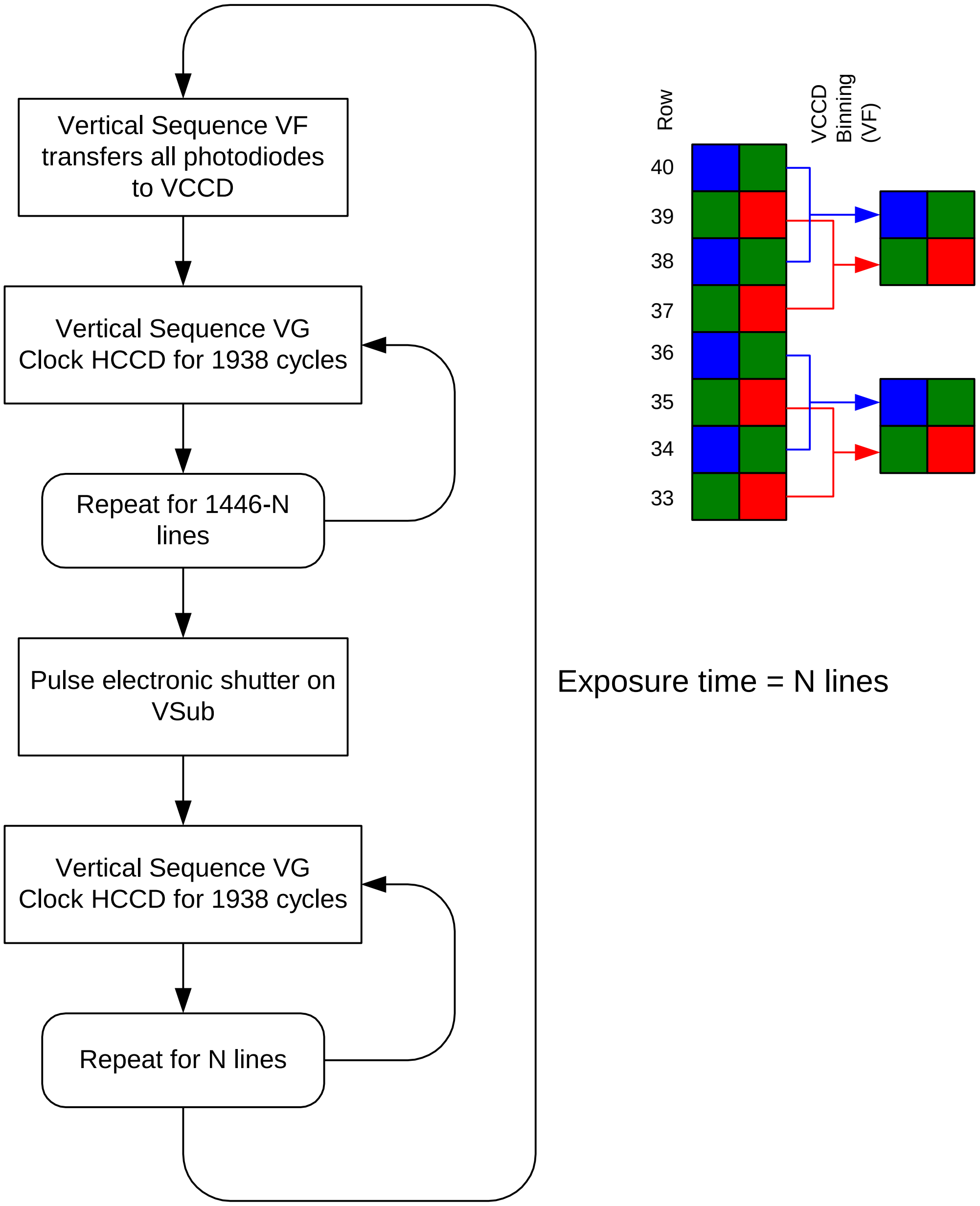


Figure 17: FB2 Mode -Timing Flow

PROGRESSIVE SCAN 2X2 BINNING READOUT (FB4 MODE)

Flow Chart FB4

This is the ¼ resolution mode. Four pixels are summed together. The image is read out progressive scan. Primary use of this mode is for low light photography at higher frame rate.

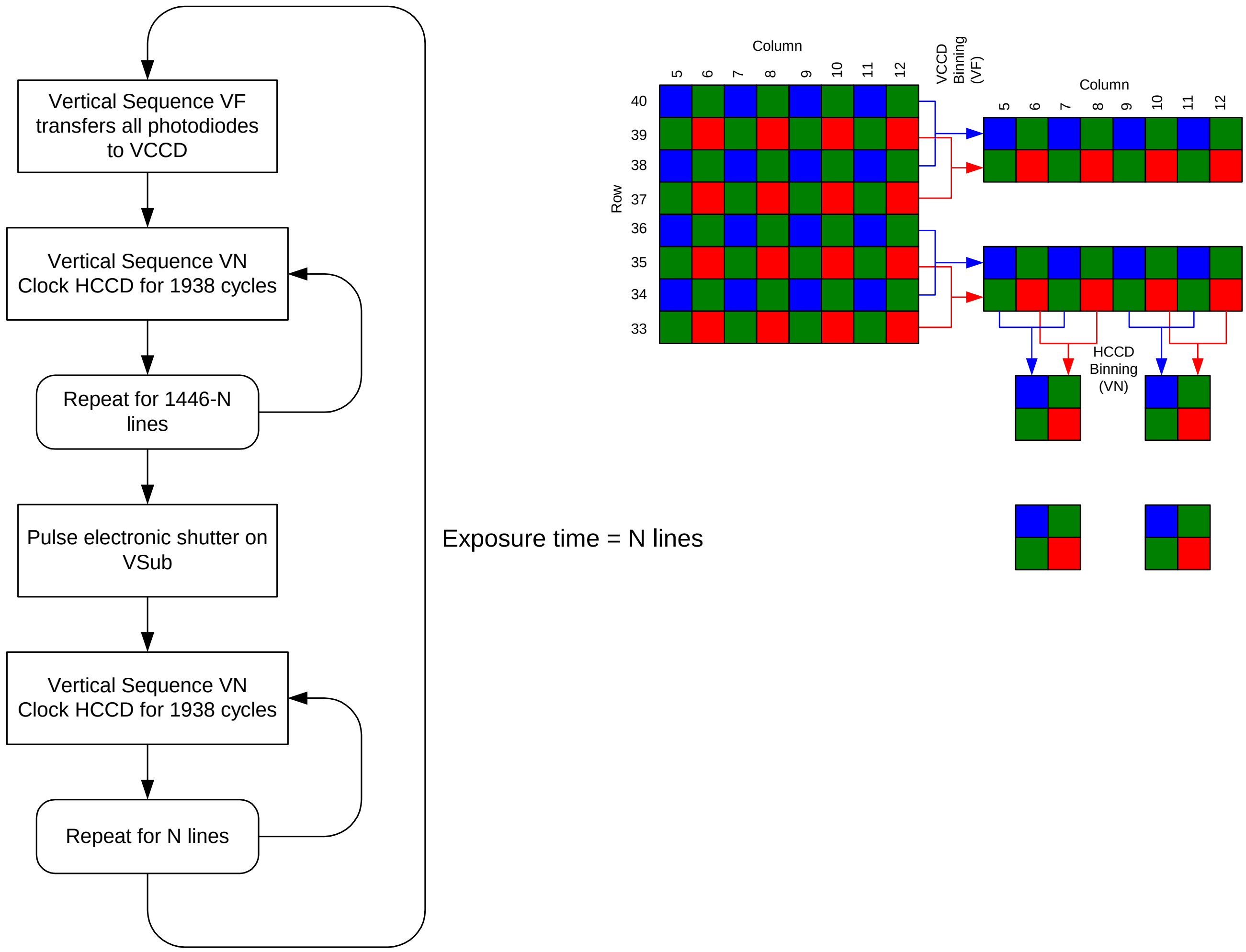


Figure 18: FB4 Mode -Timing Flow

PROGRESSIVE SCAN 4X4 BINNING READOUT (FD16 MODE)

Flow Chart FD16

This is a full image preview mode for low light levels. All pixels are sampled. Four pixels are summed in the VCCD and four pixels are summed on the output amplifier floating diffusion.

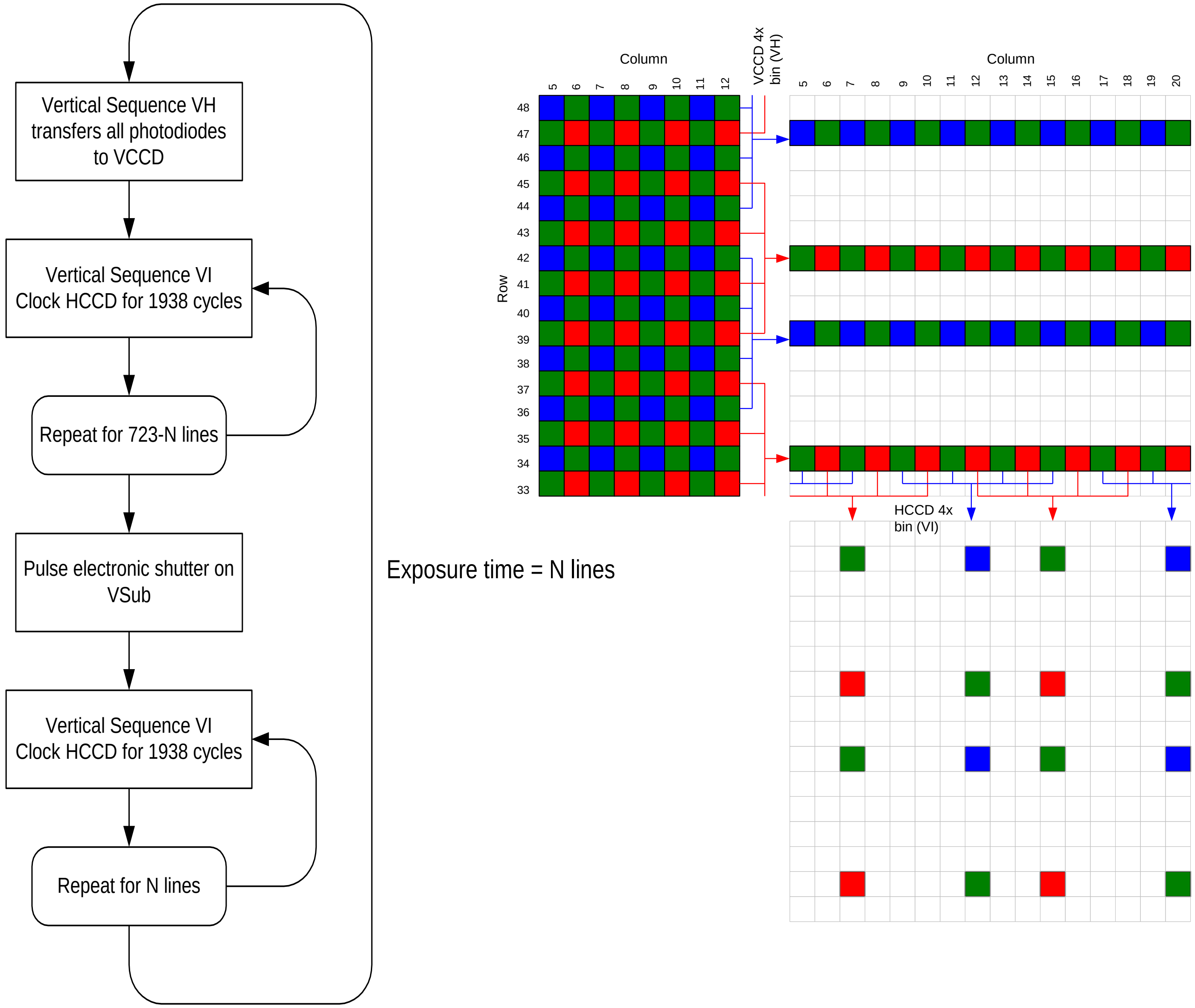


Figure 19: FD16 Mode -Timing Flow

There is a missing clock cycle on H2 of timing sequence VI. This unusual timing at the beginning of each line provides a more evenly spaced Bayer color pattern. With the missing clock cycles output A is the sum of columns 12+14+16+18 and output B is the sum of columns 9+11+13+15. If there were no missing clock cycle then output A would be the sum of columns 10+12+14+16 and output B would be the sum of columns 9+11+13+15.

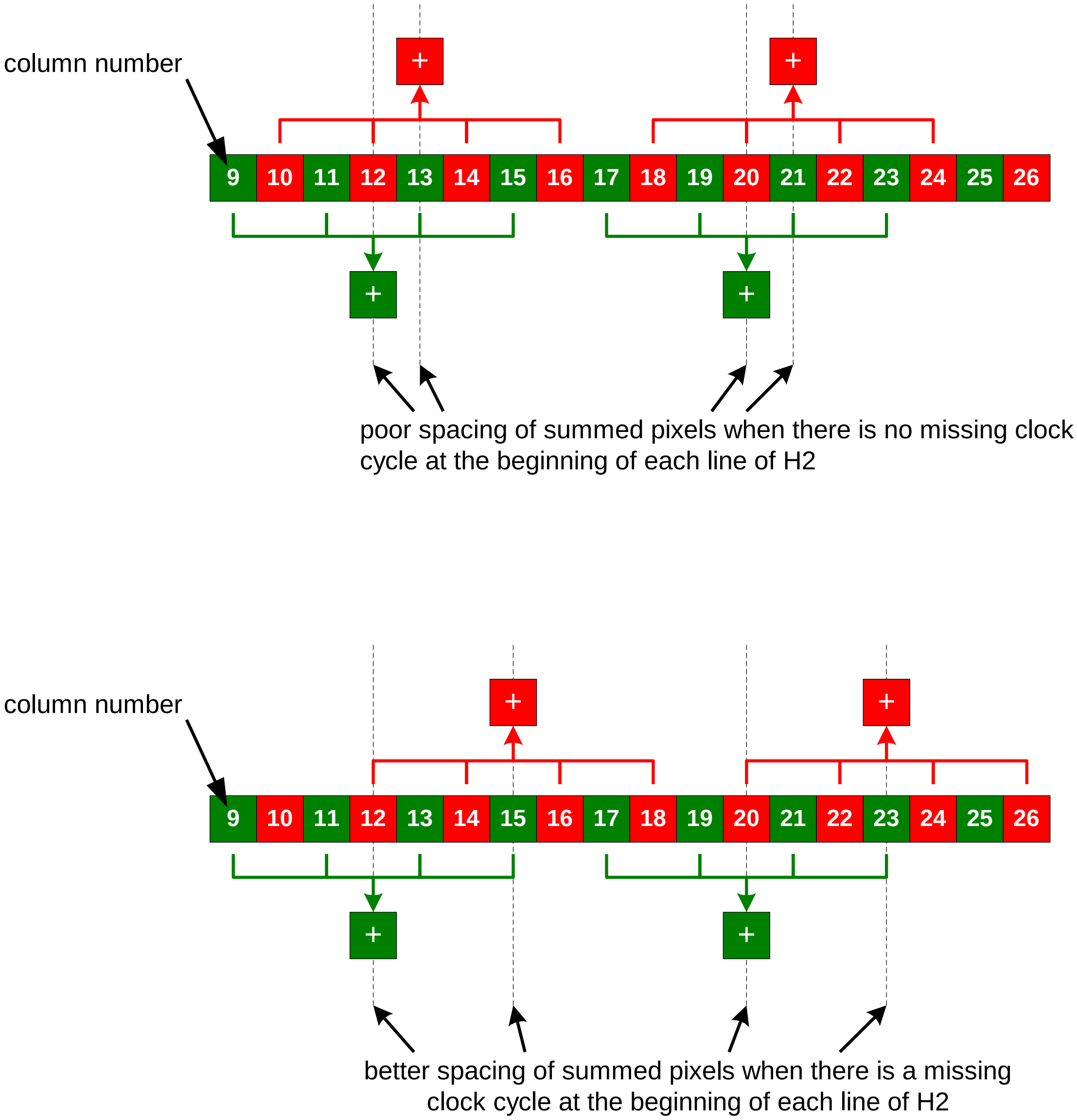


Figure 20: FD16 Mode – Clock Order Information

Vertical Timing Sequence

FA MODE

Sequence VA

Transfers Field 1 from the photodiodes to VCCD. This is for full resolution readout. No VCCD binning. 8 phase VCCD.

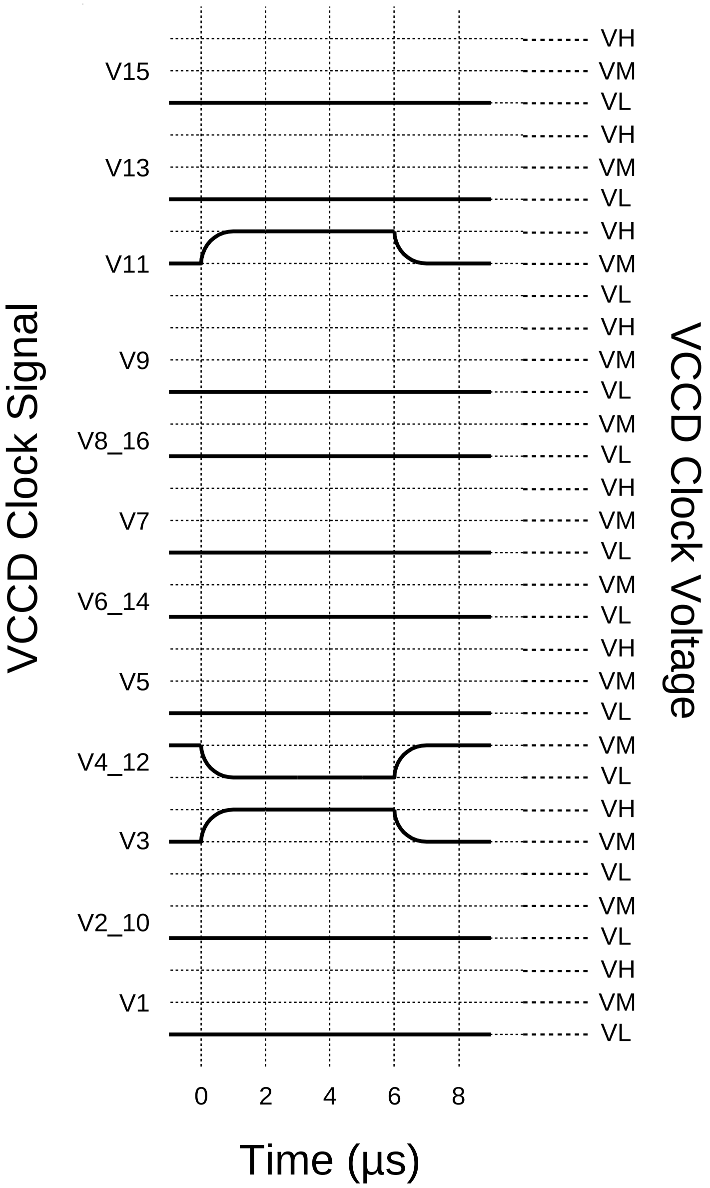


Figure 21: FA Mode –Vertical Timing Sequence - VA

Sequence VB

Transfers Field 2 from the photodiodes to VCCD. This is for full resolution readout. No VCCD binning. 8-phase VCCD.

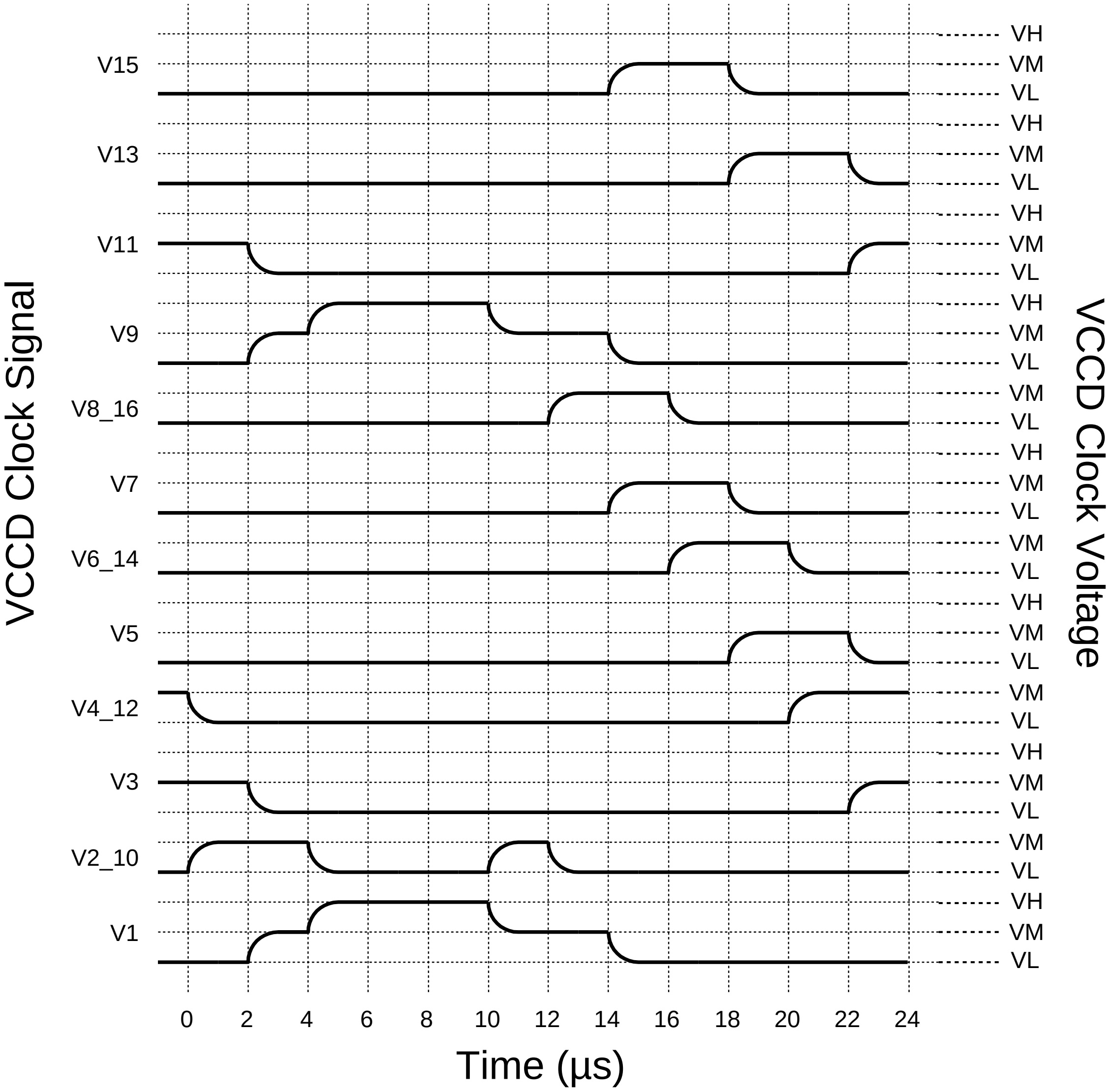


Figure 22: FA Mode –Vertical Timing Sequence - VB

Sequence VC

Transfers Field 3 from the photodiodes to VCCD. This is for full resolution readout. No VCCD binning. 8-phase VCCD.

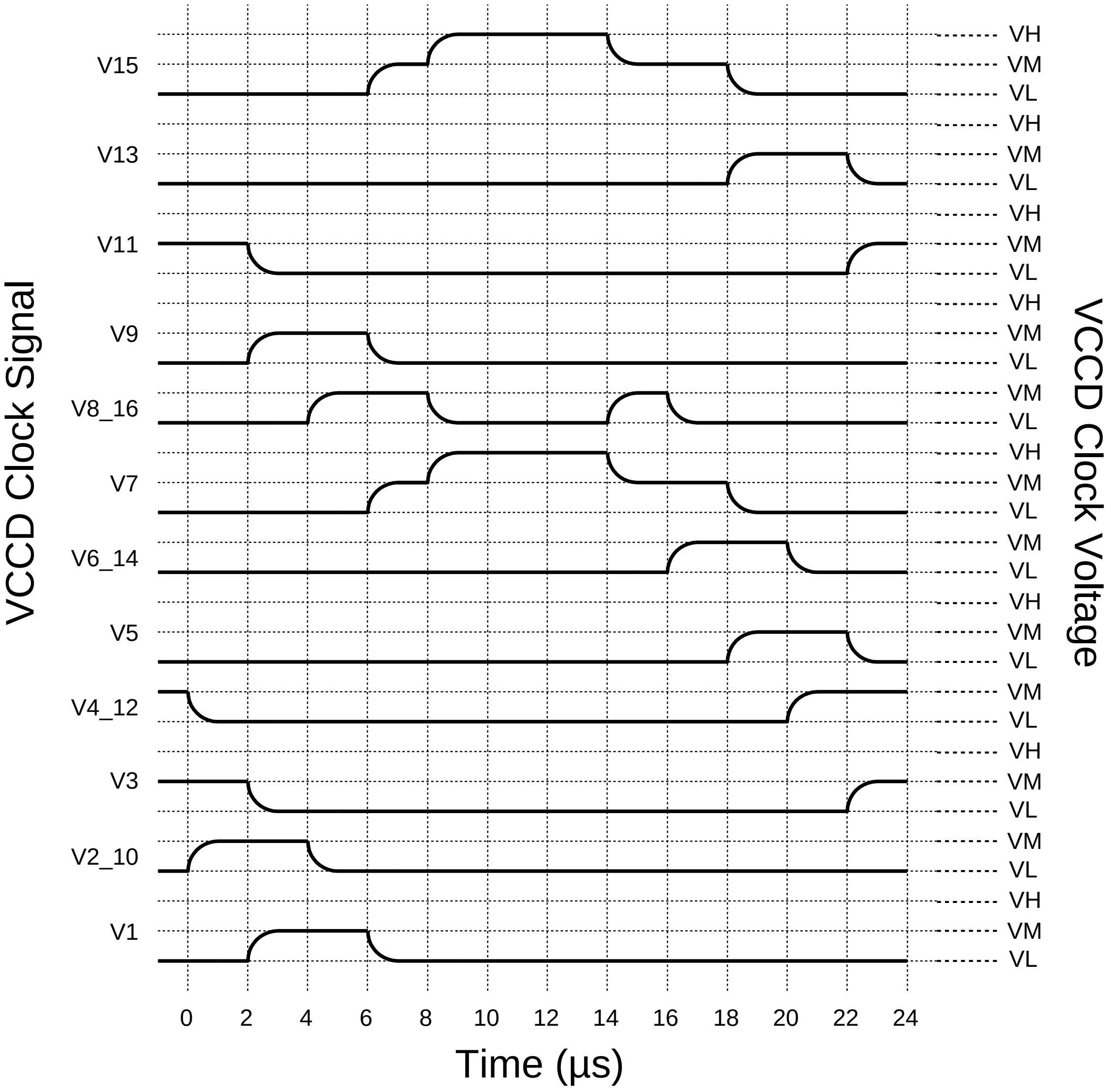


Figure 23: FA Mode –Vertical Timing Sequence - VC

Sequence VD

Transfers Field 4 from the photodiodes to VCCD. This is for full resolution readout. No VCCD binning. 8-phase VCCD.

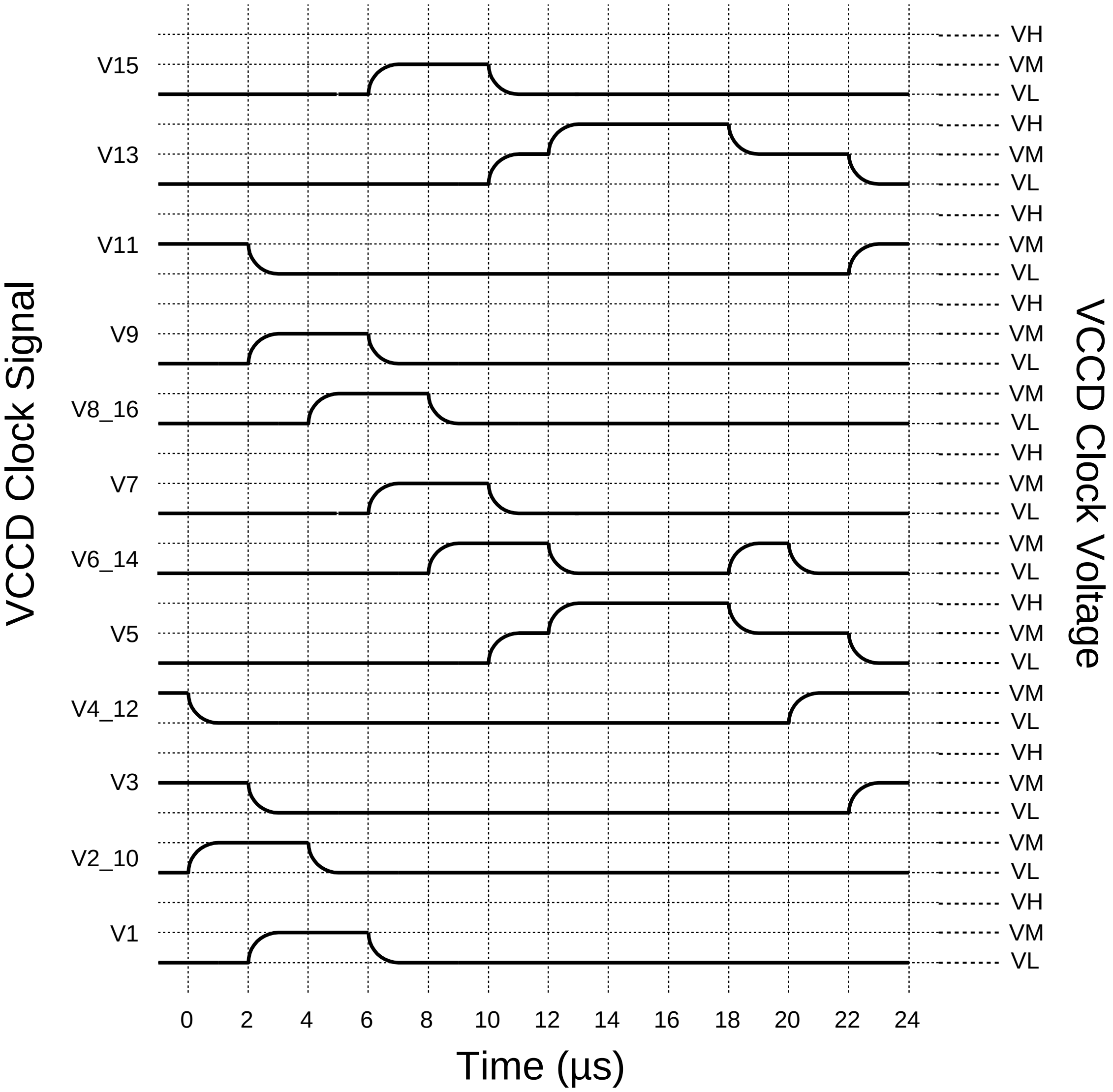


Figure 24: FA Mode –Vertical Timing Sequence - VD

Sequence VE

Transfers one row from the VCCD into the HCCD. This is for full horizontal resolution readout. No HCCD binning. 8-phase VCCD.

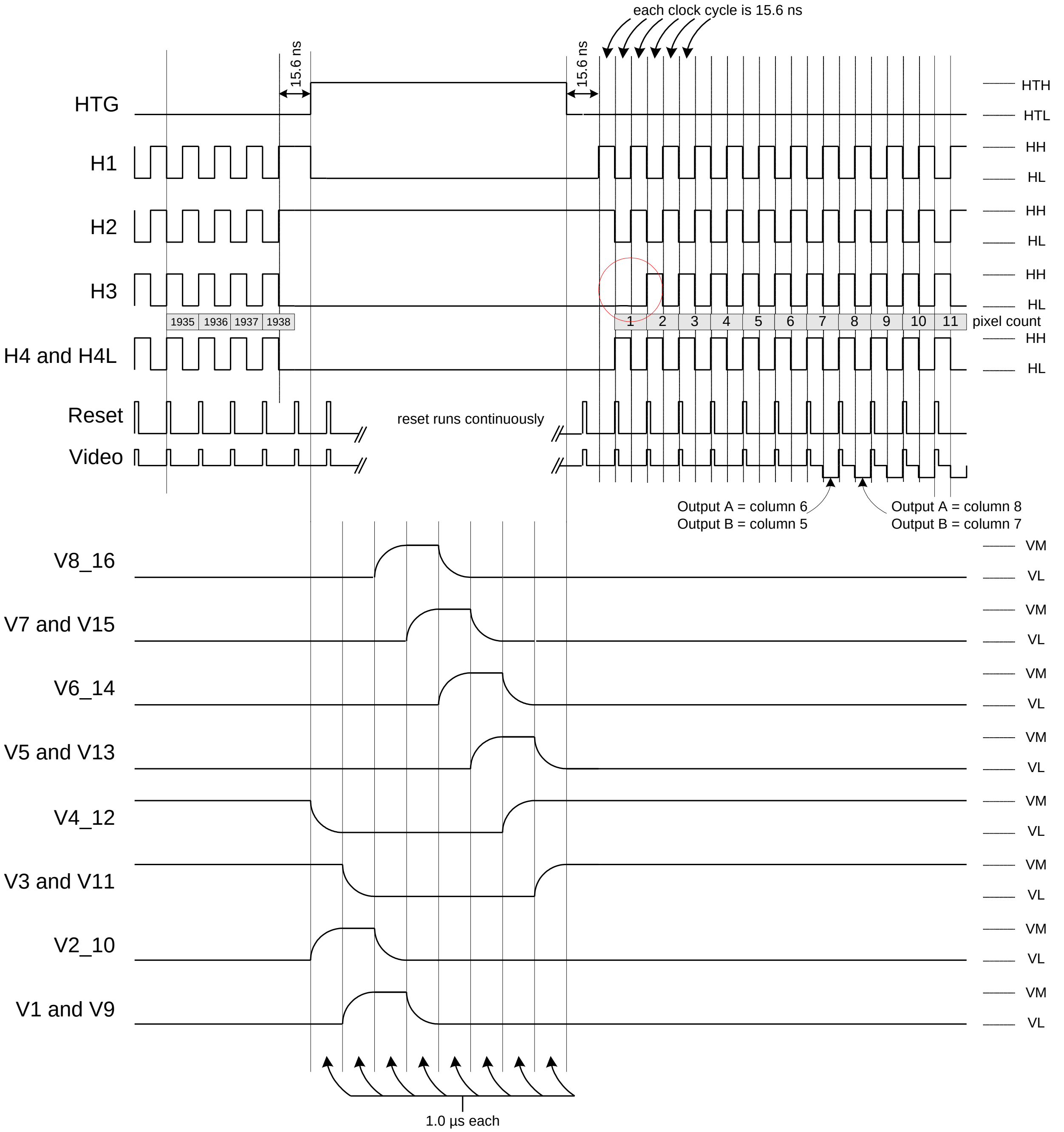


Figure 25: FA Mode –Vertical Timing Sequence - VE

FB2 AND FB4 MODE

Sequence VF

This sums together two rows in the VCCD. Progressive scan readout. Vertical resolution is reduced by a factor of 2. 4-phase VCCD.

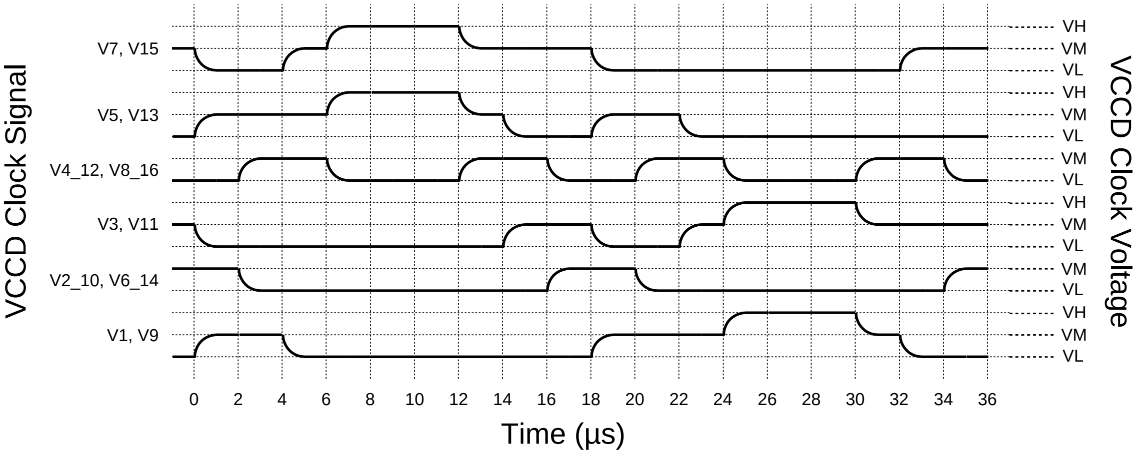


Figure 26: FB2/FB4 Mode –Vertical Timing Sequence - VF

Sequence VG

This transfers one row from the VCCD to the HCCD. There is no horizontal binning. 4-phase VCCD.

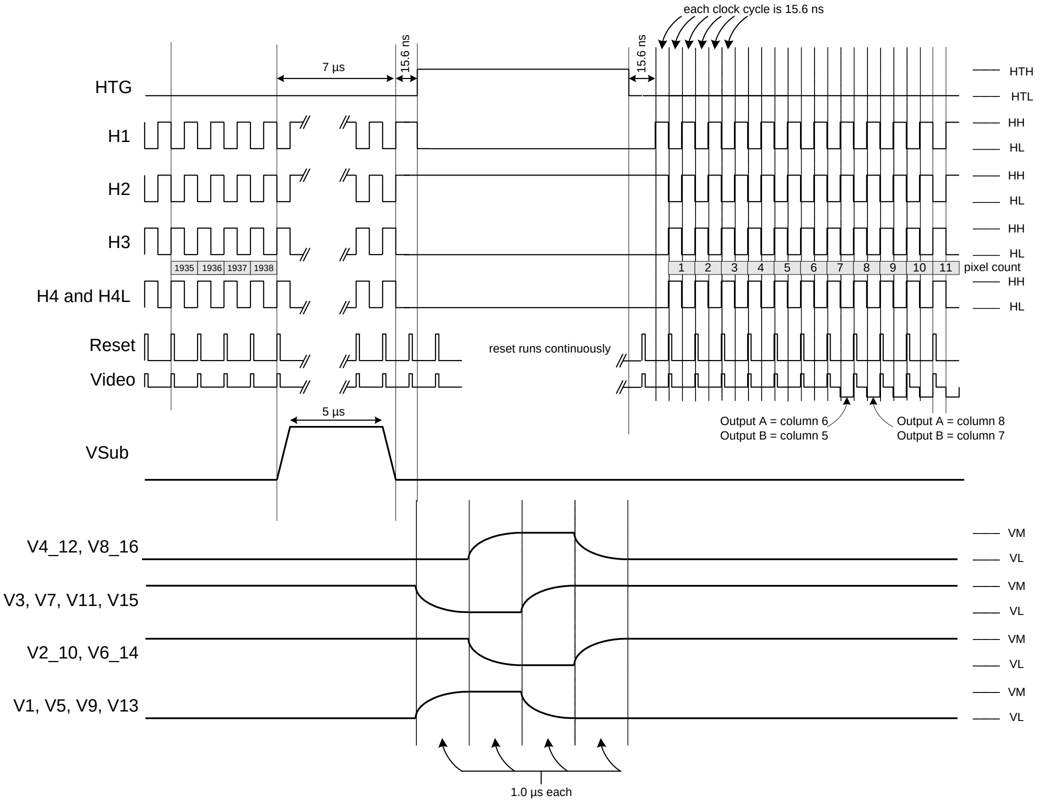


Figure 27: FB2/FB4 Mode –Vertical Timing Sequence - VG

Sequence VN

Transfers one row from the VCCD to the HCCD. Two charge packets are summed together on the amplifier floating diffusion. 4-phase VCCD.

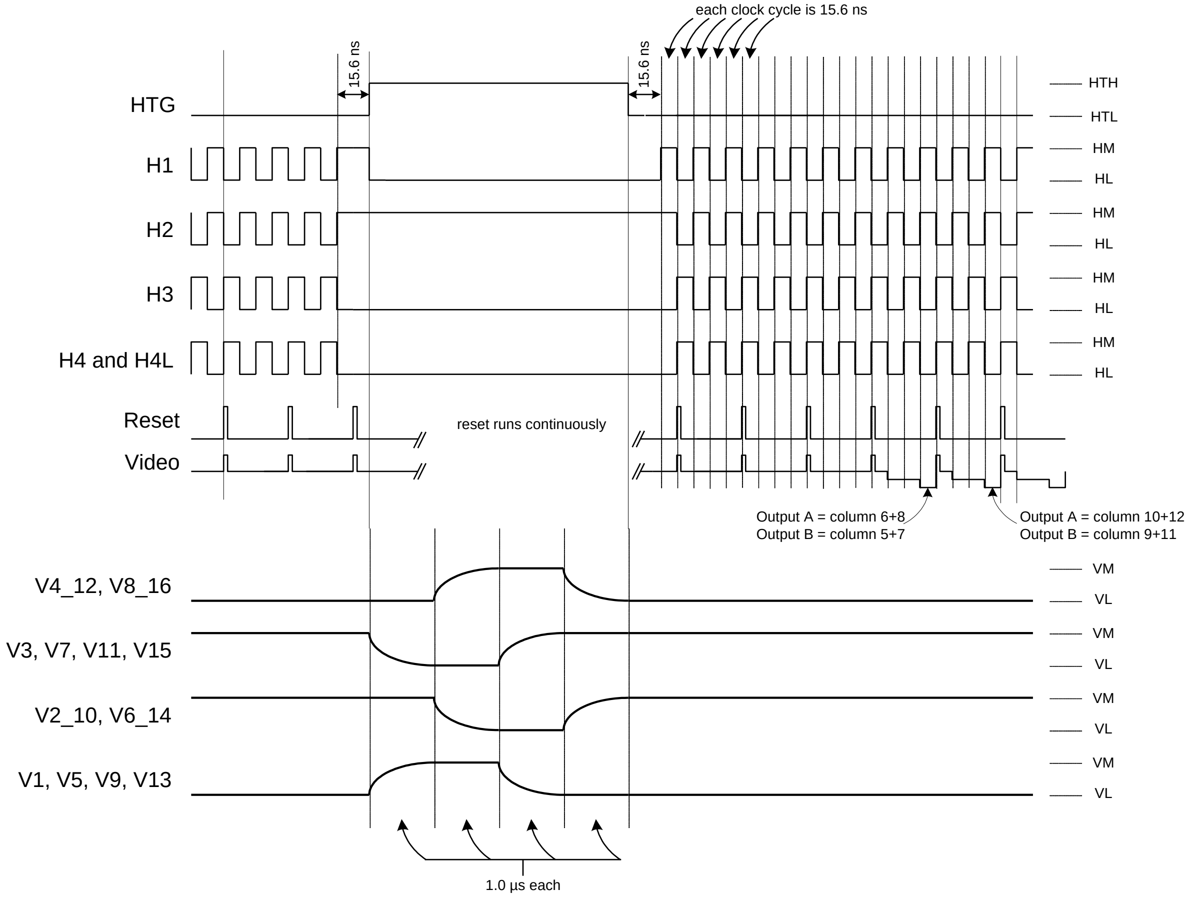


Figure 28: FB2/FB4 Mode –Vertical Timing Sequence - VN

FD16 MODE

Sequence VH

This sums together 4 rows in the VCCD. Progressive scan readout. Vertical resolution is reduced by a factor of 4. 8-phase VCCD.

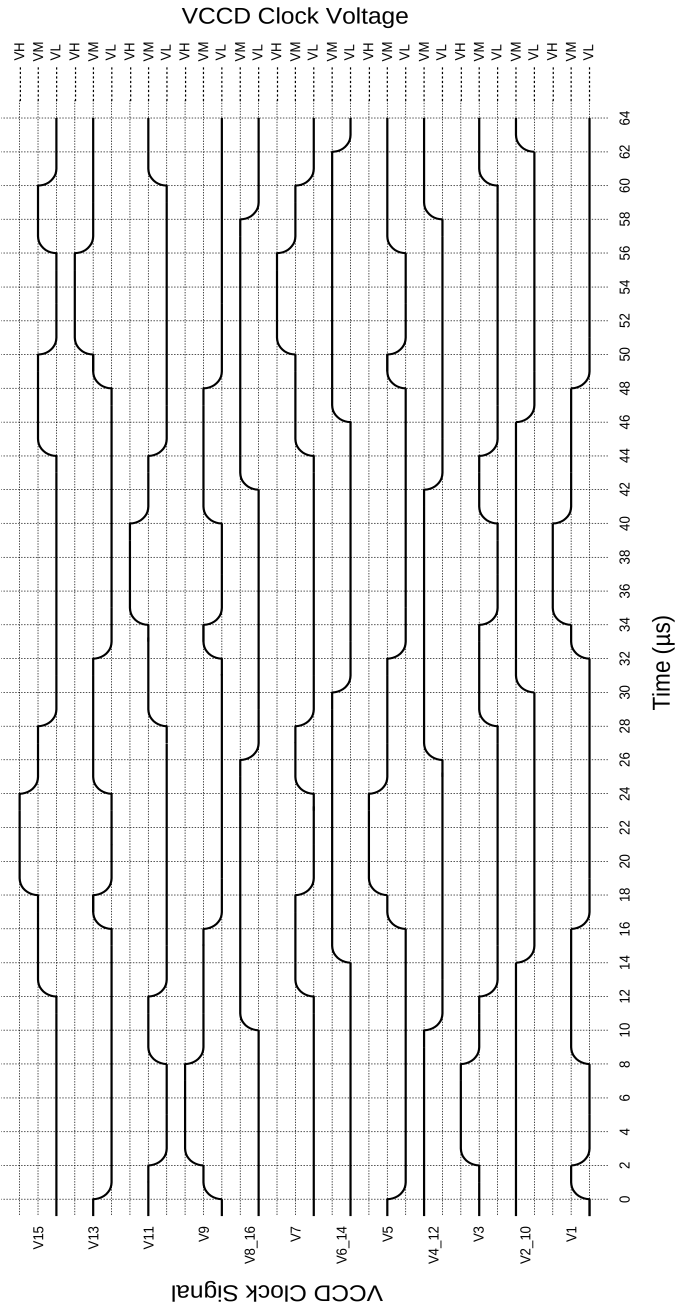


Figure 29: FD16 Mode –Vertical Timing Sequence - VH

Sequence VI

Transfers one row from the VCCD to the HCCD. Sums together 4 charge packets on the amplifier floating diffusion. 8-phase VCCD.

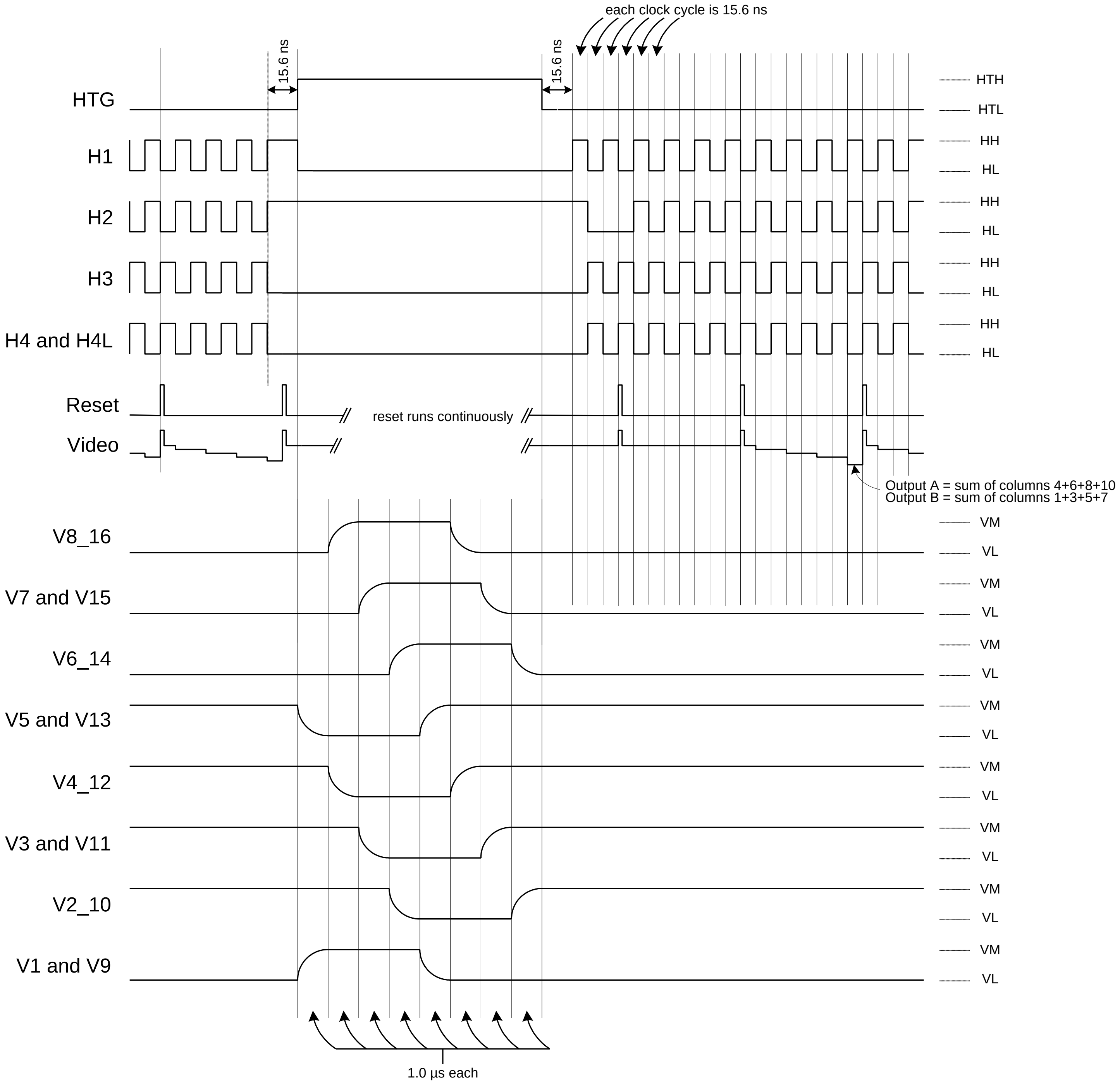


Figure 30: FD16 Mode –Vertical Timing Sequence - VI

ELECTRONIC SHUTTERING

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is at VSUBS volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above VSUBS volts decreases the charge capacity of the photodiodes until 30 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 30 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is VSUBS volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to VSUBS volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-10100 VCCD has a nominal linear charge capacity of 50,000 electrons (50.0 ke$^-$). If the SUB voltage is set such that the photodiode holds more than 50 ke$^-$, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

The amount of antiblooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The Kai-10100 has internal circuitry that will output the optimal setting of VSUB for FA and FBx modes. This voltage should be buffered and fed back to the VSUB of the device. For FD mode the VSUB should be set to 15 V.

The electronic shutter provides a method of precisely controlling the image exposure time in FB2, FB4 and FD16 modes without any mechanical components. If an integration time of TINT is desired, then the substrate voltage of the sensor is pulsed to at least 30 volts TINT seconds before the photodiode to VCCD transfer pulse on Vx. The electronic shutter pulse on VSUB can only be pulsed when the HCCD does not contain valid image charge. The shutter pulse will empty the HCCD of charge. The best place for the electronic shutter pulse is at the end of a line when the HCCD is empty and before the VCCD transfers another line into the HCCD.

Ideally, the electronic shutter pulse would occur once for each image read out. Only one line of the image would be extended by 0.7 μs to insert the electronic shutter pulse. This minimizes the power requirements and time to read out an image.

Storage and Handling

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	80	°C	1
Humidity	RH	5	90	%	2

Notes:

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices.*

ENVIRONMENTAL EXPOSURE

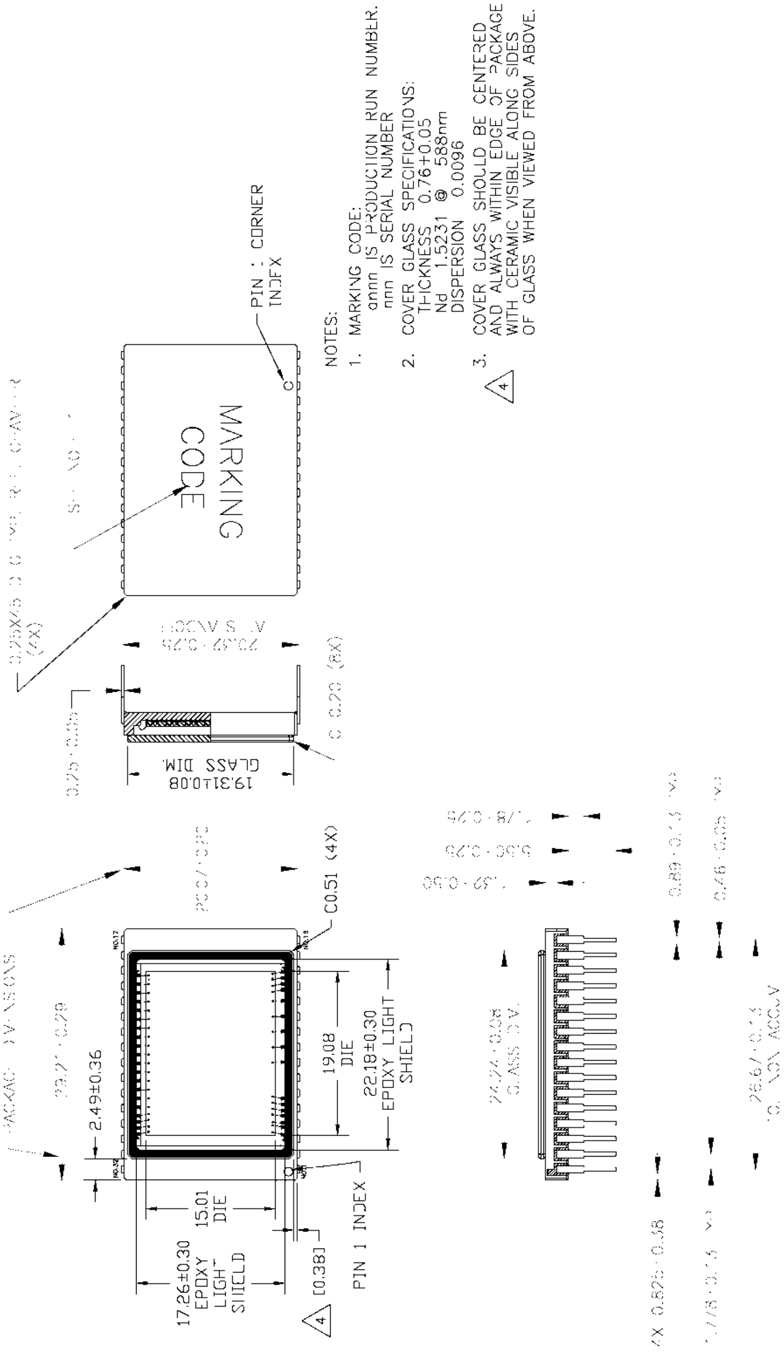
1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discoloured. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions.*
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

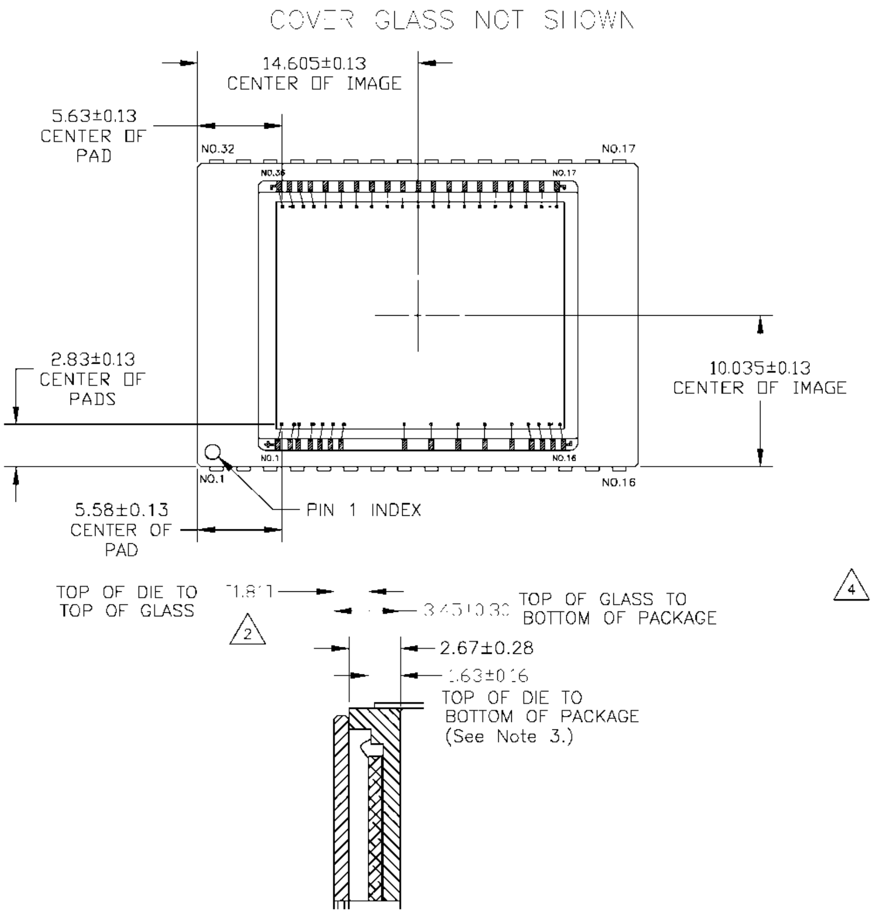
Mechanical Drawings

COMPLETED ASSEMBLY



NOTES:
1. MARKING CODE:
annn IS PRODUCTION RUN NUMBER.
nnn IS SERIAL NUMBER
2. COVER GLASS SPECIFICATIONS:
THICKNESS 0.76+0.05
Nd 1.5231 @ 588nm
DISPERSION 0.0096
3. COVER GLASS SHOULD BE CENTERED AND ALWAYS WITHIN EDGE OF PACKAGE WITH CERAMIC VISIBLE ALONG SIDES OF GLASS WHEN VIEWED FROM ABOVE.

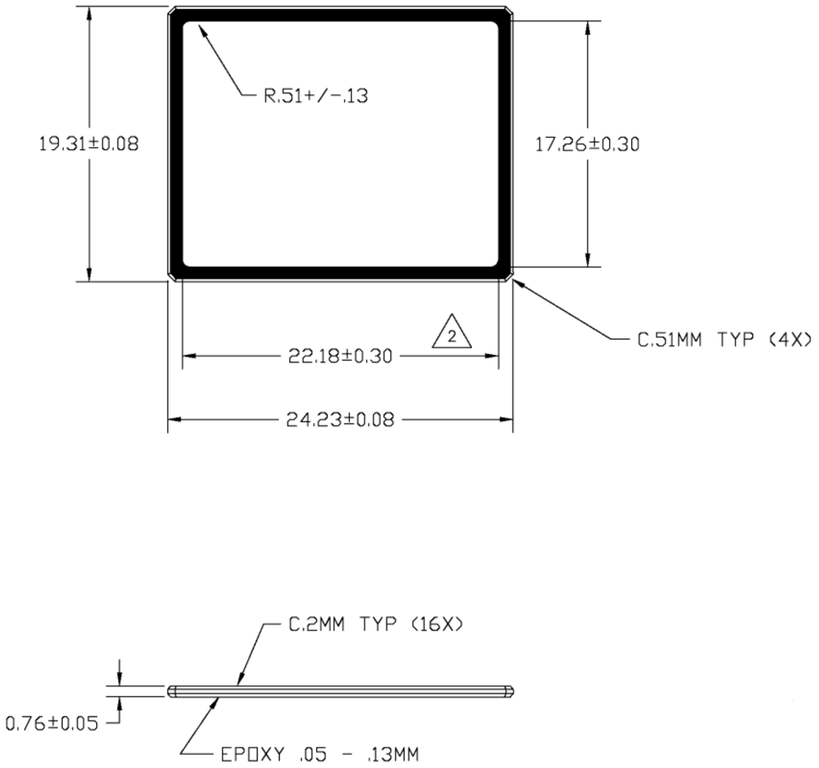
Figure 31: Completed Assembly (1 of 2)



NOTES:
1. CENTER OF IMAGE AREA IS OFFSET FROM CENTER OF PACKAGE BY (0.00,0.00) MM NOMINAL.
2. ANGULAR SPECIFICATION: DIE TO PACKAGE < 1DEGREE.
3. MAXIMUM DIE TILT WITH RESPECT TO BOTTOM OF PACKAGE IS 25 UM.
4. WIRE LOOP HEIGHT: 0.010" +/-0.004" FROM TOP OF DIE TO TOP OF LOOP.

Figure 32: Completed Assembly (2 of 2)

COVER GLASS



NOTES:
1. MATERIAL: SCHOTT D-263T eco OR EQUIVALENT.
2. EPOXY : NCO-150HB
3. DUST, SCRATCH, DIG, INCLUSION SPEC: : 10 MICRON MAX.

Figure 33: Glass Drawing

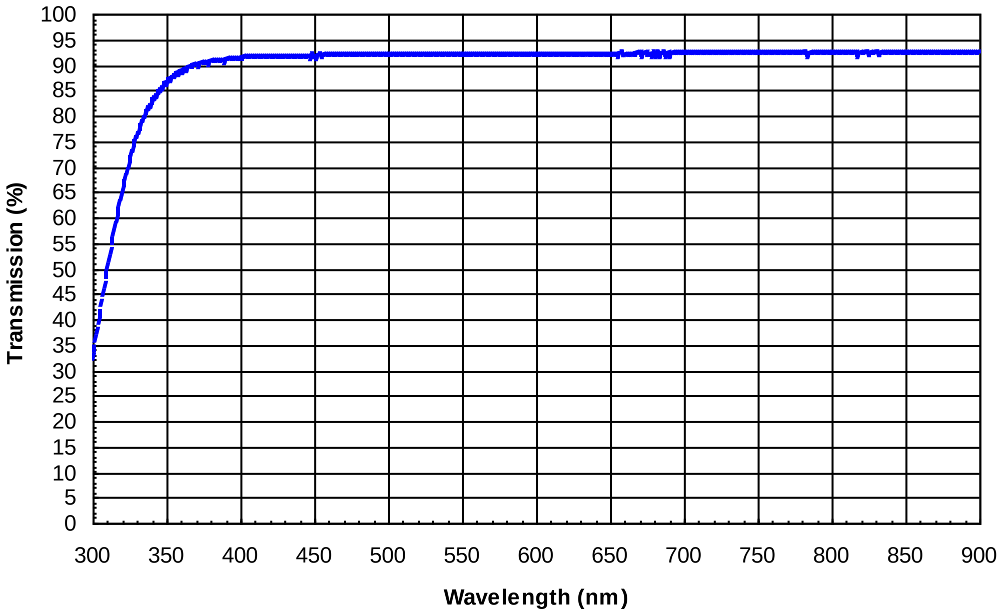


Figure 34: Glass Transmission

Quality Assurance and Reliability

QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-1029

Revision Number	Description of Changes
1.0	• Initial Release.
2.0	• Added catalog numbers 4H2106 and 4H2107
3.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections ○ Absolute Maximum Ratings ○ DC Bias Operating Conditions ○ AC Operating Conditions ○ Storage and Handling • Changed cover glass material to D263T eco or equivalent

PS-0027

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
1.1	• Updated branding

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