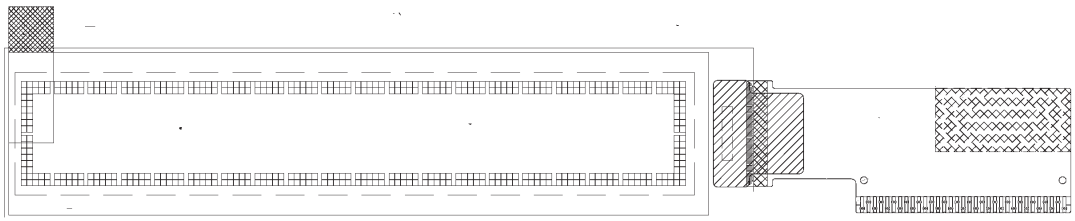
HANTRONIX

PRODUCT SPECIFICATION

HDR202-1

20 CHARACTERS , 2 LINES
OLED DISPLAY MODULE (WHITE)



HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	Q.A.: Z.W.	REV.: 1.0	HDR202-1	SHEET 1 OF 35 DATE: 7/3/14

FEATURES

- Small molecular organic light emitting diode.
- Color : White.
- Panel matrix : 20x2 character.
- Driver IC : SSD1311
- Extremely thin thickness for best mechanism design : 2.027mm.
- High contrast : 2000:1.
- Wide viewing angle : 160°.
- Interface : 8-bit 6800/8080-series parallel interface, Serial Peripheral Interface, I^2C Interface.
- Wide range of operating temperature : -40 to 70 ℃
- Anti-glare polarizer.

MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Number of Characters	20 Character (5x8) (W) x 2 (H)	
2	Dot Size	0.62 (W) x 0.67 (H)	mm^2
3	Dot Pitch	0.65 (W) x 0.7 (H)	mm^2
4	Character Size	3.22 (W) x 5.57 (H)	mm^2
5	Character Pitch	3.7 (W) x 5.95 (H)	mm^2
6	Active Area	73.52 (W) x 11.52 (H)	mm^2
7	Panel Size	83 (W) x 19 (H)	mm^2
8*	Panel Thickness	1.82 ± 0.1	mm
9	Module Size	118.1 (W) x 19 (H) x 2.027 (D)	mm^3
10	Diagonal A/A size	2.93	inch
11	Module Weight	6.77 ± 10%	gram

* Panel thickness includes 0.7mm substrate glass, 1.1mm cover glass and UV glue thickness.

MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DDIO})	-0.3	6	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	10	16	V	Ta = 25℃	IC maximum rating
Supply Voltage (V_{DD})	-0.3	V_{DDIO}	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity	-	85	%		
Life Time	38,000	-	Hrs	140 cd/m², 50% checkerboard	Note (1)
Life Time	45,000	-	Hrs	120 cd/m², 50% checkerboard	Note (2)
Life Time	54,000	-	Hrs	100 cd/m², 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 12V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 140 cd/m^2 :

- Contrast setting : 0x92
- Frame rate : 105Hz
- Duty setting : 1/16

(2) Setting of 120 cd/m^2 :

- Contrast setting : 0x7c
- Frame rate : 105Hz
- Duty setting : 1/16

(3) Setting of 100 cd/m^2 :

- Contrast setting : 0x65
- Frame rate : 105Hz
- Duty setting : 1/16

ELECTRICAL CHARACTERISTICS

D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)		11.5	12	12.5	V
V_{DDIO}	Low voltage power supply,power supply for I/O pins	Low Voltage I/O Application	2.4	-	3.6	V
		5V I/O Application	4.4	-	5.5	V
V_{DD}	Logic Supply Voltage	Low Voltage I/O Application	2.4	-	V_{DDIO}	V
		5V I/O Application (VDD as output)	-	-	-	V
I_{DD}	V_{DD} Supply Current V_{DDIO} = V_{DD} = 3.3V (Low Voltage I/O Application), V_{CC} = 12V, Contrast = FFh, IREF = 15uA , No panel attached, Display ON, All ON		-	90	110	uA
I_{DDIO}	V_{DDIO} Supply Current V_{CC} = 12V, Contrast = FFh,IREF = 15uA , No panel attached, Display ON, All ON	V_{DDIO} = V_{DD} = 3.3V (Low Voltage I/O Application)	-	2	5	uA
		V_{DDIO} = 5V (Internal V_{DD}) (5V I/O Application)	-	130	160	uA
I_{CC}	V_{CC} Supply Current V_{DDIO} = V_{DD} = 3.3V, V_{CC} =12V, Contrast = FFh, IREF =15uA, No panel attached, Display ON, All ON		-	560	670	uA
V_{OH}	High logic output level	I_{OUT} = 100uA, 3.3MHz	0.9* V_{DDIO}	-	-	V
V_{OL}	Low logic output level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1* V_{DDIO}	V
V_{IH}	High logic input level		0.8* V_{DDIO}	-	-	V
V_{IL}	Low logic input level		-	-	0.2* V_{DDIO}	V
I_{SEG}	Segment Output Current, V_{DDIO} = V_{DD} =3.3V (LV I/O)or	Contrast= FFh	-	450	550	uA
		Contrast= AFh	-	340	-	uA
		Contrast= 7Fh	-	225	-	uA

	V_{DDIO} = 5V (5V I/O), V_{CC} = 12V, IREF = 15uA, Display ON	Contrast= 3Fh	-	112	-	uA
		Contrast= 0Fh	-	56	-	uA

ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	24.5	26	mA	All pixels on
Standby mode current consumption	-	1.5	2	mA	Standby mode 10% pixels on
Normal mode power consumption	-	294	312	mW	All pixels on
Standby mode power consumption	-	18	24	mW	Standby mode 10% pixels on
Pixel Luminance	100	120		cd/m^2	Display Average
Standby Luminance		20		cd/m^2	
CIEx (White)	0.25	0.29	0.33		CIE1931
CIEy (White)	0.27	0.31	0.35		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

(1) Normal mode condition :

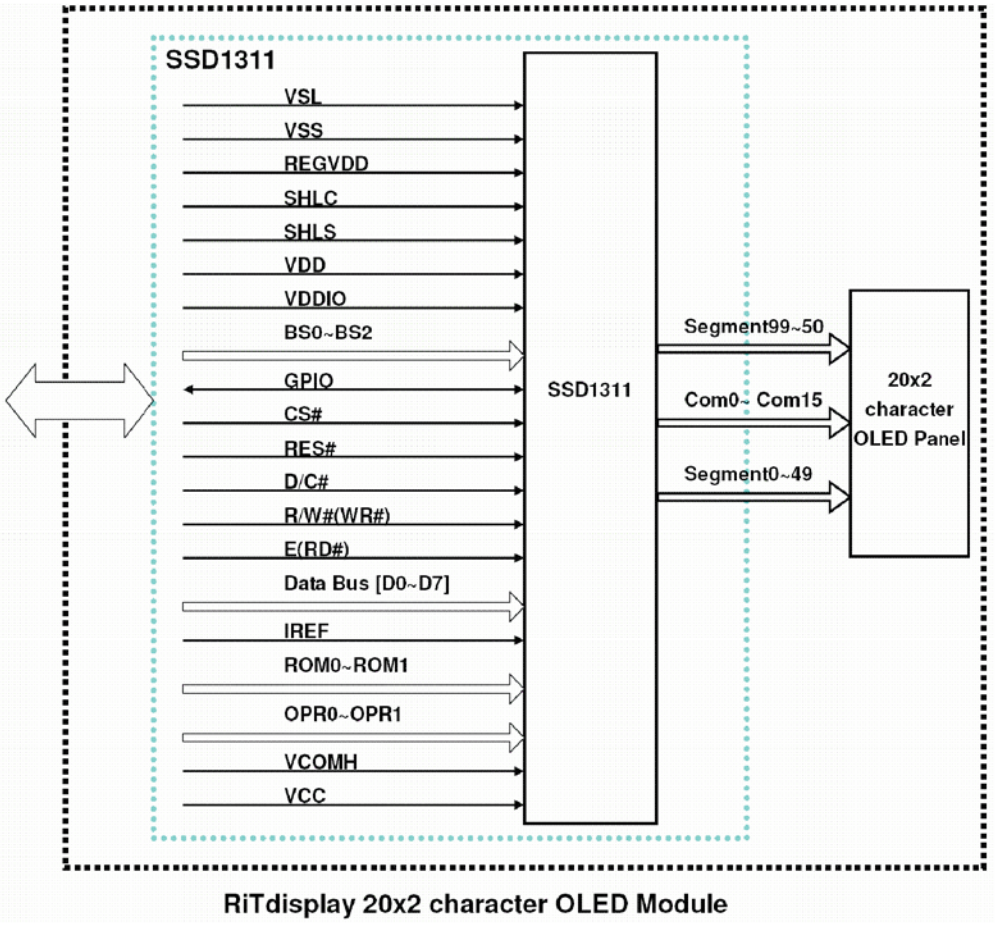
- Driving Voltage : 12V
- Contrast setting : 0x7c
- Frame rate : 105Hz
- Duty setting : 1/16

(2) Standby mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x11
- Frame rate : 105Hz
- Duty setting : 1/16

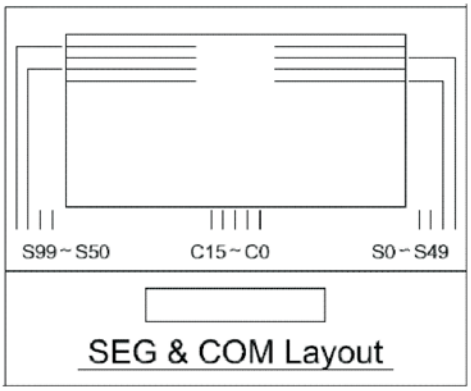
INTERFACE

FUNCTION BLOCK DIAGRAM



RiTdisplay 20x2 character OLED Module

PANEL LAYOUT DIAGRAM



PIN ASSIGNMENTS

<table>
<tr><th>PIN NAME</th><th>PIN NO</th><th>DESCRIPTION</th></tr>
<tr><td>N.C.</td><td>1</td><td>No connection.</td></tr>
<tr><td>VSL</td><td>2</td><td>This is segment voltage reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground.</td></tr>
<tr><td>VSS</td><td>3</td><td>Ground pin.</td></tr>
<tr><td>REGVDD</td><td>4</td><td>Internal VDD regulator selection pin in 5V I/O application mode.
When this pin is pulled HIGH, internal VDD regulator is enabled (5V I/O application).
When this pin is pulled LOW, internal VDD regulator is disabled (Low voltage I/Oapplication).</td></tr>
<tr><td>SHLC</td><td>5</td><td>This pin is used to determine the Common output scanning direction.
<table>
<tr><th>SHLC</th><th>COM scan direction</th></tr>
<tr><td>1</td><td>COM0 to COM31 (Normal)</td></tr>
<tr><td>0</td><td>COM31 to COM0 (Reverse)</td></tr>
</table></td></tr>
<tr><td>SHLS</td><td>6</td><td>This pin is used to change the mapping between the display data column address and the Segment driver.
<table>
<tr><th>SHLS</th><th>SEG direction</th></tr>
<tr><td>1</td><td>SEG0 to SEG99 (Normal)</td></tr>
<tr><td>0</td><td>SEG99 to SEG0 (Reverse)</td></tr>
</table></td></tr>
<tr><td>VDD</td><td>7</td><td>Power supply for core logic operation.

VDD can be supplied externally or regulated internally.
In LV IO application (internal VDD is disabled), this is a power input pin.
In 5V IO application (internal VDD is enabled), VDD is regulated internally from VDDIO.

A capacitor should be connected between VDD and VSS under all circumstances.</td></tr>
<tr><td>VDDIO</td><td>8</td><td>Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.</td></tr>
<tr><td>BS0</td><td>9</td><td>MCU bus interface selection pins.
<table>
<tr><th>BS[2:0]</th><th>Interface</th></tr>
<tr><td>000</td><td>Serial Interface</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>BS1

BS2</td><td>10

11</td><td><table>
<tr><td>001</td><td>Invalid</td></tr>
<tr><td>010</td><td>I²C</td></tr>
<tr><td>011</td><td>Invalid</td></tr>
<tr><td>100</td><td>8-bit 6800 parallel</td></tr>
<tr><td>101</td><td>4-bit 6800 parallel</td></tr>
<tr><td>110</td><td>8-bit 8080 parallel</td></tr>
<tr><td>111</td><td>4-bit 8080 parallel</td></tr>
</table></td></tr>
<tr><td>GPIO</td><td>12</td><td>It is a GPIO pin.</td></tr>
<tr><td>CS#</td><td>13</td><td>This pin is the chip select input connecting to the MCU.</td></tr>
<tr><td>RES#</td><td>14</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>D/C#</td><td>15</td><td>This pin is Data/Command control pin connecting to the MCU.
When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.
In I²C mode, this pin acts as SA0 for slave address selection.
When serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>R/W#(WR#)</td><td>16</td><td>This pin is read / write control input pin connecting to the MCU interface.

When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.

When serial or I²C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>E(RD#)</td><td>17</td><td>This pin is MCU interface input.

When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.

When serial or I²C interface is selected, this pin must be connected to VSS.</td></tr>
</table>

<table>
<tr><td>D0</td><td>18</td><td rowspan="8">These pins are bi-directional data bus connecting to the MCU data bus.
Unused pins are recommended to tie LOW.

When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD.When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td>D1</td><td>19</td></tr>
<tr><td>D2</td><td>20</td></tr>
<tr><td>D3</td><td>21</td></tr>
<tr><td>D4</td><td>22</td></tr>
<tr><td>D5</td><td>23</td></tr>
<tr><td>D6</td><td>24</td></tr>
<tr><td>D7</td><td>25</td></tr>
<tr><td>IREF</td><td>26</td><td>This pin is the segment output current reference pin.
IREF is supplied externally.
A resistor should be connected between this pin and VSS.</td></tr>
<tr><td>ROM0</td><td>27</td><td rowspan="2">These pins are used to select Character ROM; select appropriate logic setting as described in the following table.
<table>
<tr><td>ROM1</td><td>ROM0</td><td>ROM</td></tr>
<tr><td>0</td><td>0</td><td>A</td></tr>
<tr><td>0</td><td>1</td><td>B</td></tr>
<tr><td>1</td><td>0</td><td>C</td></tr>
<tr><td>1</td><td>1</td><td>S/W selectable</td></tr>
</table></td></tr>
<tr><td>ROM1</td><td>28</td></tr>
<tr><td>OPR0</td><td>29</td><td rowspan="2">This pin is used to select the character number of character generator.
<table>
<tr><td>OPR1</td><td>OPR0</td><td>CGROM</td><td>CGRAM</td></tr>
<tr><td>1</td><td>1</td><td>256</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>248</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>250</td><td>6</td></tr>
<tr><td>0</td><td>0</td><td>240</td><td>8</td></tr>
</table></td></tr>
<tr><td>OPR1</td><td>30</td></tr>
<tr><td>VCOMH</td><td>31</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.
No external power supply is allowed to connect to this pin.</td></tr>
<tr><td>VCC</td><td>32</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.</td></tr>
<tr><td>N.C.</td><td>33</td><td>No connection.</td></tr>
</table>

GRAPHIC DISPLAY DATA RAM ADDRESS MAP

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

Display of 5-Dot Font Width Character

5-dot 1-line Display

In case of 1-line display with 5-dot font, the address range of DDRAM is 00H-4FH

1-line x 20ch. Display (5-dot Font Width)

Display position

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM0																				
COM7	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13

SEG0 SEG99

DDRAM Address

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM0																				
COM7	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14

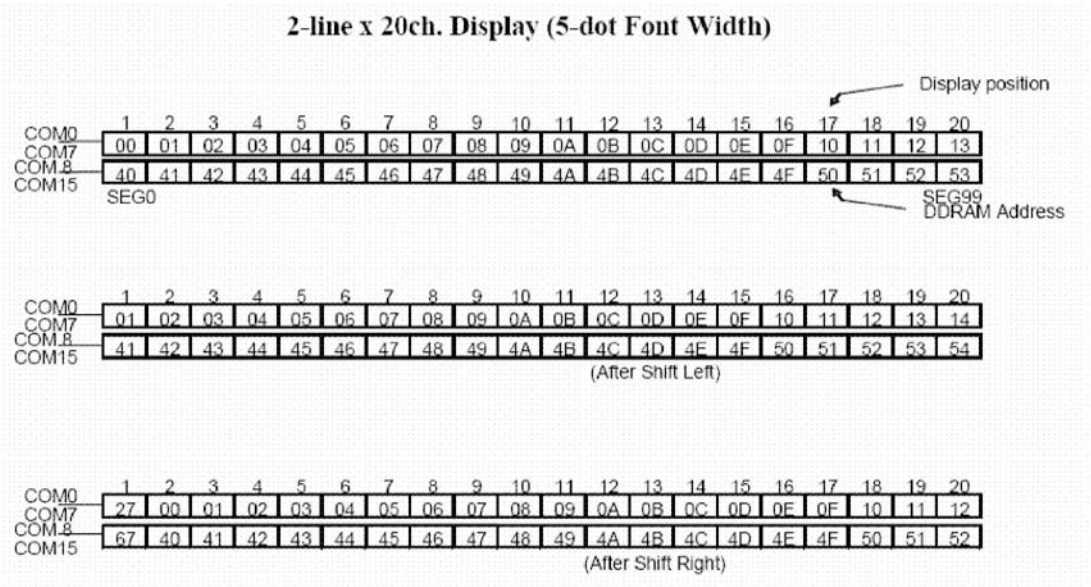
(After Shift Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM0																				
COM7	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12

(After Shift Right)

5-dot 2-line Display

In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-27H, 40H-67H



INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

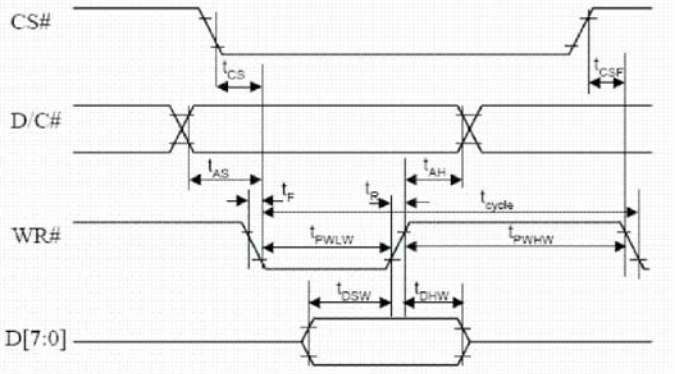
8080-Series MCU Parallel Interface Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

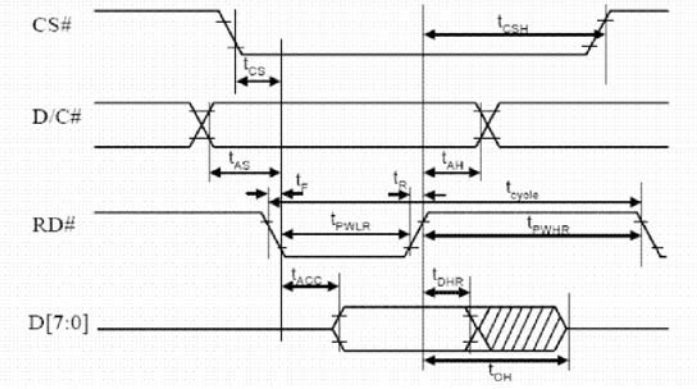
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	.0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

8080-series parallel interface characteristics

Write cycle



Read Cycle



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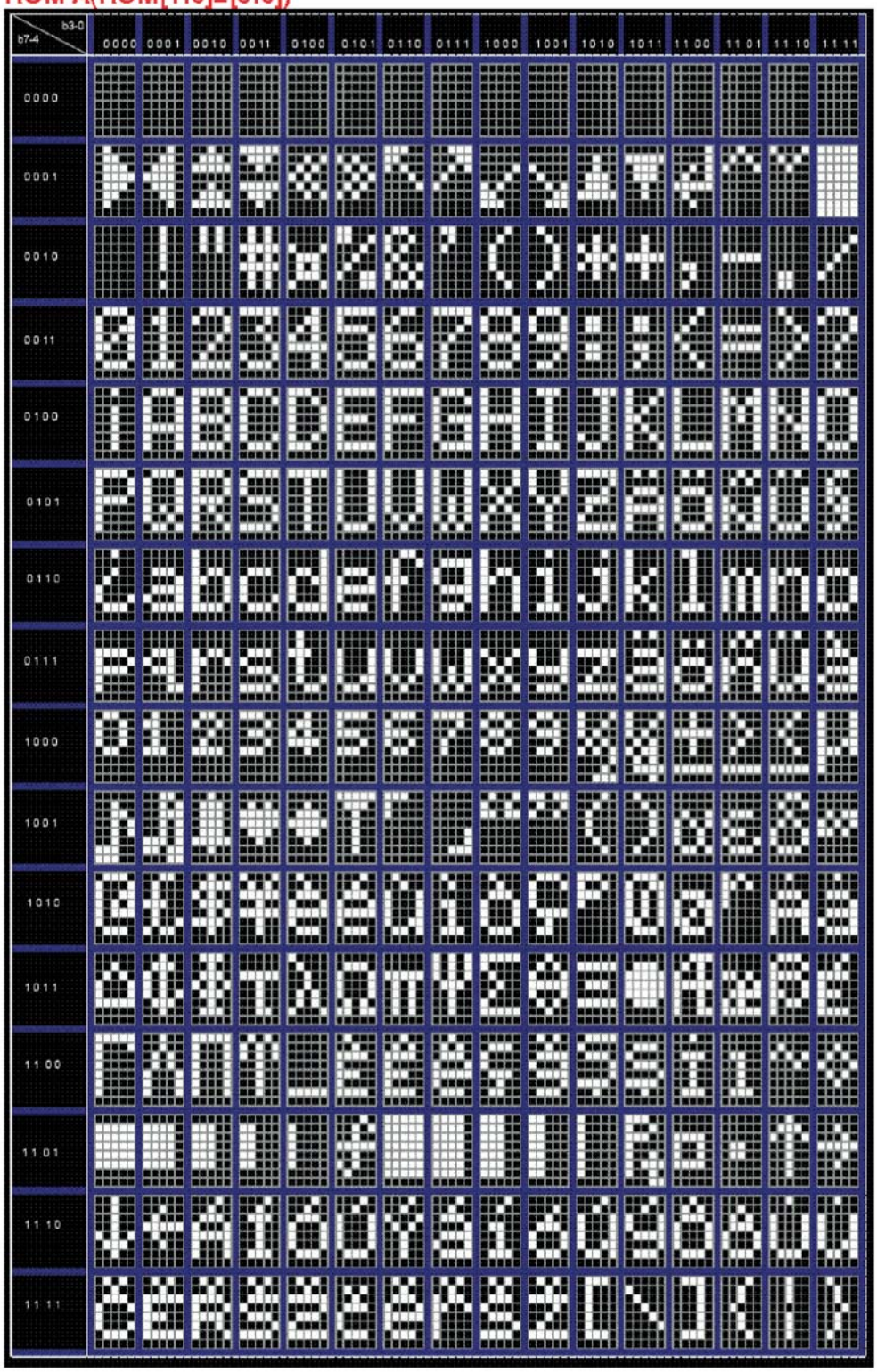
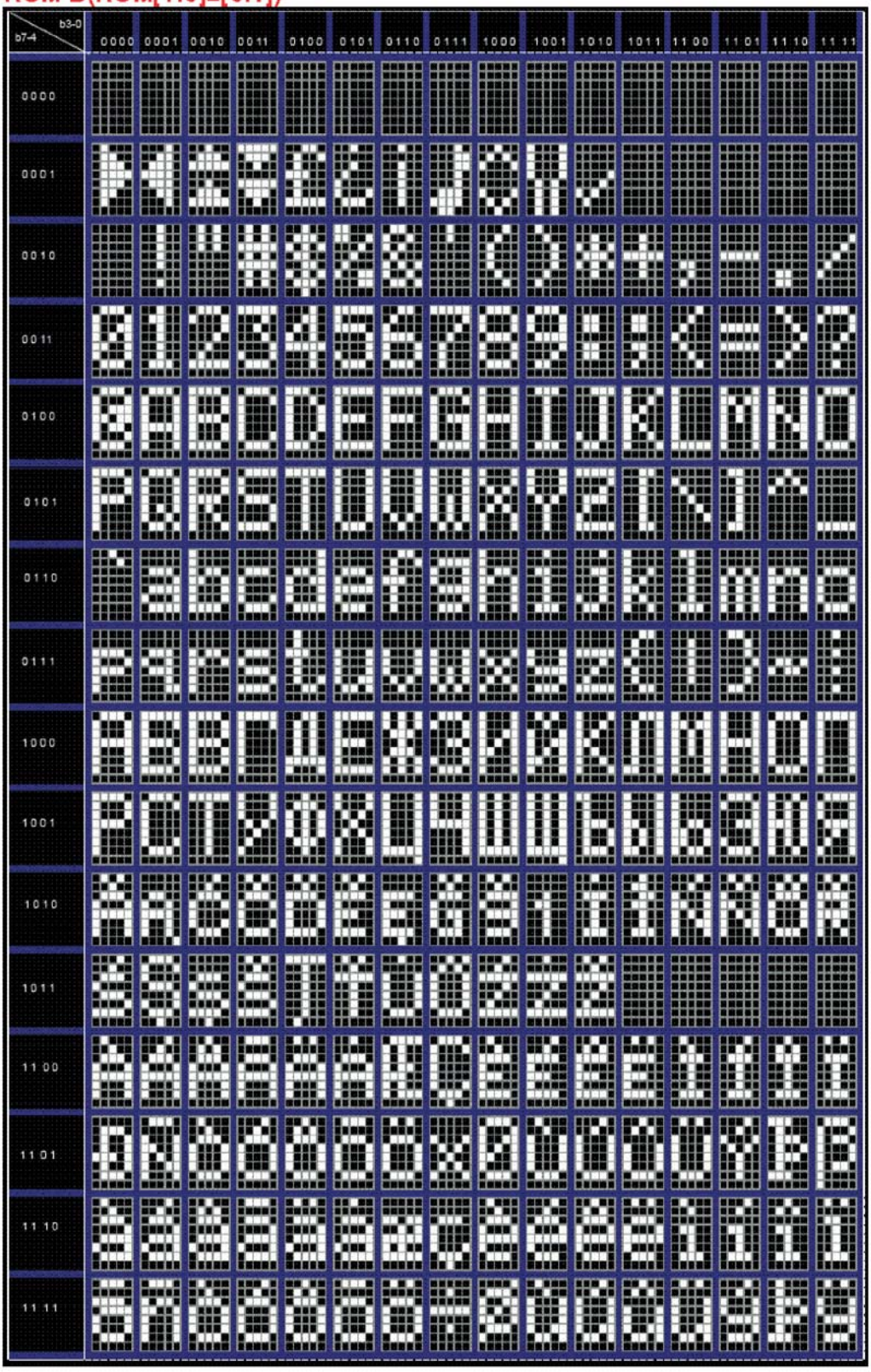
7.6 BUILT-IN CGROM CHARACTER CODE

ROM A(ROM[1:0]=[0:0])



ROM B(ROM[1:0]=[0:1])



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ROM C(ROM[1:0]=[1:0])

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POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

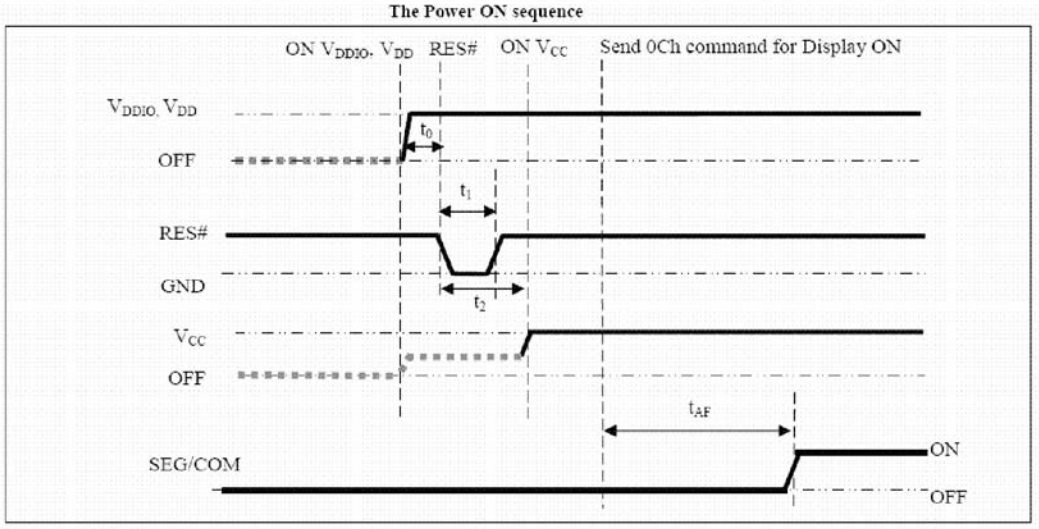
POWER ON / OFF SEQUENCE

When low voltage (2.4V~3.6V) I/O mode is chosen:

Power ON sequence:

1. Power ON V_{DDIO}, V_{DD}
2. After V_{DDIO}, V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON.SEG/COM will be ON after 100ms (t_{AF}).

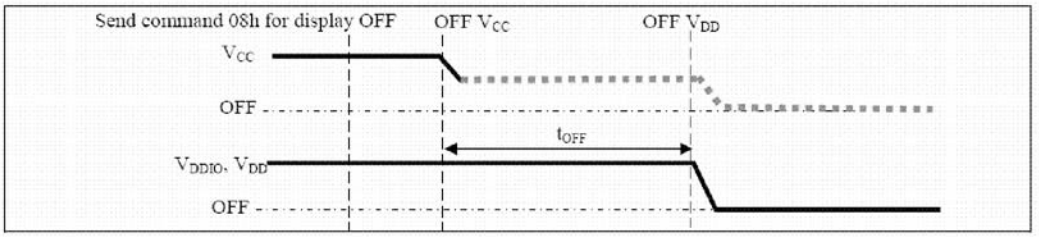
The Power ON sequence



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Power OFF V_{DDIO}, V_{DD} after t_{OFF}. (where Minimum t_{OFF}=80ms [5], Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

(3) Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

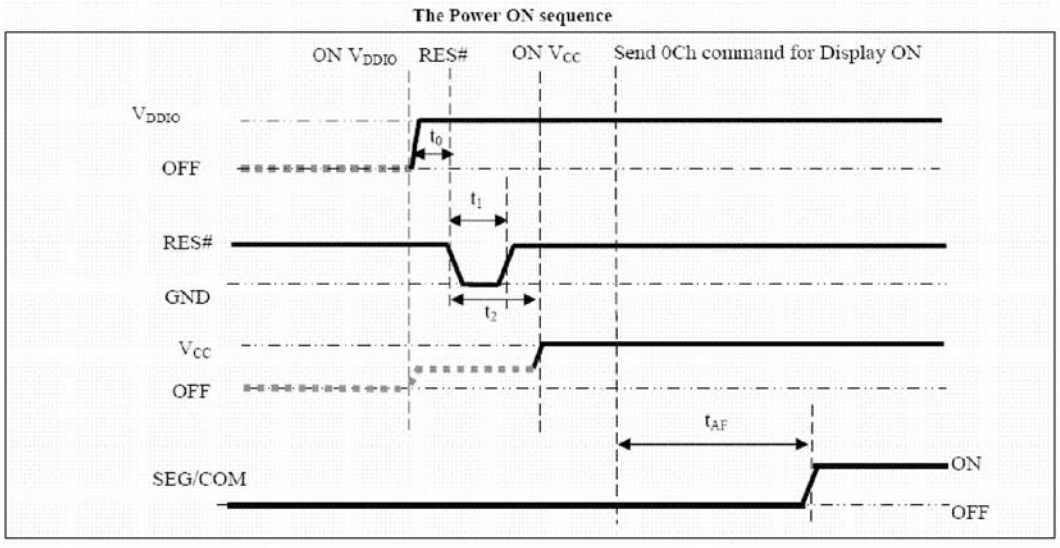
(4) The register values are reset after t_1.

(5) V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

When 5V I/O mode is chosen:

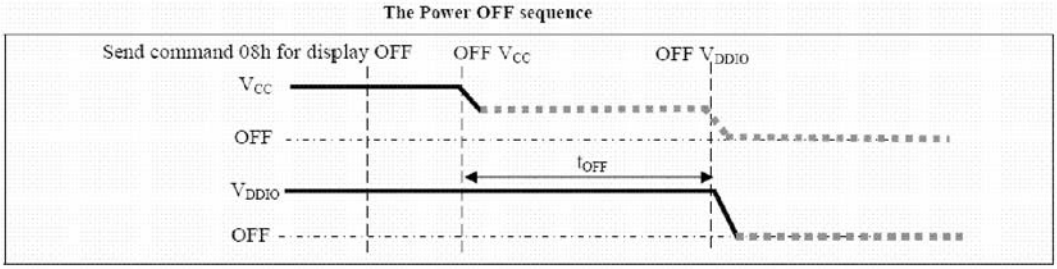
Power ON sequence:

1. Power ON V_{DDIO}
2. After V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON.SEG/COM will be ON after 200ms (t_{AF}).



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Power OFF V_{DDIO} after t_{OFF}. (where Minimum t_{OFF}=80ms [5], Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

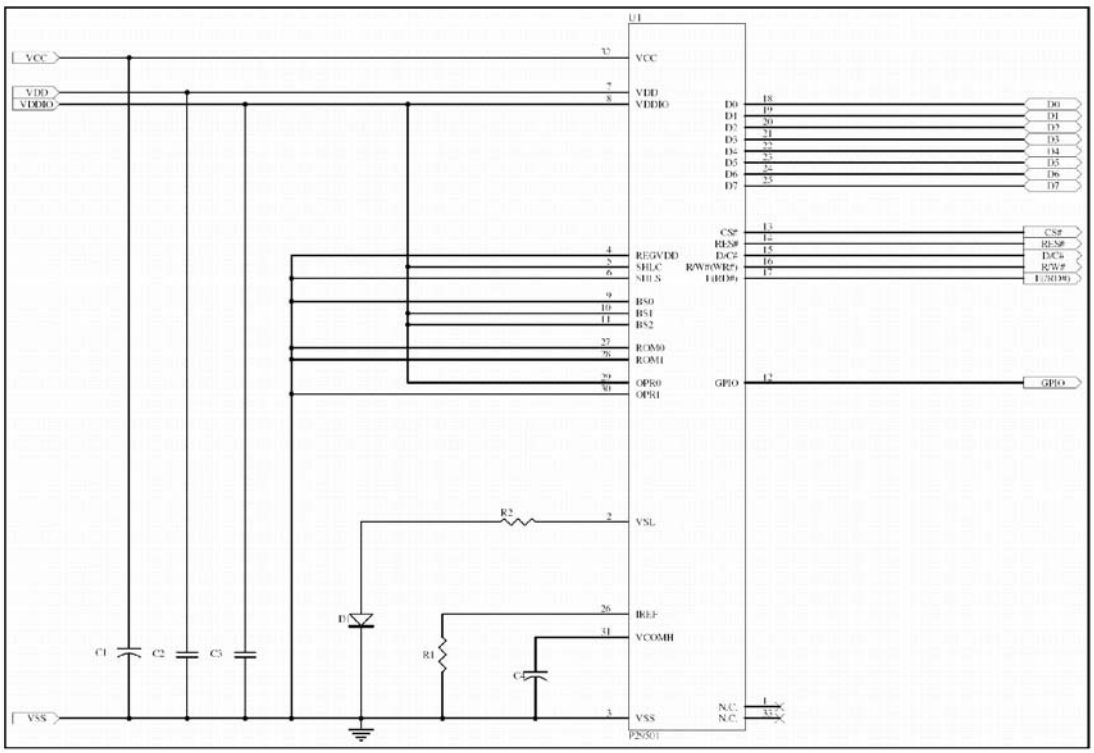
(3) Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

APPLICATION CIRCUIT

(CHARACTER CODE:ROM A) (CGROM:248,CGRAM:8)



Recommend components:

C1, C4: 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)

C2, C3: 1uF/16V(0603)

R1: 470K ohm 1%(0603)

R2: 50 ohm 1/4W

D1: ≤1.4V 0.5W

This circuit is for 8080 8bits interface.

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RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

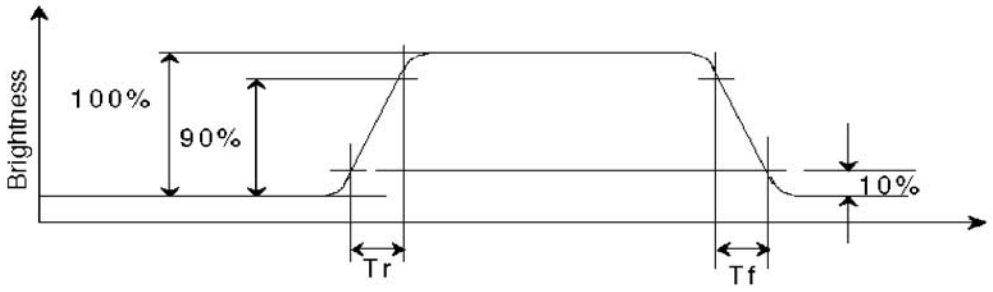


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

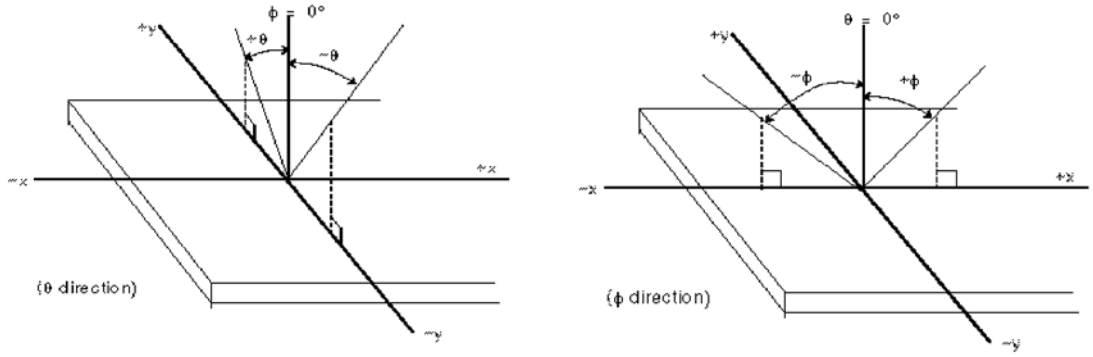
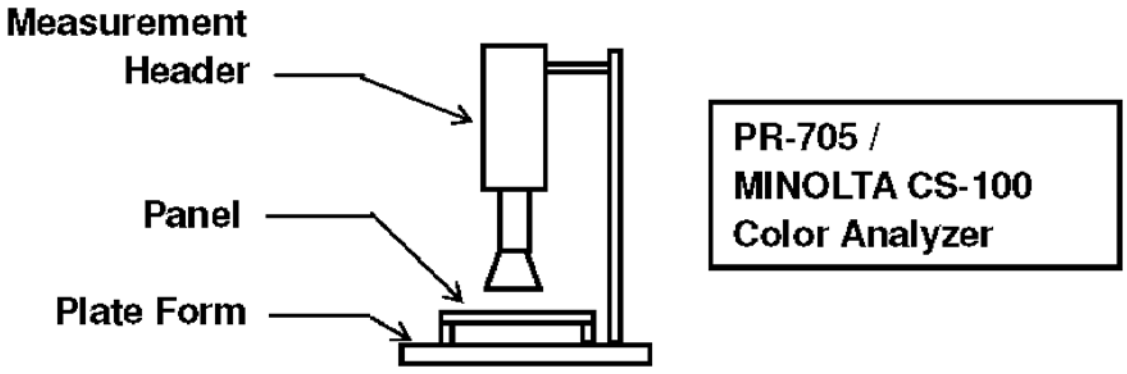


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

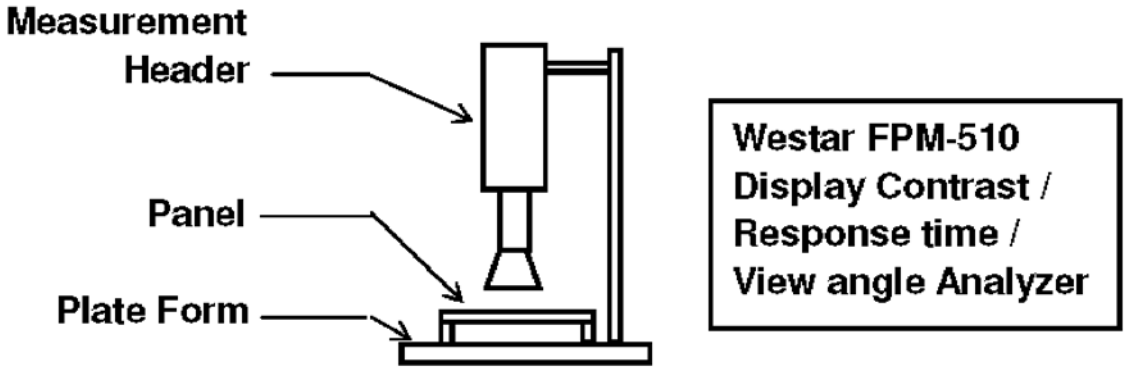
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

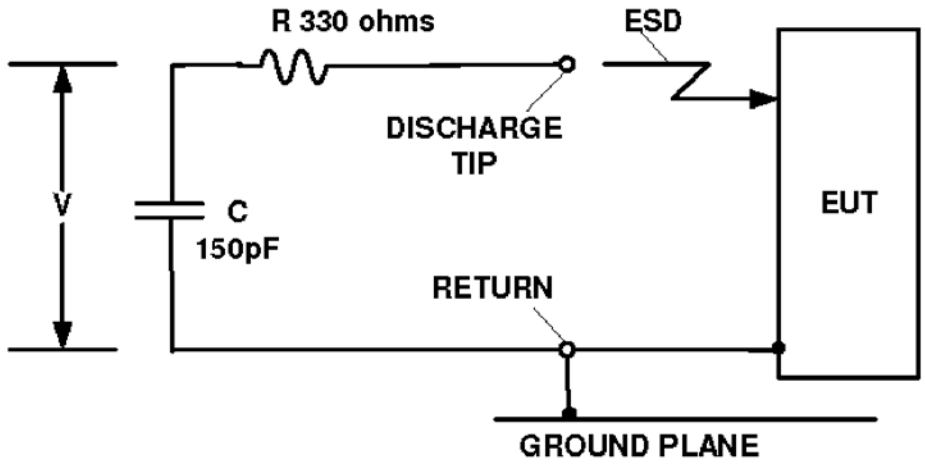


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



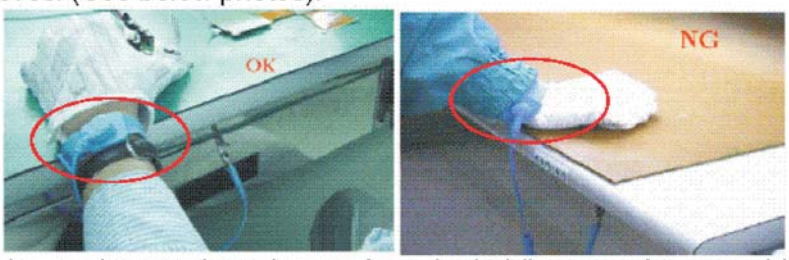
APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



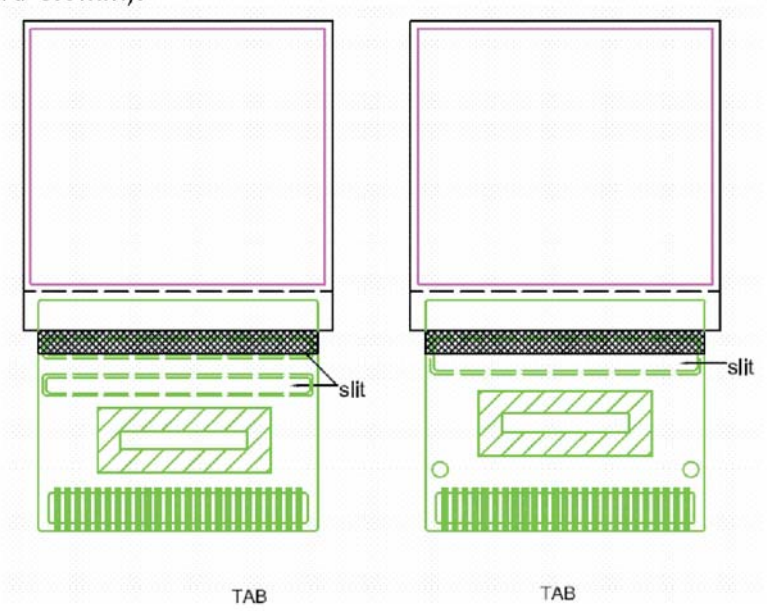
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

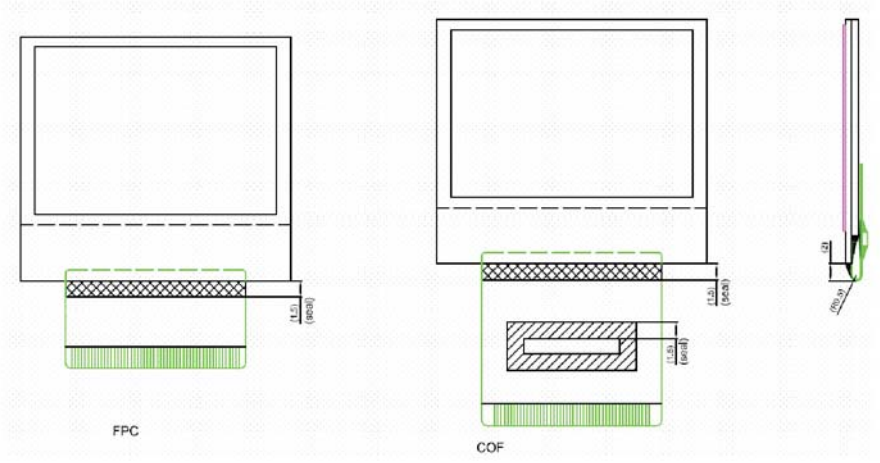
5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

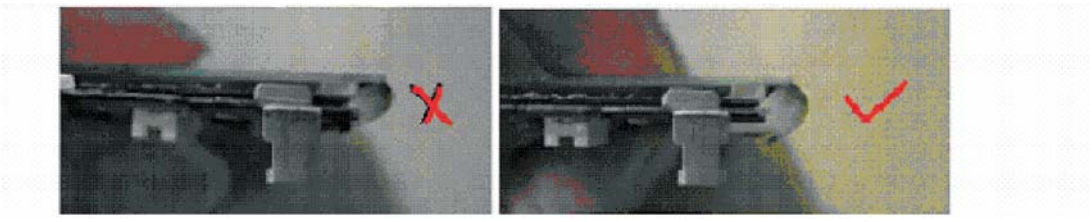
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).







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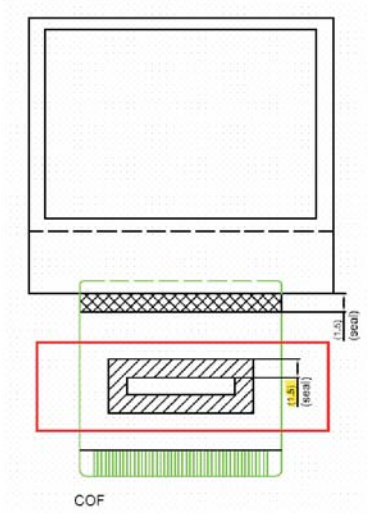
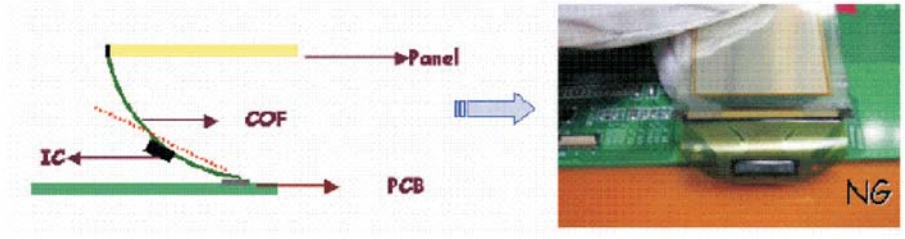
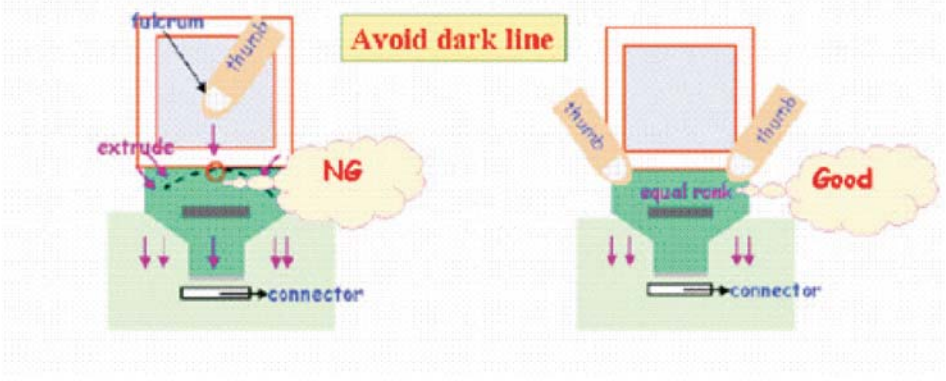
9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.





10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.



11. The working area for the panel should be kept clean. If the panel is accidentally dropped on the floor, do visual inspection of the panel first. Please use clean-room wiping cloth moistened with alcohol to wipe it off if dirt or grease stains the panel.

12. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

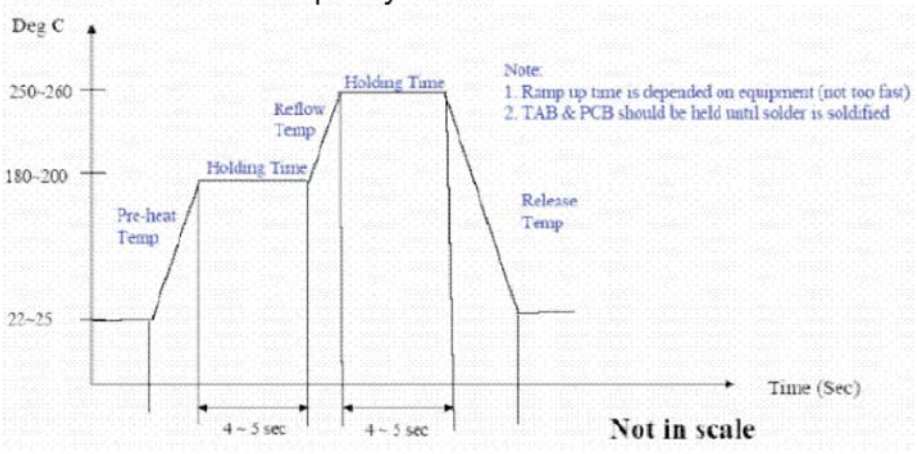
13. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

14. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

15. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

16. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

17. Suggestion for soldering process:
    i. TAB Lead- free soldering hot bar process
        1. Use pulse heated bonding tool equipment
        2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
        3. Bonding Force:--4kg per centimeter square as the starting point.
        4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.



ii. TAB Lead- free soldering wire process

In case of manual soldering (Lead- free solder wire)

1. Solder wire contact iron directly: 280±5℃ at 3-5secs
2. Solder wire contact TAB lead directly (near iron but not contact): 380±5 ℃, 3-5secs
3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380 ℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

Precautions for Electrical

1. Design using the settings in the specification

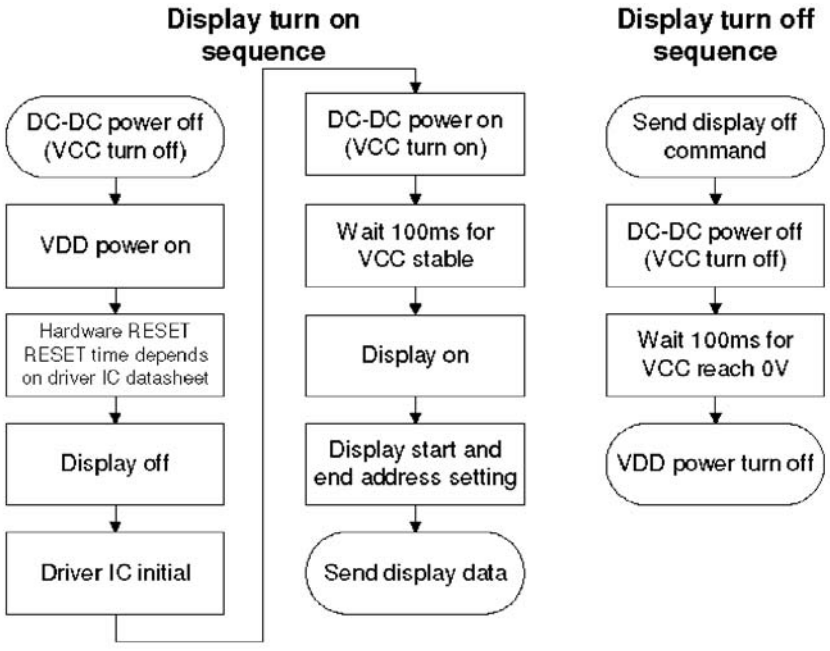
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

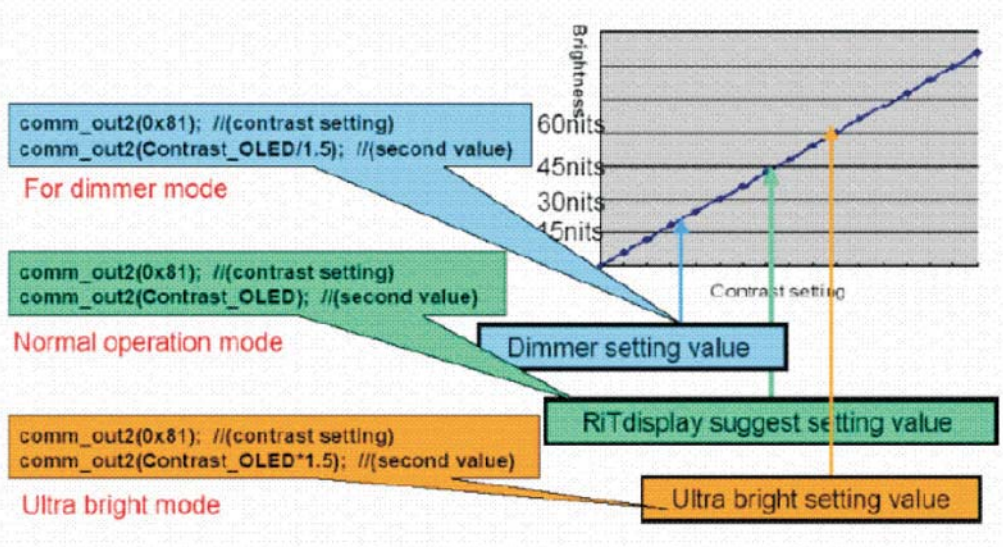
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



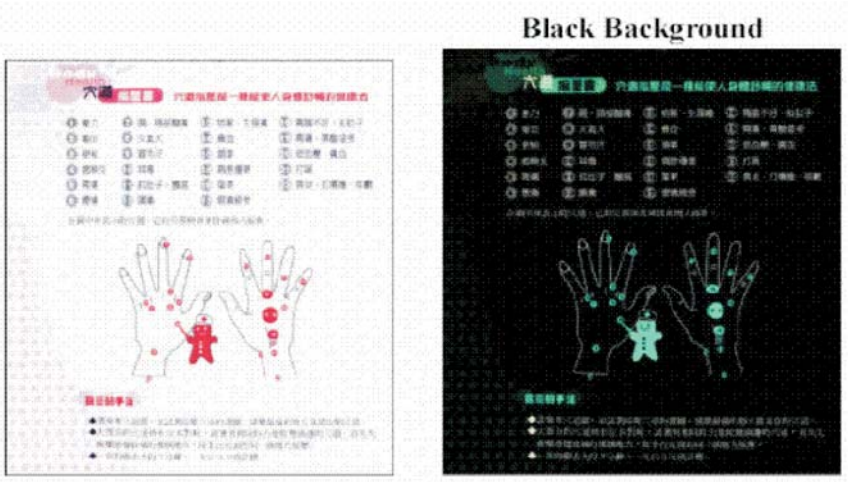
5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

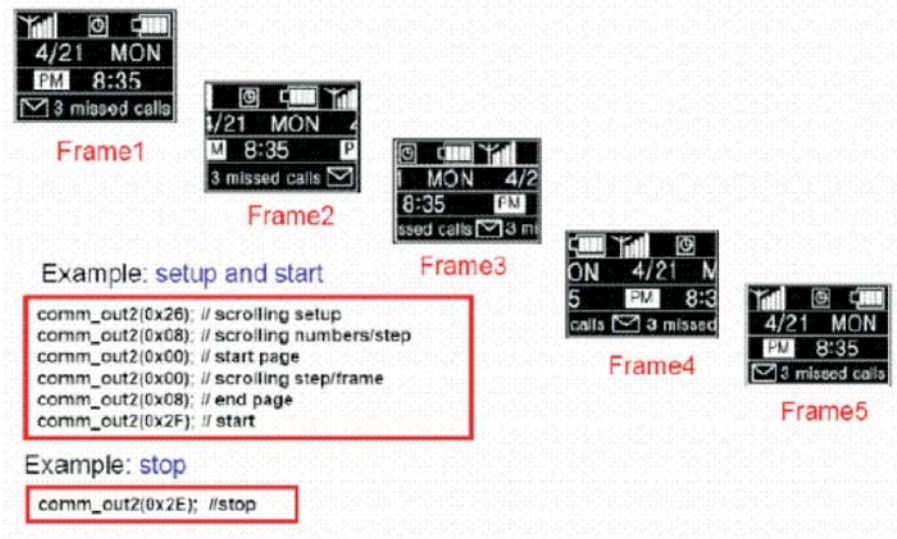
6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays
3. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.



Scrolling example



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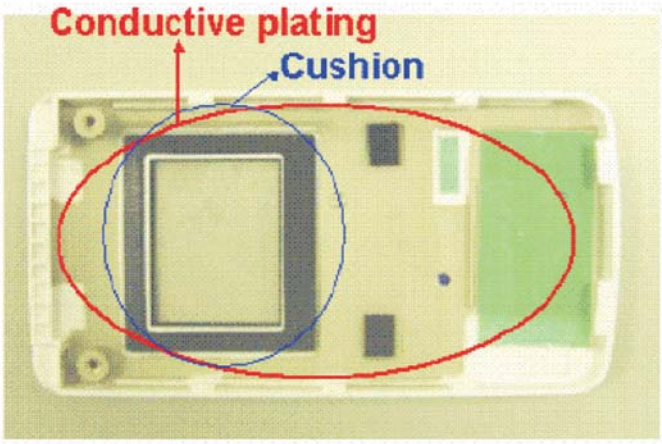
Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

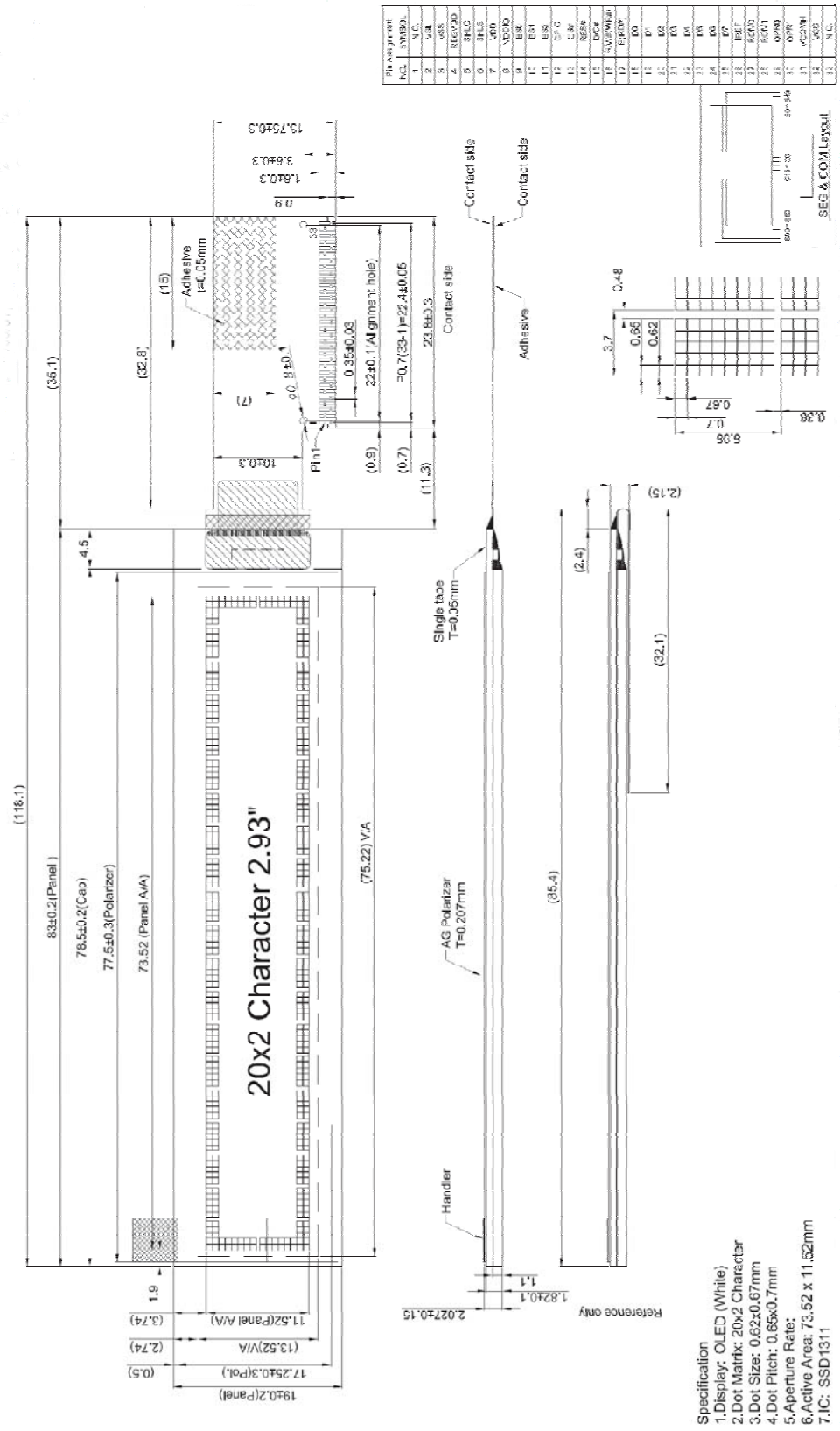
It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.



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