GD25Q21B
DATASHEET

- Content -

1. FEATURES

♦ 2M-bit Serial Flash

- 256K-byte
- 256 bytes per programmable page

♦ Standard, Dual, Quad SPI

- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3

♦ High Speed Clock Frequency

- 104MHz for fast read with 30PF load
- Dual I/O Data transfer up to 208Mbits/s
- Quad I/O Data transfer up to 416Mbits/s

♦ Software/Hardware Write Protection

- Write protect all/portion of memory via software
- Enable/Disable protection with WP# pin
- Top or Bottom, Sector or Block selection

♦ Program/Erase Speed

- Page Program time: 0.35ms typical
- Sector Erase time: 50ms typical
- Block Erase time: 0.18/0.25s typical
- Chip Erase time: 0.8s typical

♦ Flexible Architecture

- Sector of 4K-byte
- Block of 32/64K-byte

♦ Low Power Consumption

- 12mA maximum active current
- 5μA maximum power down current

♦ Single Power Supply Voltage

- Full voltage range: 2.7~3.6V

♦ Minimum 100,000 Program/Erase Cycles

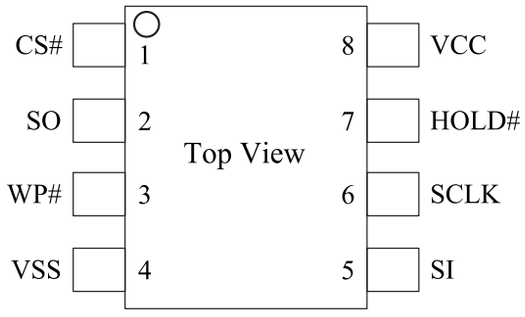
♦ Advanced security Features

- Power Supply Lock-Down
- 3×512-Byte Security Registers With OTP Locks
- Volatile and Non-volatile Status Register Bits

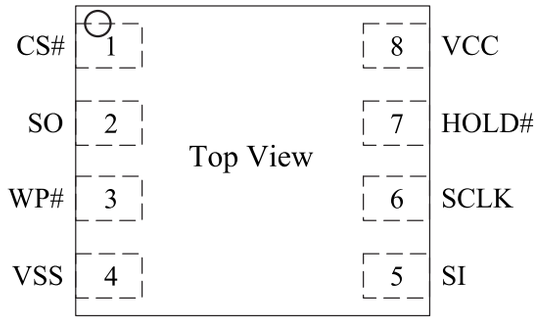
2. GENERAL DESCRIPTION

The GD25Q21B Serial flash supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz for Dual Output & Dual I/O read command, and 416MHz for Quad output & Quad I/O read command.

Connection Diagram



8-LEAD SOP



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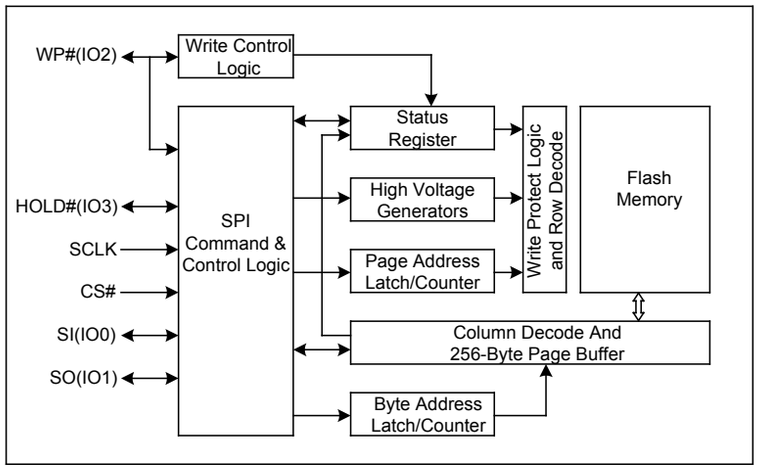
Pin Description

Pin Name	I / O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
VCC		Power Supply

Block Diagram



3. MEMORY ORGANIZATION

GD25Q21B

Each device has	Each block has	Each sector has	Each page has	
256K	64/32K	4K	256	bytes
1K	256/128	16	-	pages
64	16/8	-	-	sectors
4/8	-	-	-	blocks

Uniform Block Sector Architecture

GD25Q21B 64K Bytes Block Sector Architecture

Block	Sector	Address range	
3	64	03F000H	03FFFFH
	-----	-----	-----
	-----	-----	-----
2	47	02F000H	02FFFFH
	-----	-----	-----
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	-----	-----	-----
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	-----	-----	-----
	0	000000H	000FFFH

4. DEVICE OPERATION

SPI Mode

Standard SPI

The GD25Q21B feature a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25Q21B supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

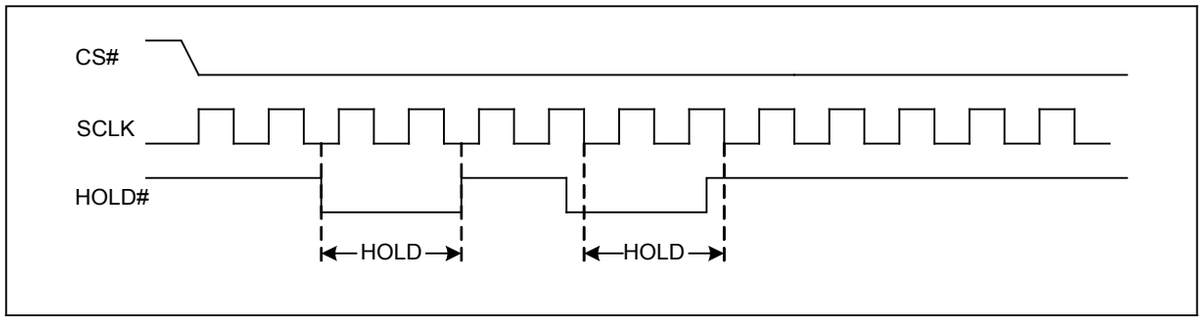
Quad SPI

The GD25Q21B supports Quad SPI operation when using the "Quad Output Fast Read"," Quad I/O Fast Read", "Quad I/O Word Fast Read", "Quad Page Program" (6BH, EBH, E7H, 32H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress. The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low). The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure 1. Hold Condition



5. DATA PROTECTION

The GD25Q21B provides the following data protection methods:

- ♦ Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  - Erase Security Register / Program Security Register
- ♦ Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- ♦ Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP0~1 bits.
- ♦ Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0 GD25Q21B Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	×	×	0	0	NONE	NONE	NONE	NONE
0	0	×	0	1	3	030000H-03FFFFH	64KB	Upper 1/4
0	0	×	1	0	2 and 3	020000H-03FFFFH	128KB	Upper 1/2
0	1	×	0	1	0	000000H-00FFFFH	64KB	Lower 1/4
0	1	×	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/2
0	×	×	1	1	0 to 3	000000H-03FFFFH	256KB	ALL
1	×	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000H-03FFFFH	4KB	Upper 1/64
1	0	0	1	0	3	03E000H-03FFFFH	8KB	Upper 1/32
1	0	0	1	1	3	03C000H-03FFFFH	16KB	Upper 1/16
1	0	1	0	×	3	038000H-03FFFFH	32KB	Upper 1/8
1	0	1	1	0	3	038000H-03FFFFH	32KB	Upper 1/8
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/64
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/32
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/16
1	1	1	0	×	0	000000H-007FFFH	32KB	Lower 1/8
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/8
1	×	1	1	1	0 to 3	000000H-03FFFFH	256KB	ALL

Table1.0. GD25Q21B Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	×	×	0	0	0 to 3	000000H-03FFFFH	256KB	ALL
0	0	×	0	1	0 to 2	000000H-02FFFFH	192KB	Lower 3/4
0	0	×	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/2
0	1	×	0	1	1 to 3	010000H-03FFFFH	192KB	Upper 3/4
0	1	×	1	0	2 and 3	020000H-03FFFFH	128KB	Upper 1/2
0	×	×	1	1	NONE	NONE	NONE	NONE
1	×	0	0	0	0 to 3	000000H-03FFFFH	256KB	ALL
1	0	0	0	1	0 to 3	000000H-03EFFFH	252KB	Lower 63/64
1	0	0	1	0	0 to 3	000000H-03DFFFH	248KB	Lower 31/32
1	0	0	1	1	0 to 3	000000H-03BFFFH	240KB	Lower 15/16
1	0	1	0	×	0 to 3	000000H-037FFFH	224KB	Lower 7/8
1	0	1	1	0	0 to 3	000000H-037FFFH	224KB	Lower 7/8
1	1	0	0	1	0 to 3	001000H-03FFFFH	252KB	Upper 63/64
1	1	0	1	0	0 to 3	002000H-03FFFFH	248KB	Upper 31/32
1	1	0	1	1	0 to 3	004000H-03FFFFH	240KB	Upper 15/16
1	1	1	0	×	0 to 3	008000H-03FFFFH	224KB	Upper 7/8
1	1	1	1	0	0 to 3	008000H-03FFFFH	224KB	Upper 7/8
1	×	1	1	1	NONE	NONE	NONE	NONE

6. STATUS REGISTER

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	LB3	LB2	LB1	HPF	QE	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile (Default Value is 0). They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to “None protected”.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	#WP	Status Register	Description
0	0	×	Software Protected	WP# pin has no control. The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When WP# pin is high the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	×	Power Supply Lock-Down(1)	Status Register is protected and can not be written to again until the next Power-Down, Power-Up cycle.
1	1	×	One Time Program(2)	Status Register is permanently protected and can not be written to.

NOTE: (1). When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
(2). This feature is available on special order. Please contact ELM for details.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

HPF bit.

The High Performance Flag (HPF) bit indicates the status of High Performance Mode (HPM). When HPF bit sets to 1, it means the device is in High Performance Mode, when HPF bit sets 0 (default), it means the device is not in High Performance Mode.

LB3, LB2, LB1, bits.

The LB3, LB2, LB1, bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1 are 0, the security registers are unlocked. The LB3-LB1 bits can be set to 1 individually using the Write Register instruction. The LB3-LB1 bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

SUS bit.

The SUS bit is read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75H) command. The SUS bit is cleared to 0 by Erase/Program Resume (7AH) command as well as a power-down, power-up cycle.

7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Volatile SR Write Enable	50H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8) (1)				
Write Status Register-1	31H	(S15-S8)					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	D7-D0 (2)	(continuous)
Dual I/O Fast Read	BBH	A23-A8 (3)	A7-A0 M7-M0 (3)	(D7-D0) (2)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) (4)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0 (5)	dummy (6)	(D7-D0) (4)			(continuous)
Quad I/O Word Fast Read (8)	E7H	A23-A0 M7-M0 (5)	dummy (7)	(D7-D0) (4)			(continuous)
Continuous Read Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0 (4)		
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Set Burst with Wrap	77H	dummy (10) W7-W0					
Program/Erase Suspend	75H						
Program/Erase Resume	7AH						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/ Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Manufacturer/ Device ID by Dual I/O	92H	A23-A8	A7-A0, M7-M0	(MID7-MID0) (DID7-DID0			(continuous)
Manufacturer/ Device ID by Quad I/O	94H	A23-A0, M7-M0	dummy (11) (MID7- MID0) (DID7-DID0)				(continuous)
Read Identification	9FH	(M7-M0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
High Performance Mode	A3H	dummy	dummy	dummy			
Erase Security Registers (9)	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers (9)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	
Read Security Registers (9)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	

NOTE:

(1) Write Status Register (01H)

Normally, Write Status Register (01H) is used to write both lower status register and higher status register; However, if CS# goes up at the eighth bit of the data byte, the data byte would be written as lower byte of status register, without changing the higher byte of status register.

(2) Dual Output data

IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

(3) Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

(4) Quad Output Data

IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3,…..)

(5) Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

(6) Fast Read Quad I/O Data

IO0 = (x, x, x, x, D4, D0,…)
IO1 = (x, x, x, x, D5, D1,…)
IO2 = (x, x, x, x, D6, D2,…)
IO3 = (x, x, x, x, D7, D3,…)

(7) Fast Word Read Quad I/O Data

IO0 = (x, x, D4, D0,…)
IO1 = (x, x, D5, D1,…)
IO2 = (x, x, D6, D2,…)
IO3 = (x, x, D7, D3,…)

(8) Fast Word Read Quad I/O Data: the lowest address bit must be 0.

(9) Security Registers Address:

Security Register1: A23-A16=00H, A15-A9=0001000b, A8-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A9=0010000b, A8-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A9=0011000b, A8-A0= Byte Address.

(10) Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)
IO1 = (x, x, x, x, x, x, W5, x)
IO2 = (x, x, x, x, x, x, W6, x)
IO3 = (x, x, x, x, x, x, W7, x)

(11) Address, Continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID

IO0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0, …)
IO1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1, …)
IO2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2, …)
IO3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3, …)

Table of ID Definitions:

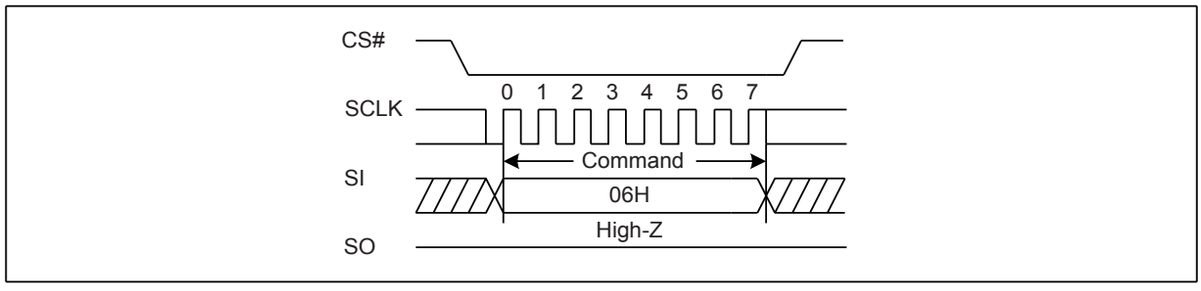
GD25Q21B

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	C8	40	12
90H	C8		11
ABH			11

7.1. Write Enable (WREN)(06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR), Program Security Register, Erase Security Register command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

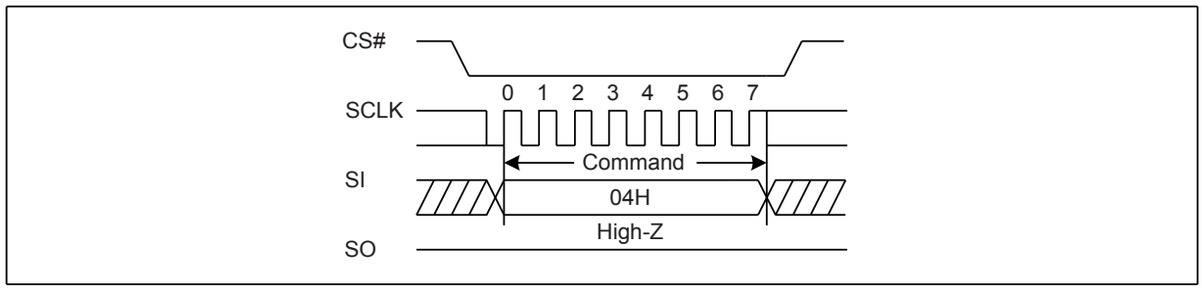
Figure 2. Write Enable Sequence Diagram



7.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase, Program Security Register, Erase Security Register commands.

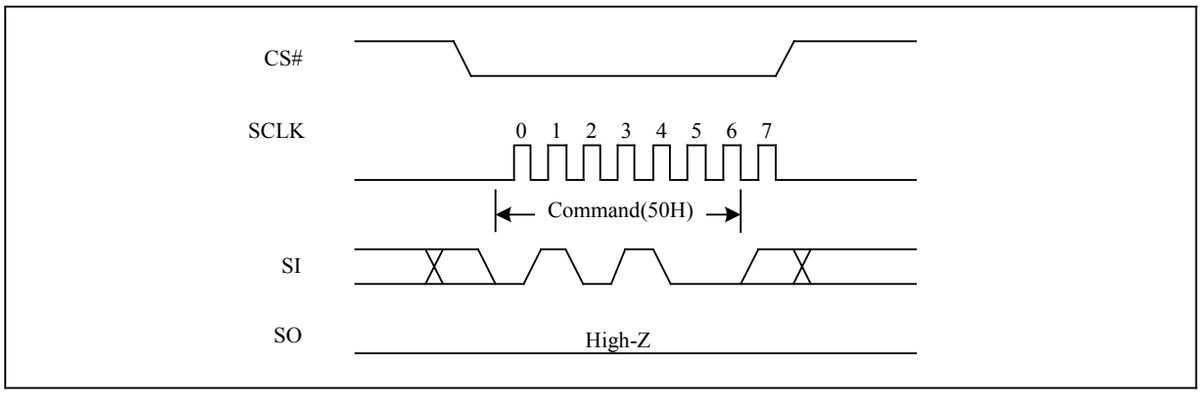
Figure 3. Write Disable Sequence Diagram



7.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

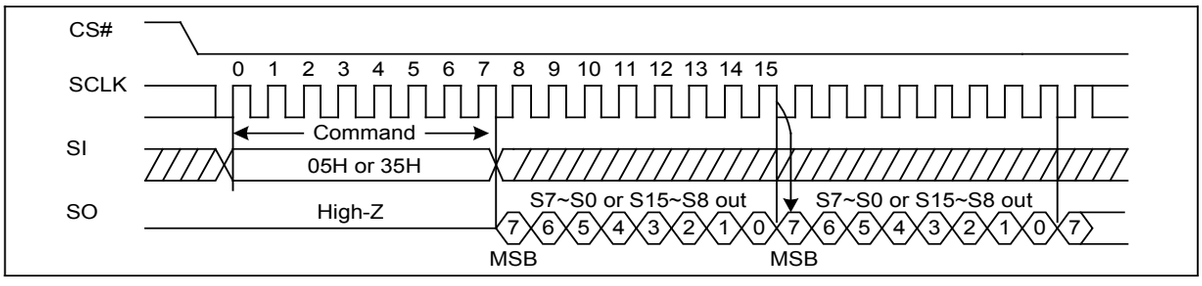
Figure 4. Write Enable for Volatile Status Register Sequence Diagram



7.4. Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

Figure 5. Read Status Register Sequence Diagram



7.5. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

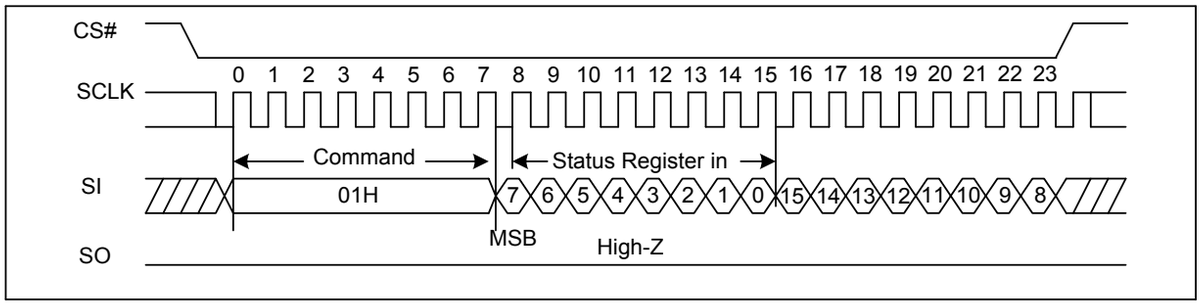
The Write Status Register (WRSR) (01H) command has no effect on S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tw) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register Instruction. Once write enabled, the instruction is entered by driving CS# low, sending the instruction code "01h", and then writing the status register data byte.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB3, LB2, LB1 can not be changed from 1 to 0 because of the OTP protection for these bits. Upon power off, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored when power on again.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure 6. Write Status Register Sequence Diagram



7.6. Write Status Register (WRSR) (31H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

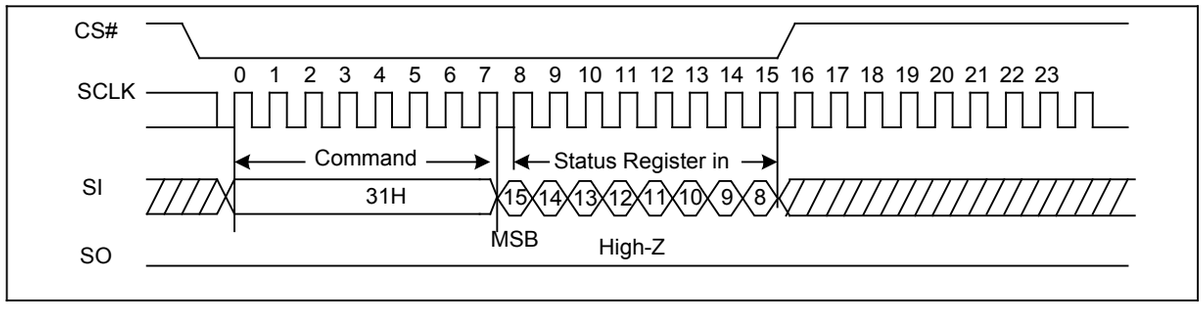
The Write Status Register (WRSR) command (31H) has no effect on S15 and S10 of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tw) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register Instruction. Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “31h”, and then writing the status register data byte.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB3, LB2, LB1 can not be changed from 1 to 0 because of the OTP protection for these bits. Upon power off, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored when power on again.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

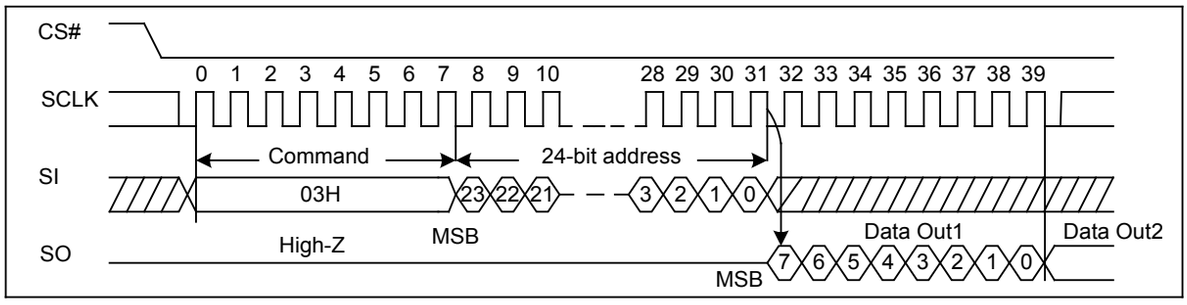
Figure 7. Write Status Register Sequence Diagram



7.7. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

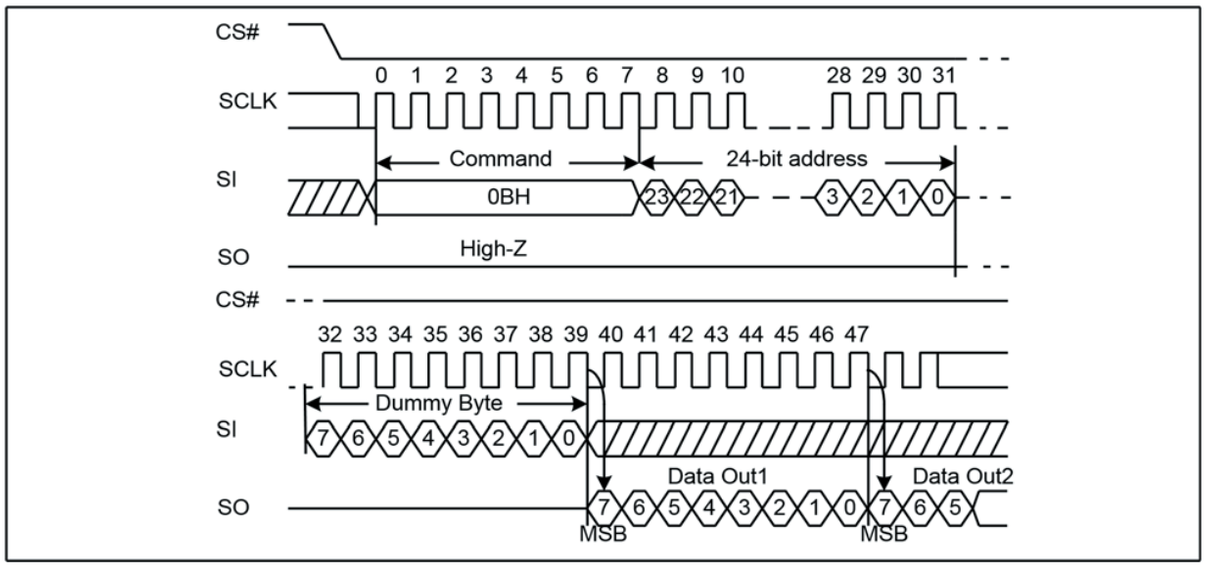
Figure 8. Read Data Bytes Sequence Diagram



7.8. Read Data Bytes at Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

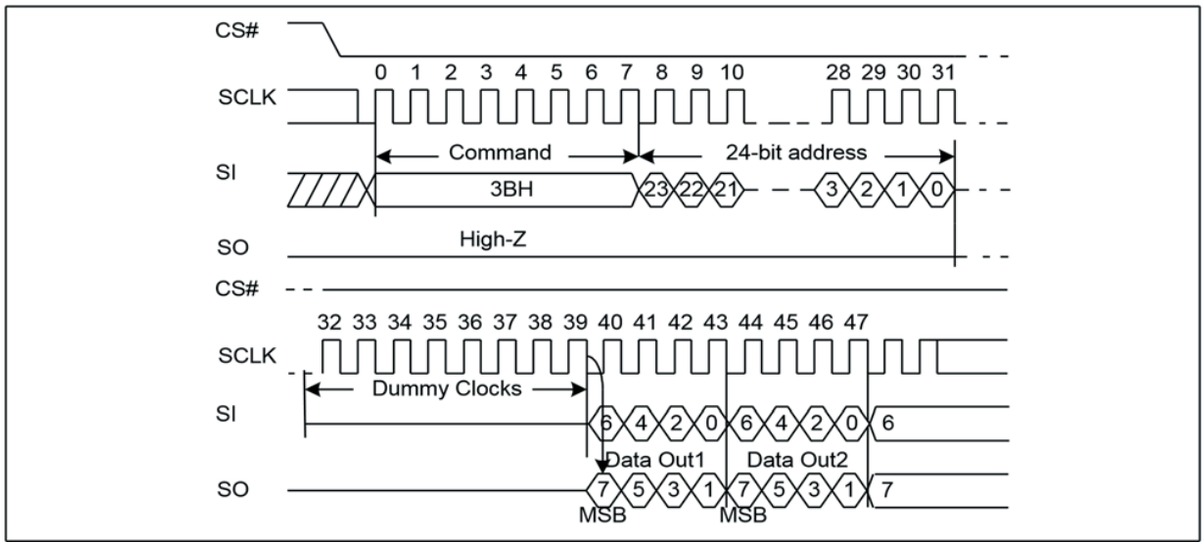
Figure 9. Read Data Bytes at Higher Speed Sequence Diagram



7.9. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

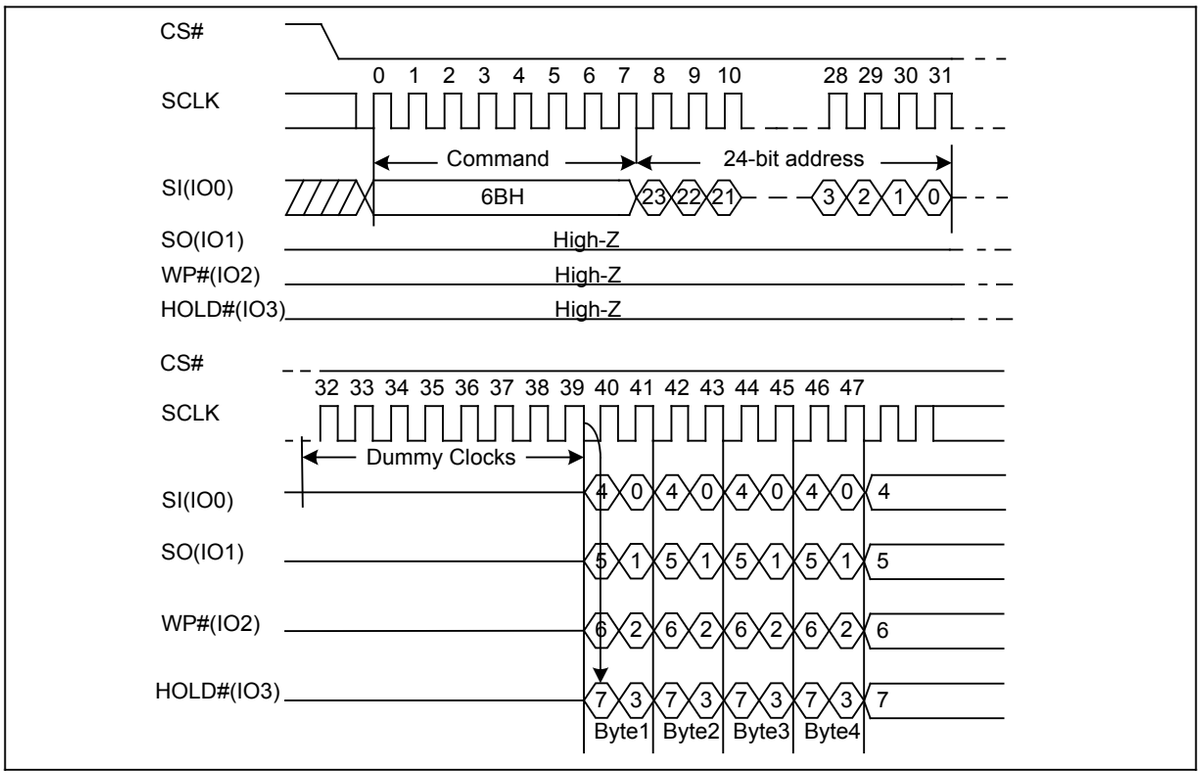
Figure 10. Dual Output Fast Read Sequence Diagram



7.10. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure11. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 11. Quad Output Fast Read Sequence Diagram



7.11. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure12. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. To ensure optimum performance the High Performance Mode (HPM) command (A3H) must be executed once, prior to the Dual I/O Fast Read command.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M7-0) =AXH, then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure13. If the “Continuous Read Mode” bits (M7-0) are any value other than AXH, the next command requires the first BBH command code, thus

returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

Figure 12. Dual I/O Fast Read Sequence Diagram (M7-0 = 0XH or not AXH)

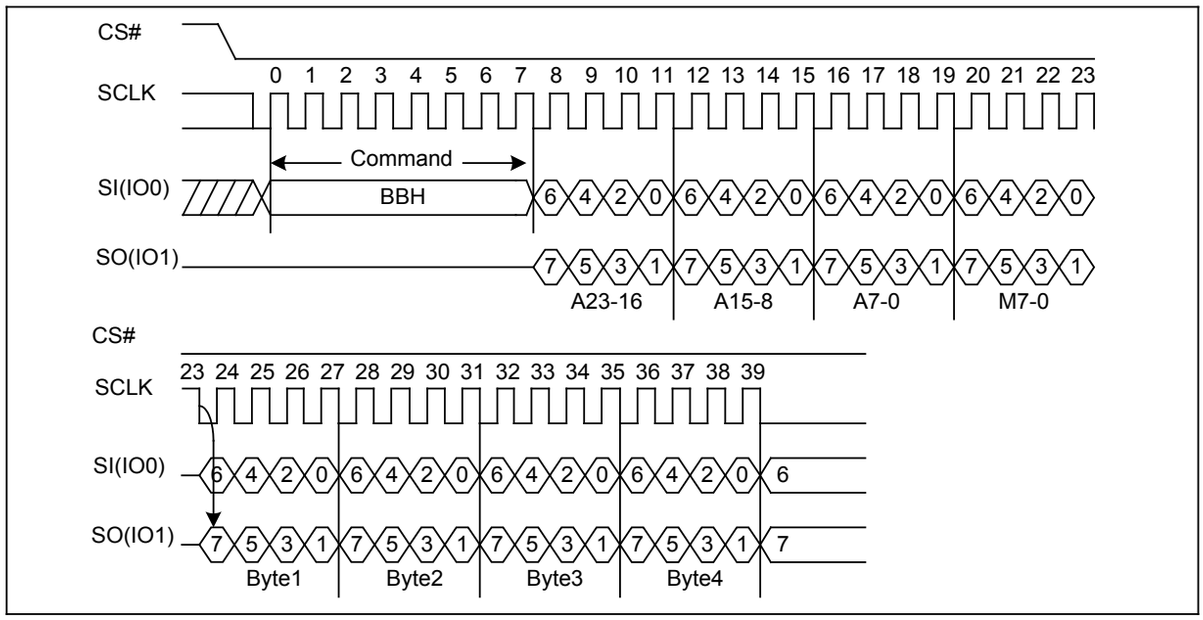
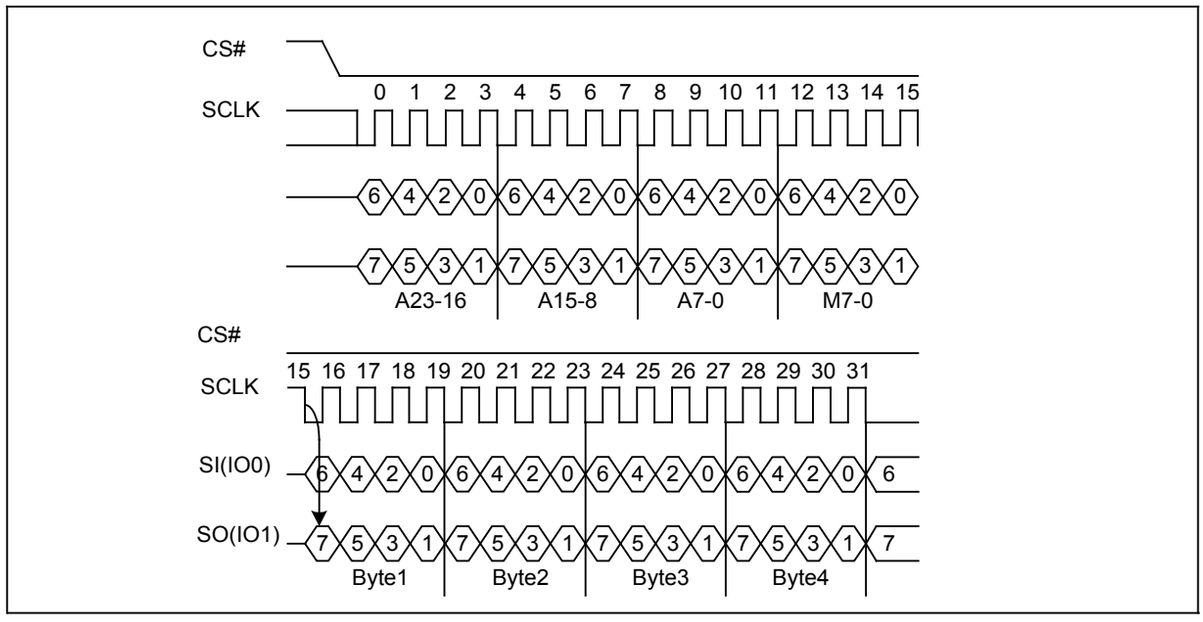


Figure 13. Dual I/O Fast Read Sequence Diagram (M7-0 = AXH)



7.12. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command. To ensure optimum performance the High Performance Mode (HPM) command (A3H) must be executed once, prior to the Quad I/O Fast Read command.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M7-0) =AXH, then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure15. If the "Continuous Read Mode" bits (M7-0) are any value other than AXH, the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure 14. Quad I/O Fast Read Sequence Diagram (M7-0 = 0XH or not AXH)

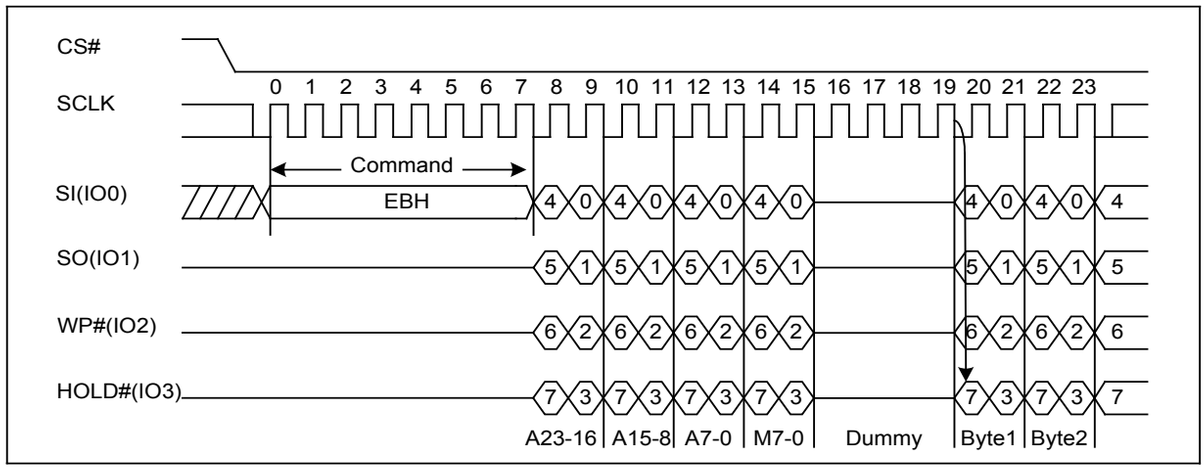
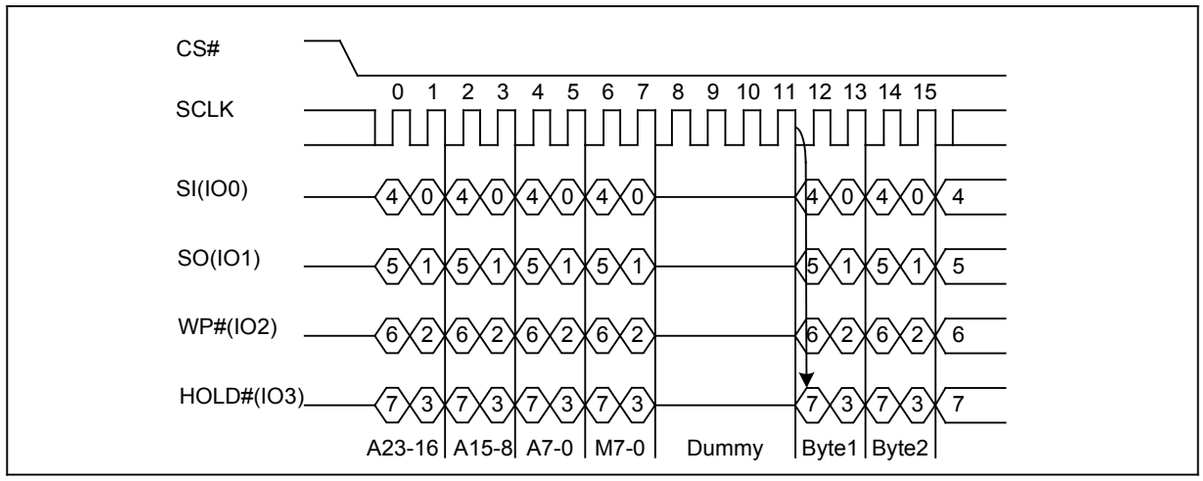


Figure 15. Quad I/O Fast Read Sequence Diagram (M7-0 = AXH)



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.13. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure16. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command. To ensure optimum performance the High Performance Mode (HPM) command (A3h) must be executed once, prior to the Quad I/O Word Fast Read command.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M7-0) =AXH, then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure17. If the "Continuous Read Mode" bits (M7-0) are any value other than AXH, the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure 16. Quad I/O Word Fast Read Sequence Diagram (M7-0 = 0XH or not AXH)

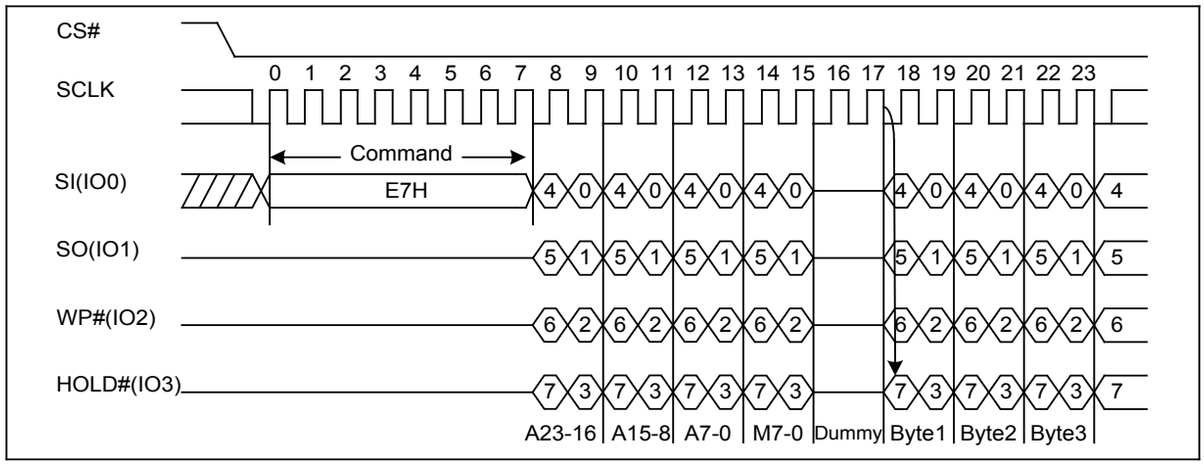
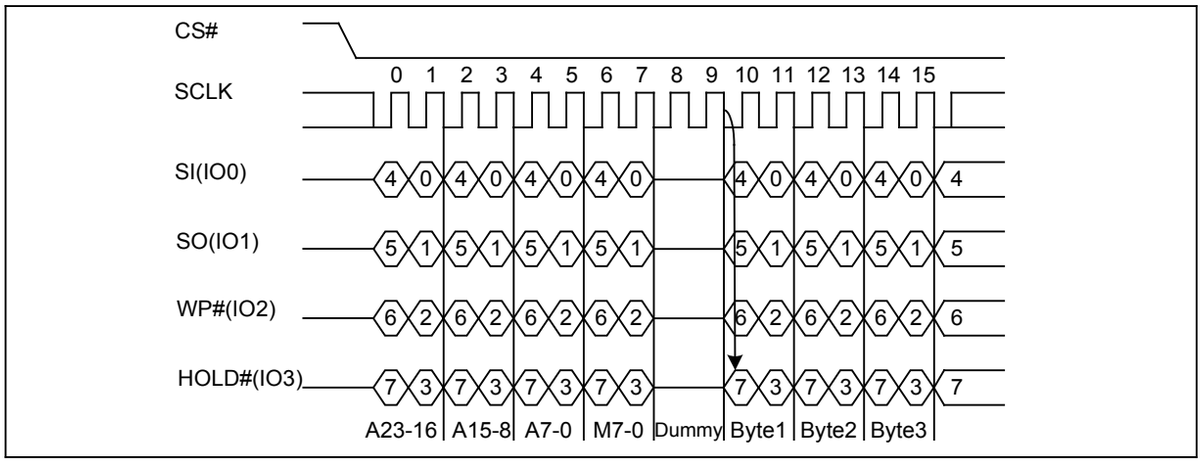


Figure 17. Quad I/O Word Fast Read Sequence Diagram (M7-0 = AXH)



Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to E7H. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following E7H commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

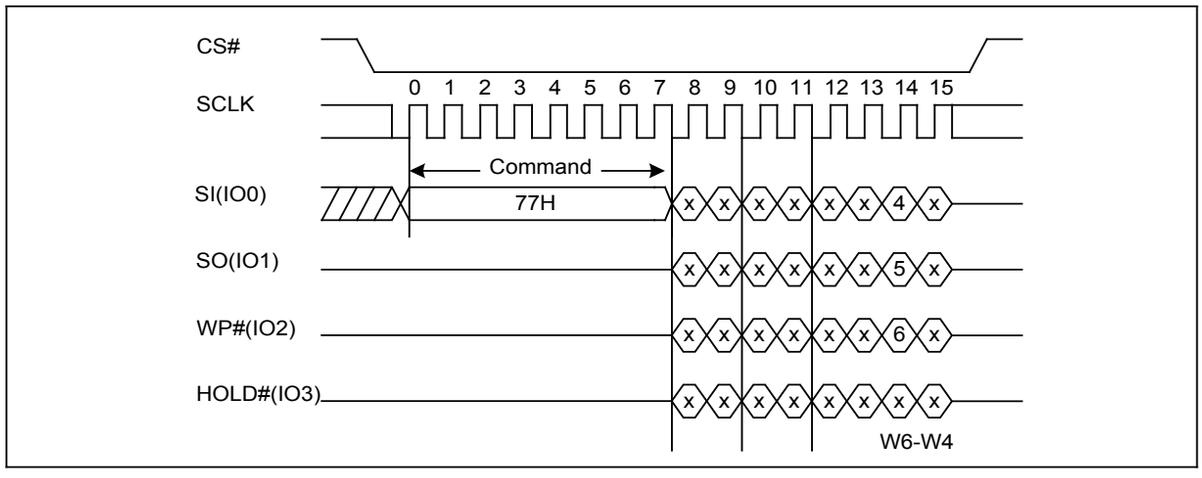
7.14. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

W6, W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 18. Set Burst with Wrap Sequence Diagram



7.15. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence.

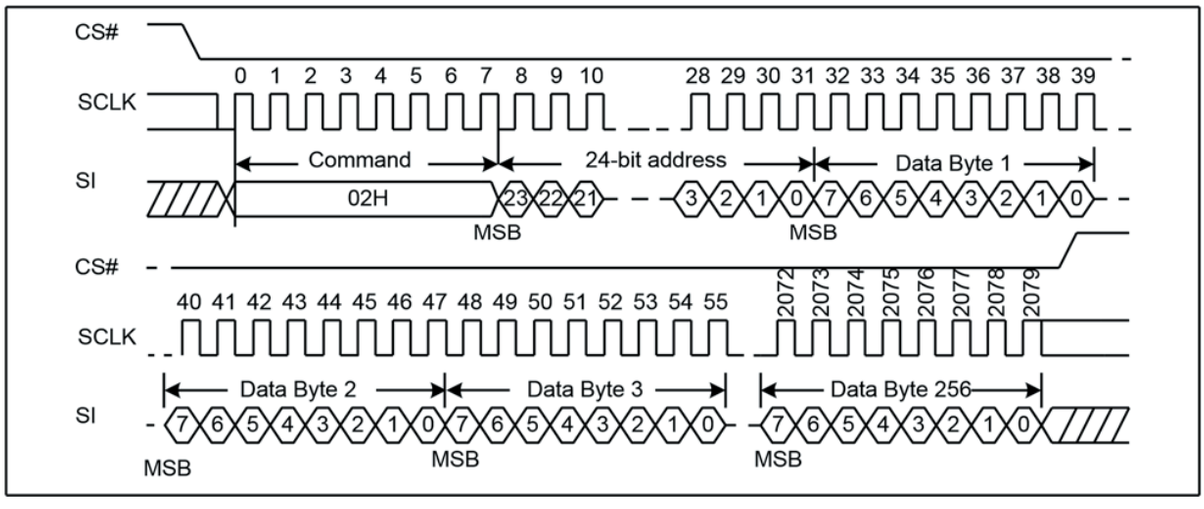
The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI→ CS# goes high. The command sequence is shown in Figure19.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure 19. Page Program Sequence Diagram



7.16. Quad Page Program (32H)

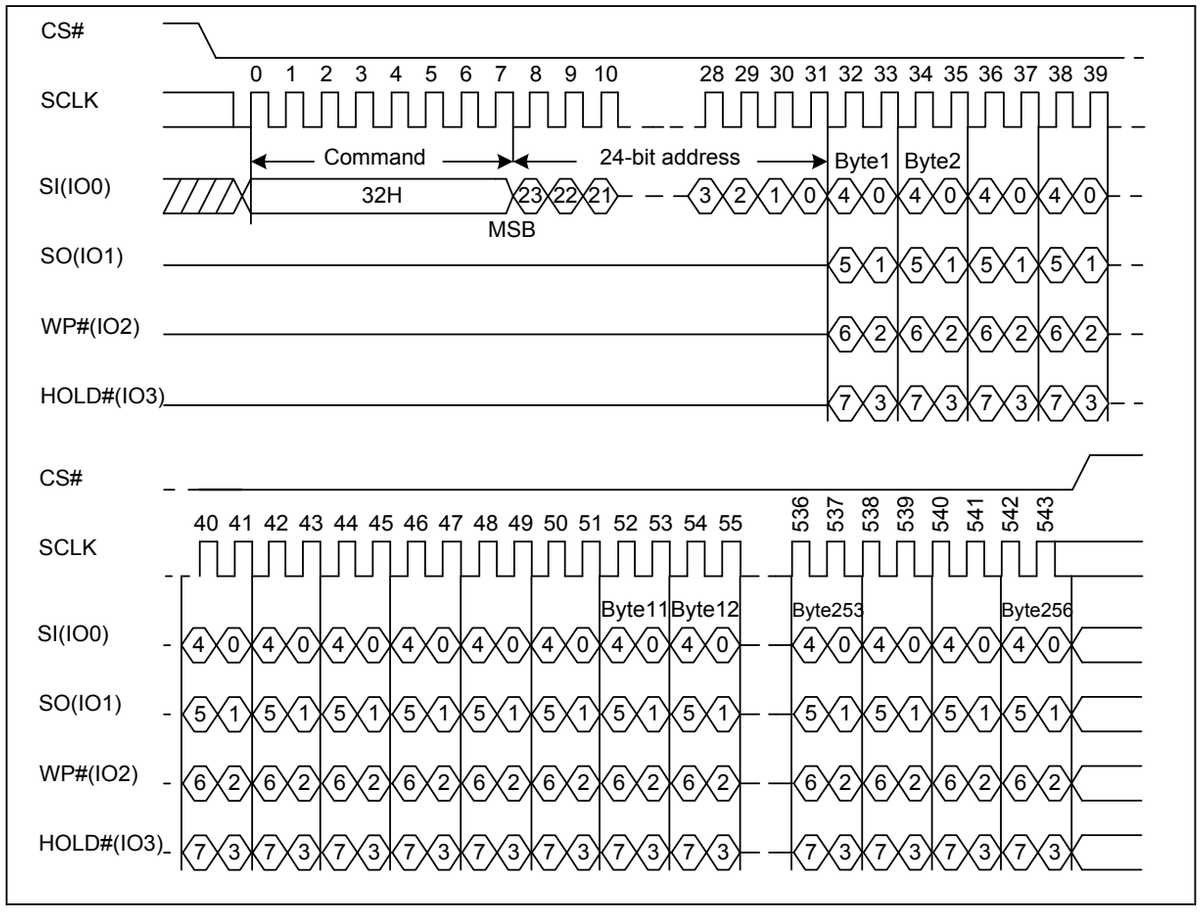
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure20. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 20. Quad Page Program Sequence Diagram

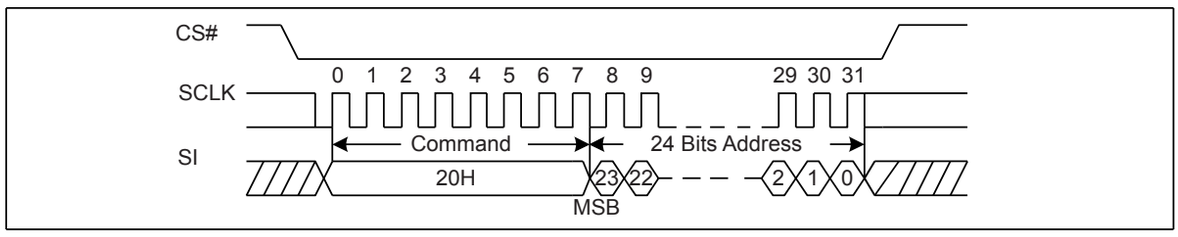


7.17. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure21. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table1.) is not executed.

Figure 21. Sector Erase Sequence Diagram

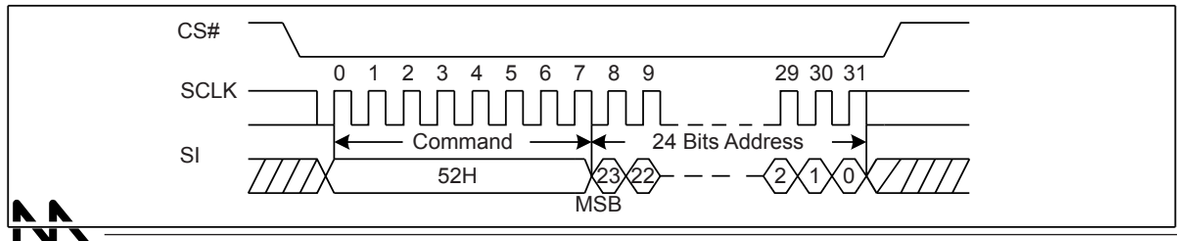


7.18. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI→ CS# goes high. The command sequence is shown in Figure22. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.) is not executed.

Figure 22. 32KB Block Erase Sequence Diagram

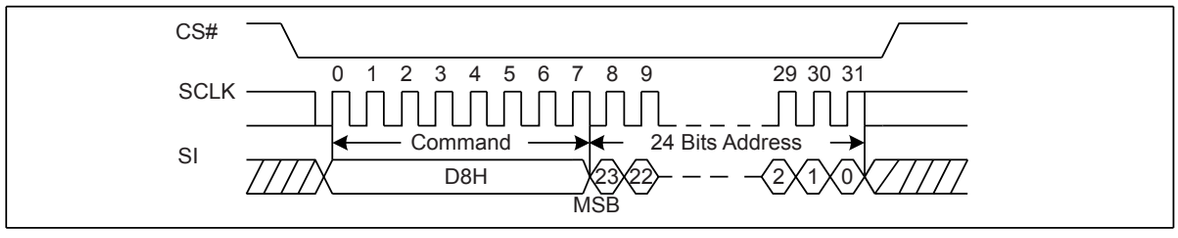


7.19. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure23. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.) is not executed.

Figure 23. 64KB Block Erase Sequence Diagram

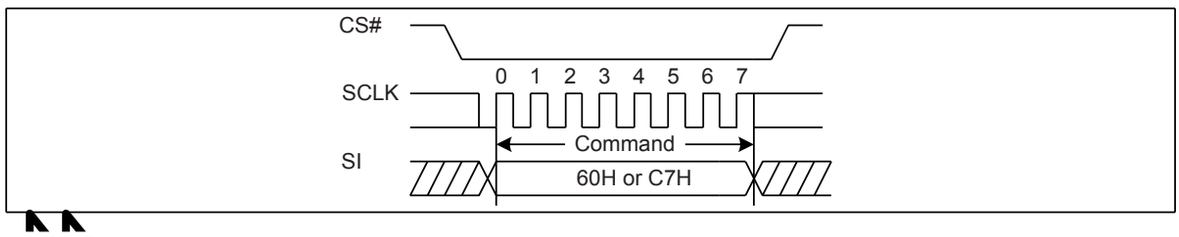


7.20. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure24. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP4,BP3,BP2, BP1, BP0) bits are set to “None protected”. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 24. Chip Erase Sequence Diagram



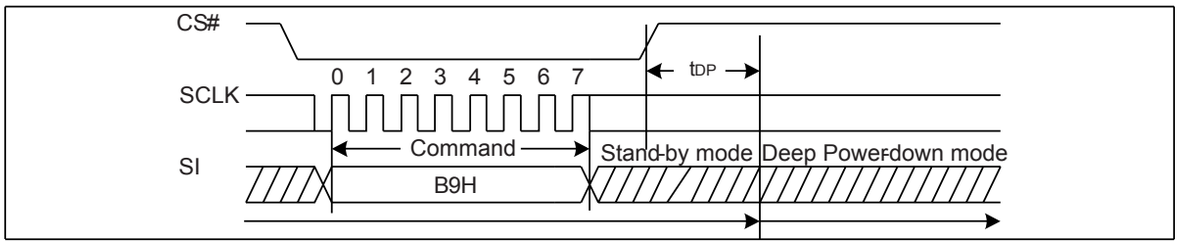
7.21. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure25. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 25. Deep Power-Down Sequence Diagram



7.22. Release from Deep Power-Down or High Performance Mode and Read Device ID (RDI) (ABH)

The Release from Power-Down or High Performance Mode/Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or High Performance Mode or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state or High Performance Mode, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure26. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure27. The Device ID value for the GD25Q21B is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 26. Release Power-Down Sequence or High Performance Mode Sequence Diagram

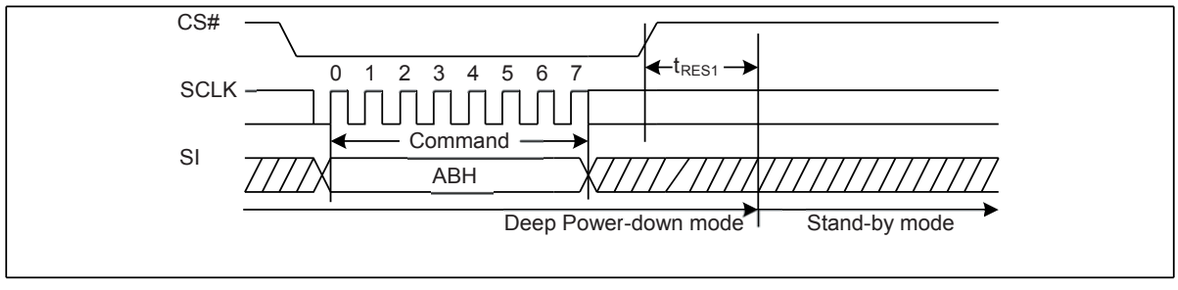
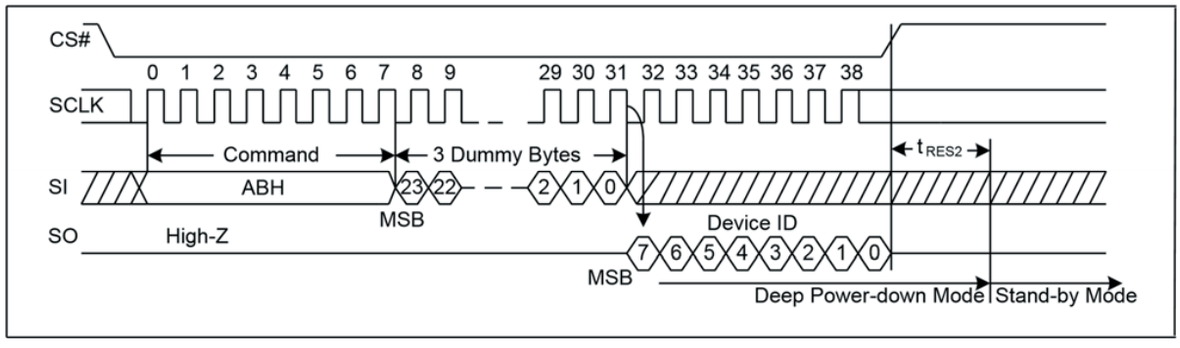


Figure 27. Release Power-Down and Read Device ID Sequence Diagram

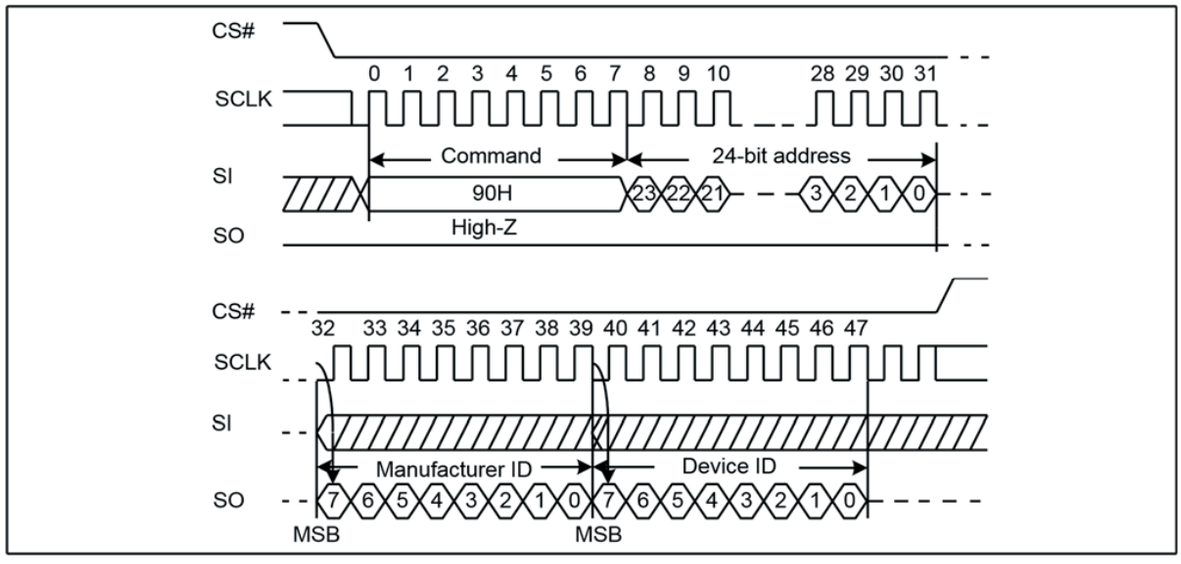


7.23. Read Manufacture ID/Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure28. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 28. Read Manufacture ID/Device ID Sequence Diagram

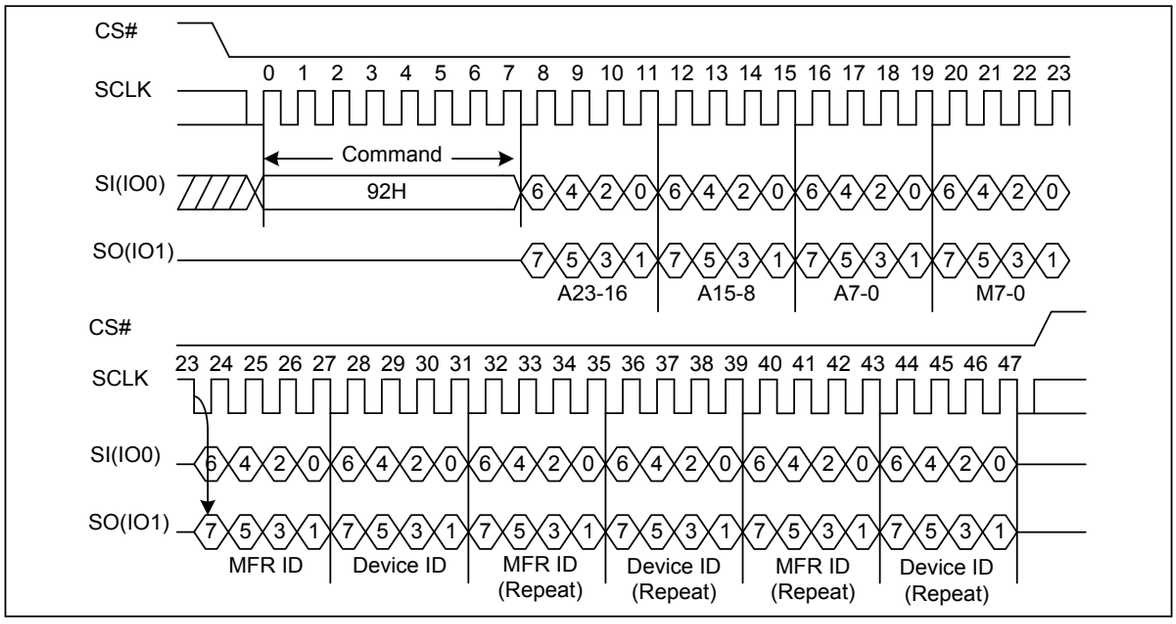


7.24. Read Manufacture ID/Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down/ Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code "92H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure29. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 29. Read Manufacture ID/Device ID Dual I/O Sequence Diagram

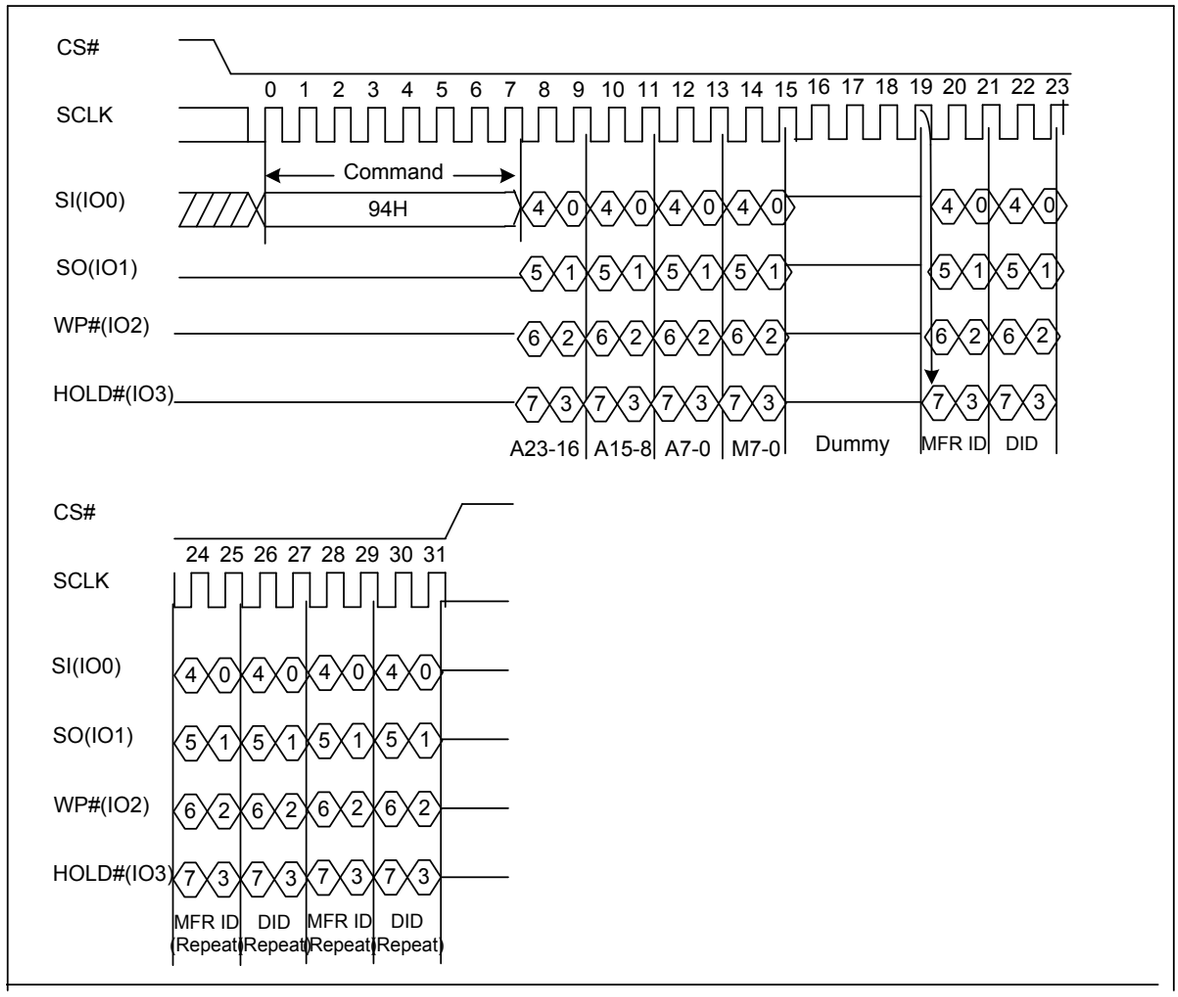


7.25. Read Manufacture ID/Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down/ Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code "94H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure30. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 30. Read Manufacture ID/Device ID Quad I/O Sequence Diagram

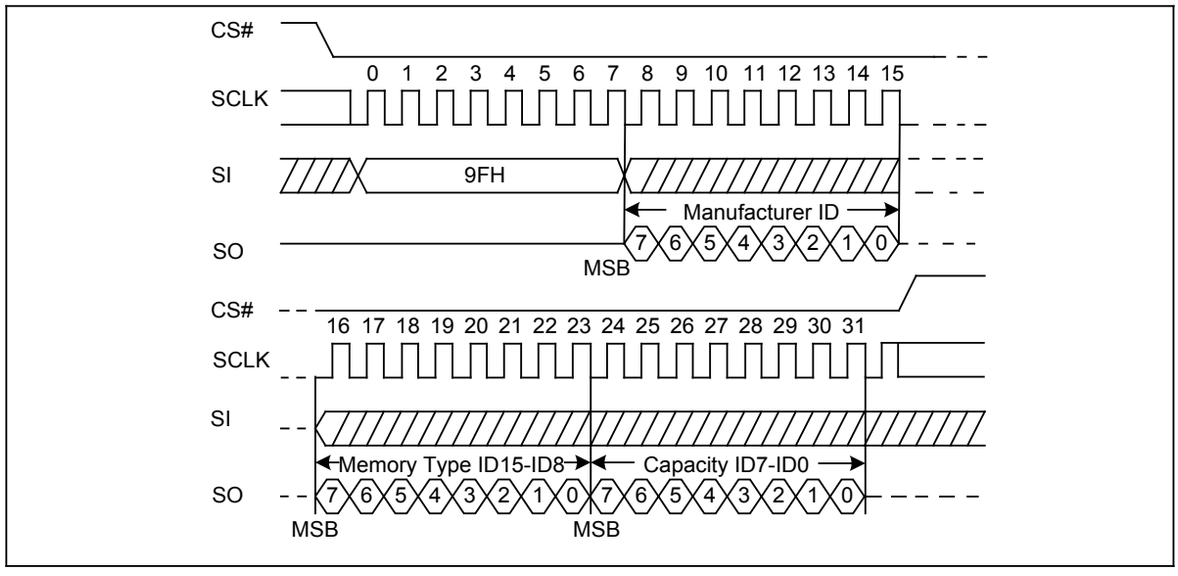


7.26. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure31. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

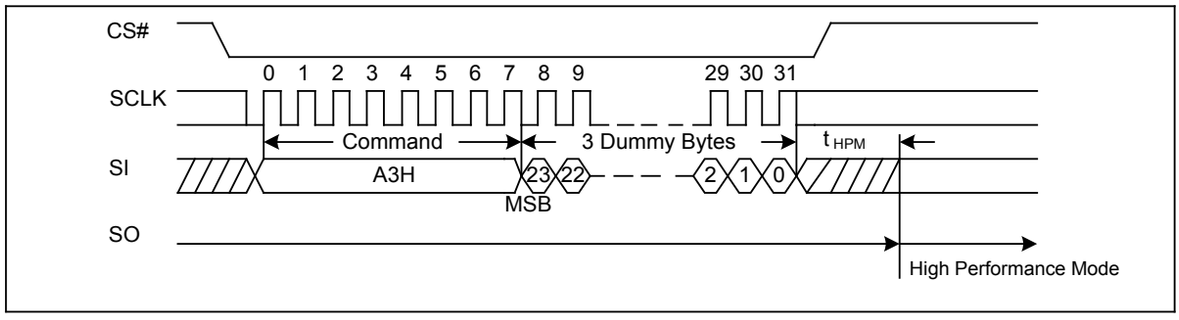
Figure 31. Read Identification ID Sequence Diagram



7.27. High Performance Mode (HPM) (A3H)

It is recommended to execute High Performance Mode (HPM) command prior to Dual or Quad I/O commands when operating at high frequencies (see f_C in AC Electrical Characteristics). This command allows pre-charging of internal charge pumps so the voltages required for accessing the flash memory array are readily available. The command sequence: CS# goes low → Sending A3H command → Sending 3-dummy byte → CS# goes high. See Figure32. After the HPM command is executed, the device will maintain a slightly higher standby current (Icc8) than standard SPI operation. The Release from Power-Down or HPM command (ABH) can be used to return to standard SPI standby current (Icc1). In addition, Power-Down command (B9H) will also release the device from HPM mode back to deep power down state.

Figure 32. High Performance Mode Sequence Diagram



7.28. Erase Security Registers (44H)

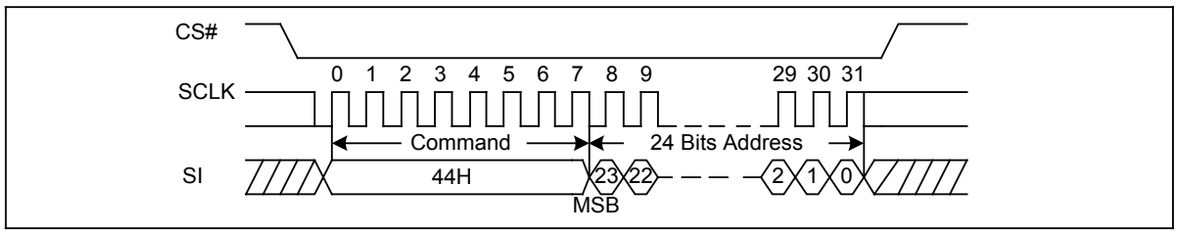
The GD25Q21B provides three 512-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0 0 0 1	0 0 0	Do not care
Security Register #2	00H	0 0 1 0	0 0 0	Do not care
Security Register #3	00H	0 0 1 1	0 0 0	Do not care

Figure 33. Erase Security Registers command Sequence Diagram



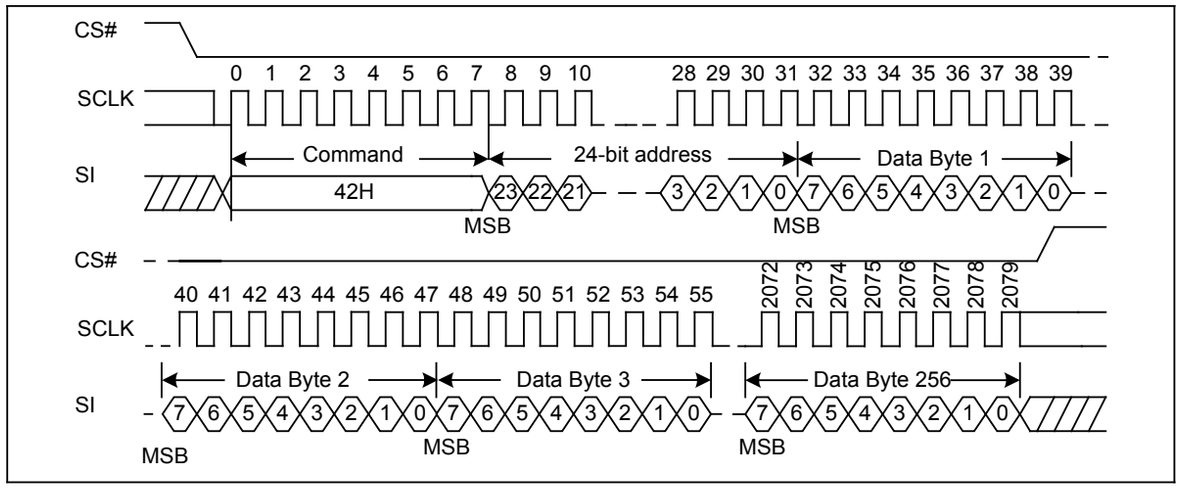
7.29. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 512 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0 0	Byte Address

Figure 34. Program Security Registers command Sequence Diagram

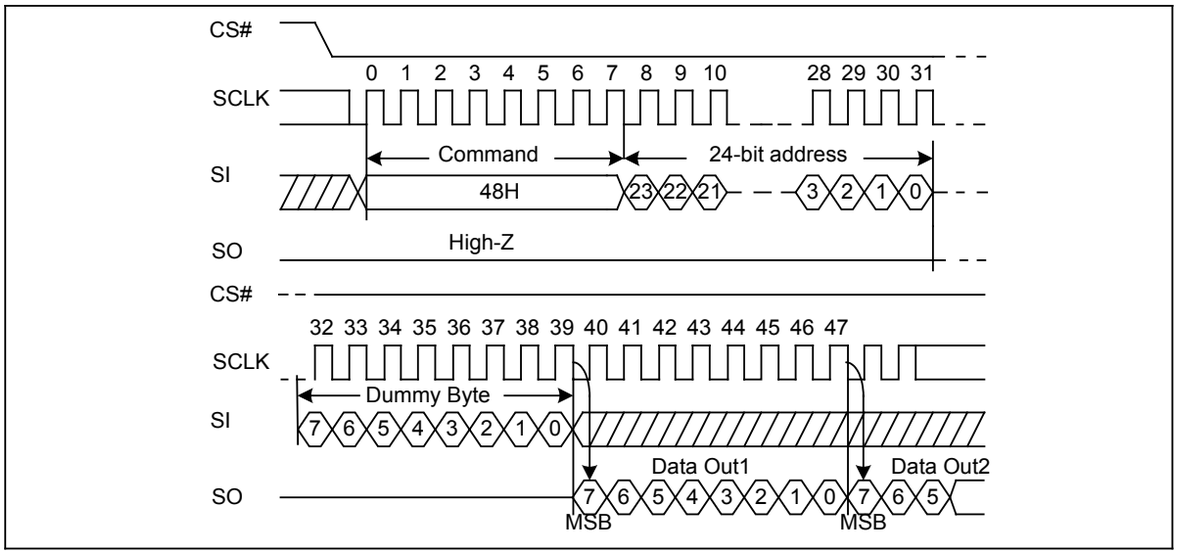


7.30. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A8-A0 address reaches the last byte of the register (Byte 1FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11-9	A8-0
Security Register #1	00H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0 0	Byte Address

Figure 35. Read Security Registers command Sequence Diagram

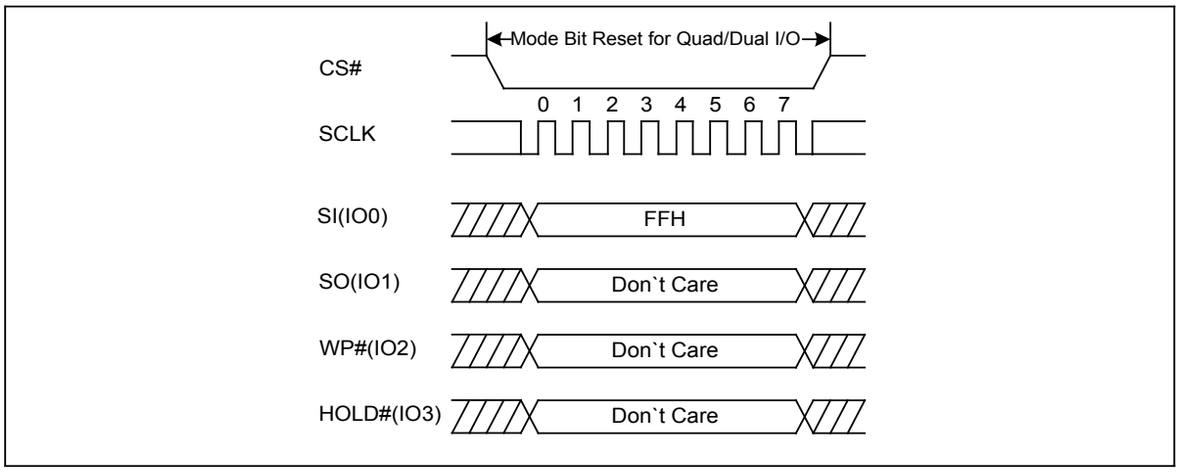


7.31. Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, "Continuous Read Mode" bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

If the system controller is reset during operation it will likely send a standard SPI command, such as Read ID (9FH) or Fast Read (0BH), to the device. Because the GD25Q21B has no hardware reset pin, so if Continuous Read Mode bits are set to "AXH", the GD25Q21B will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the "AXH" state and allow standard SPI command to be recognized. The command sequence is show below.

Figure 36. Continuous Read Mode Reset Sequence Diagram

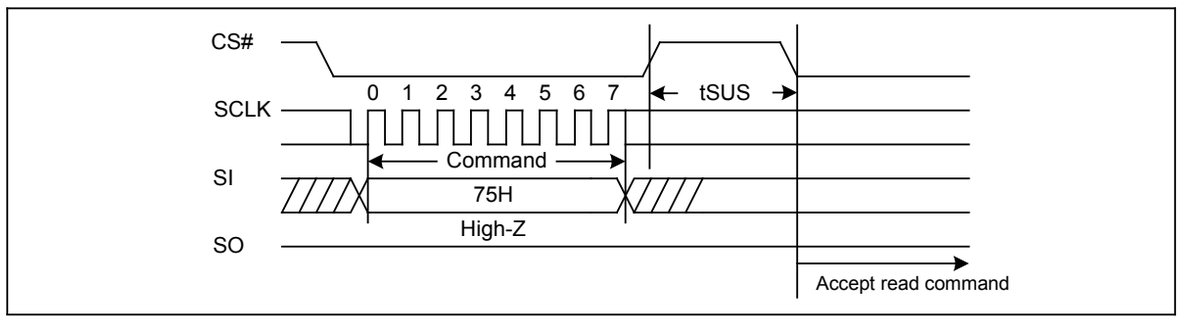


7.32. Program/Erase Suspend (PES) (75H)

The Erase/Program Suspend instruction "75H", allows the system to interrupt a sector/block erase or page program operation and then read data from any other sector or block. The Write Status Register command (01H), Page Program command (02H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during suspend. Erase/Program Suspend is valid only during the sector/block erase or page program operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation.

While the Erase/Program suspend cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Erase/Program suspend cycle and becomes a 0 when the cycle is finished and the device is ready to accept read command. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show below.

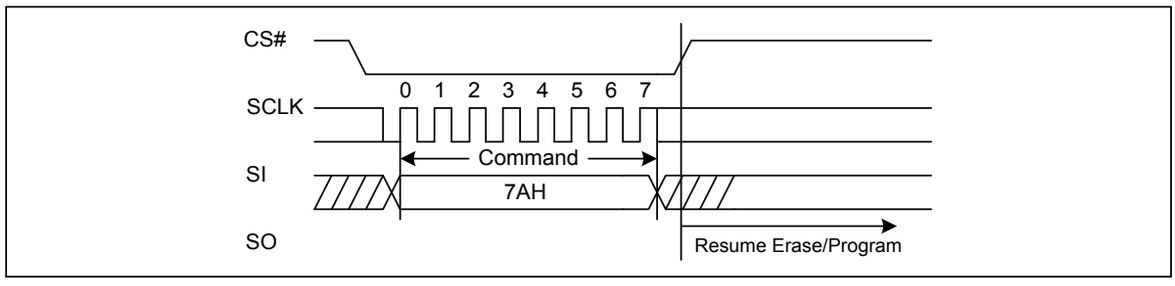
Figure 37. Program/Erase Suspend Sequence Diagram



7.33. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the sector/block erase or program operation after a Program/Erase Suspend command. After issued the BUSY bit in the status register will be set to 1 and the sector/block erase or program operation will completed. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show below.

Figure 38. Program/Erase Resume Sequence Diagram



8. ELECTRICAL CHARACTERISTICS

8.1. Power-On Timing

Figure 39. Power-on Timing Sequence Diagram

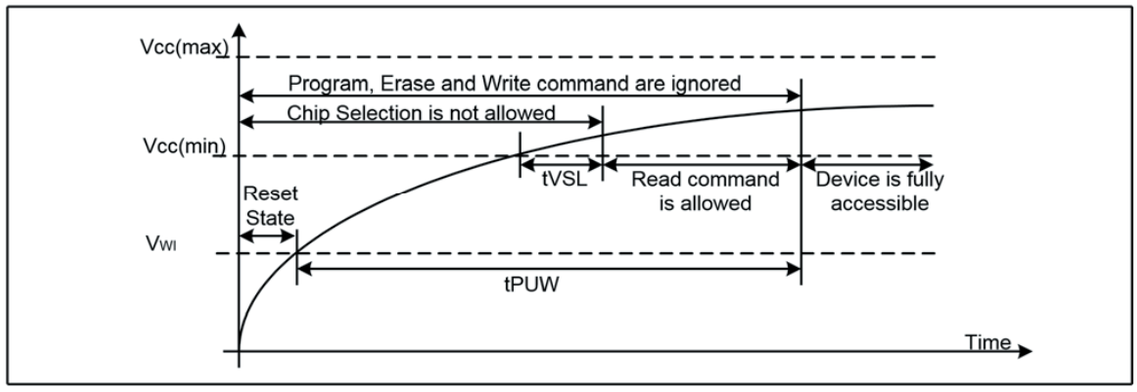


Table3. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Typ	Max	Unit
tVSL	VCC(min) To CS# Low	10			us
tPUW	Time Delay Before Write Instruction	1		10	ms
VWI	Write Inhibit Voltage	2.1	2.3	2.5	V

8.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

8.3. Data Retention and Endurance

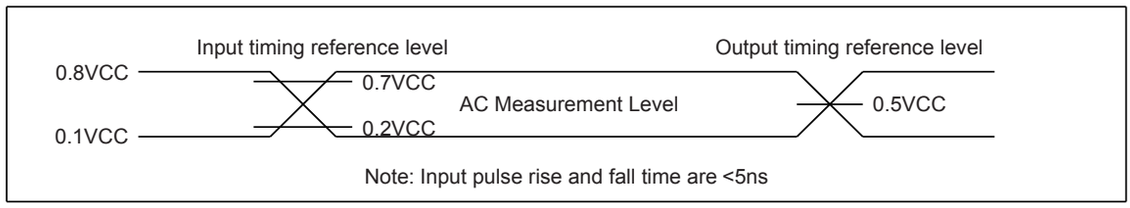
Parameter	Test Condition	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85°C	100K	Cycles

8.4. Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.5. Absolute Maximum Ratings

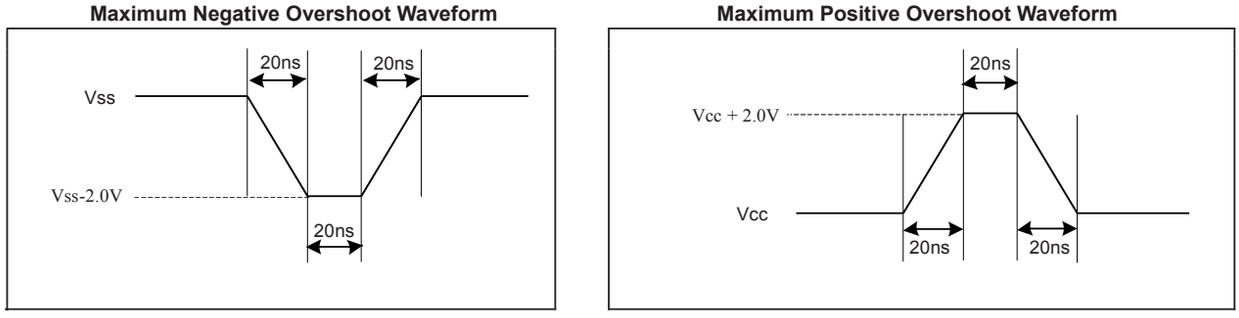
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V



8.6. Capacitance Measurement Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 40. Input Test Waveform and Measurement Level



8.7. DC Characteristics

(T= -40°C~85°C, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		20	30	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)			15	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)			12	mA
		CLK=0.1VCC/0.9VCC at 33MHz, Q=Open(*1,*2,*4 I/O)			6	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		10	15	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		8	12	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		10	15	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		10	15	mA
I_{CC8}	Operating Current (CE)			10	15	mA
I_{CC9}	High Performance Current			400	600	μA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL}=1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}=-100μA	VCC-0.2			V

8.8. AC Characteristics

(T= -40°C~85°C, VCC=2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency For: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR, RDSR, RDID (*1,*2,*4 I/O)	DC.		104	MHz
f_R	Serial Clock Frequency For: Read	DC.		80	MHz
t_{CLH}	Serial Clock High Time	3.5			ns
t_{CLL}	Serial Clock Low Time	3.5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	5			ns
t_{HLCH}	Hold# Low Setup Time (Relative to Clock)	3.5			ns
t_{HHCH}	Hold# High Setup Time (Relative to Clock)	3.5			ns
t_{CHHL}	Hold# High Hold Time (Relative to Clock)	3.5			ns
t_{CHHH}	Hold# Low Hold Time (Relative to Clock)	3.5			ns
t_{HLQZ}	Hold# Low To High-Z Output			6	ns
t_{HHQX}	Hold# Low To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	µs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			5	µs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			5	µs
t_{HPM}	CS# High To High Performance Mode			0.2	µs
t_{SUS}	CS# High To Next Command After Suspend			20	µs
t_W	Write Status Register Cycle Time		10	30	ms
t_{PP}	Page Programming Time		0.35	2.4	ms
t_{SE}	Sector Erase Time		50	200/400(1)	ms
t_{BE}	Block Erase Time(32K/64K)		0.18/0.25	0.6/0.8	s
t_{CE}	Chip Erase Time		0.8	1.5	s

Note:

(1). Max Value t_{SE} with <50K cycles is 200 ms and >50K & <100K cycles is 400 ms.

Figure41. Serial Input Timing

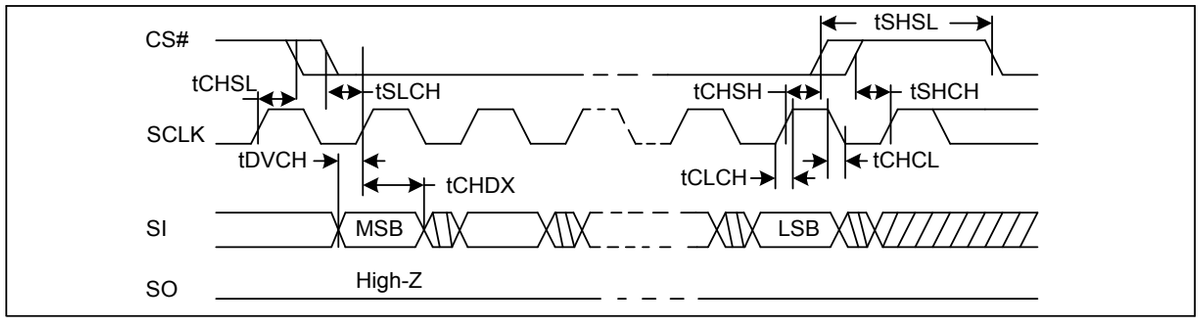


Figure42. Output Timing

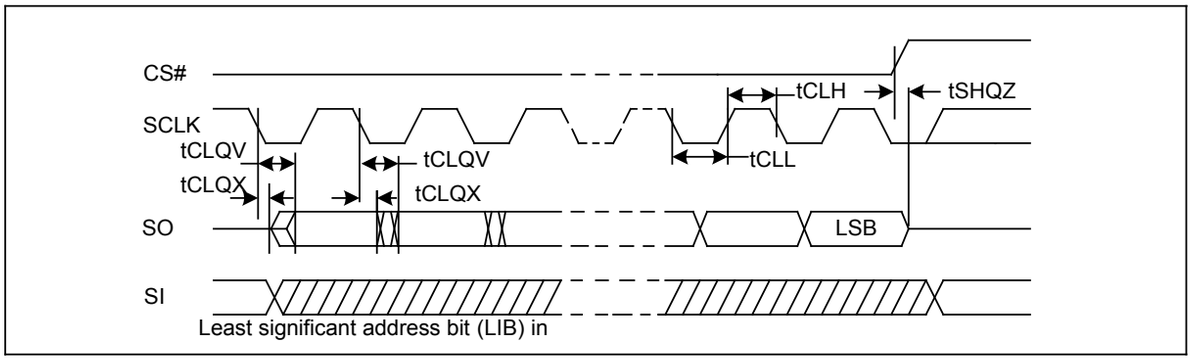
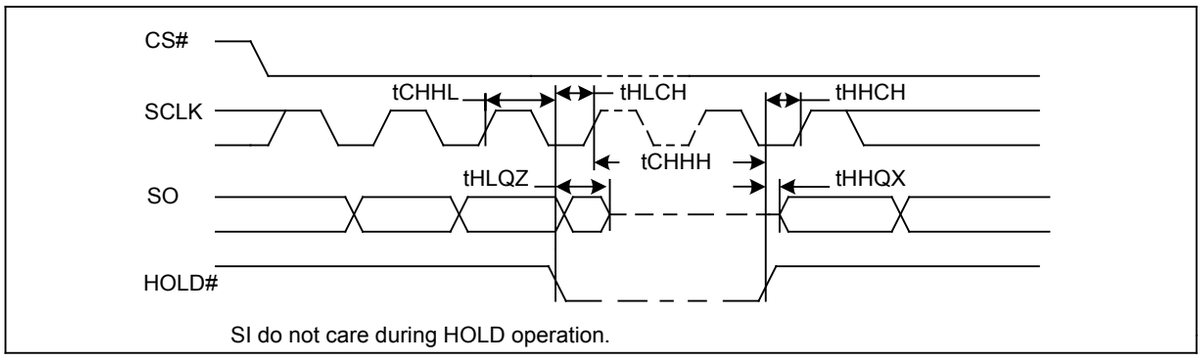
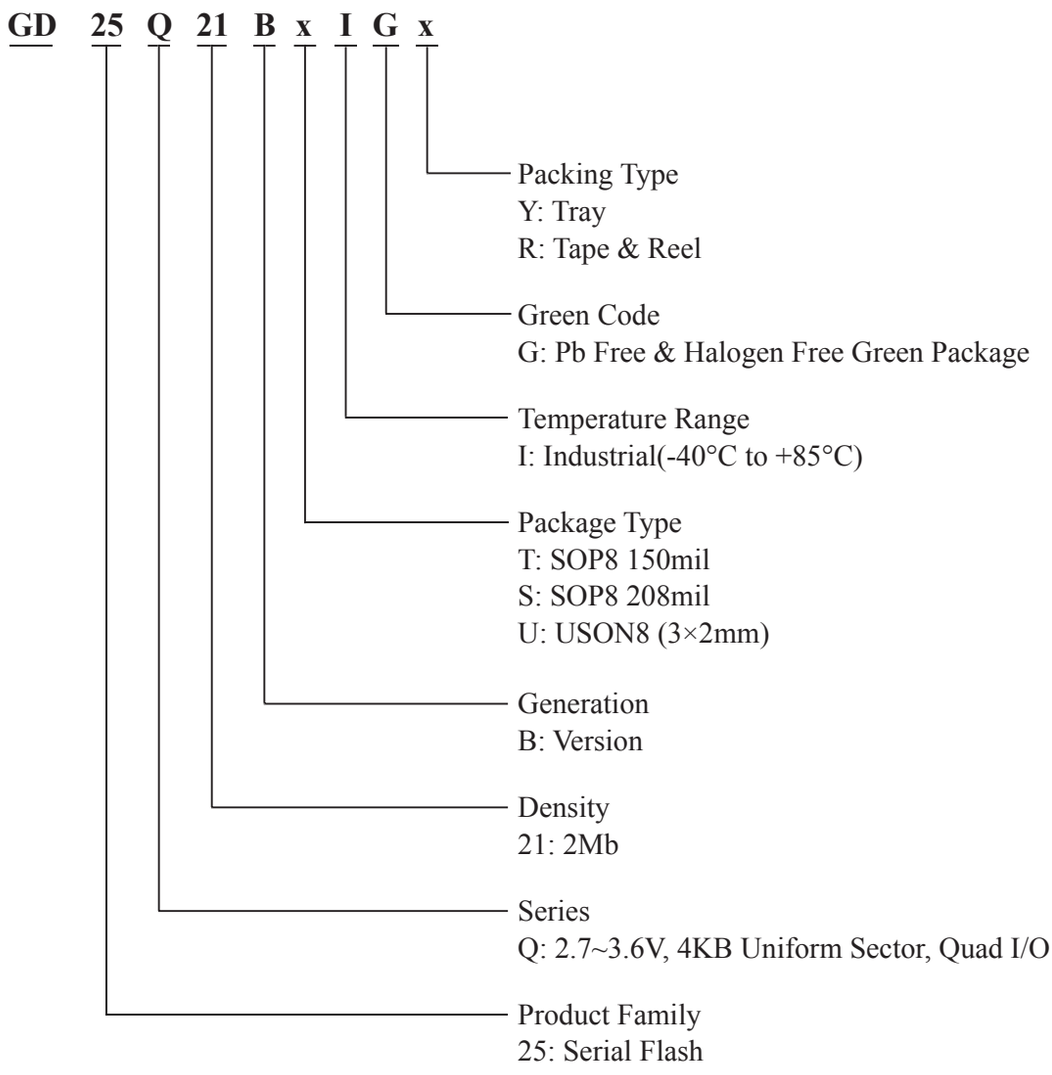


Figure43. Hold Timing

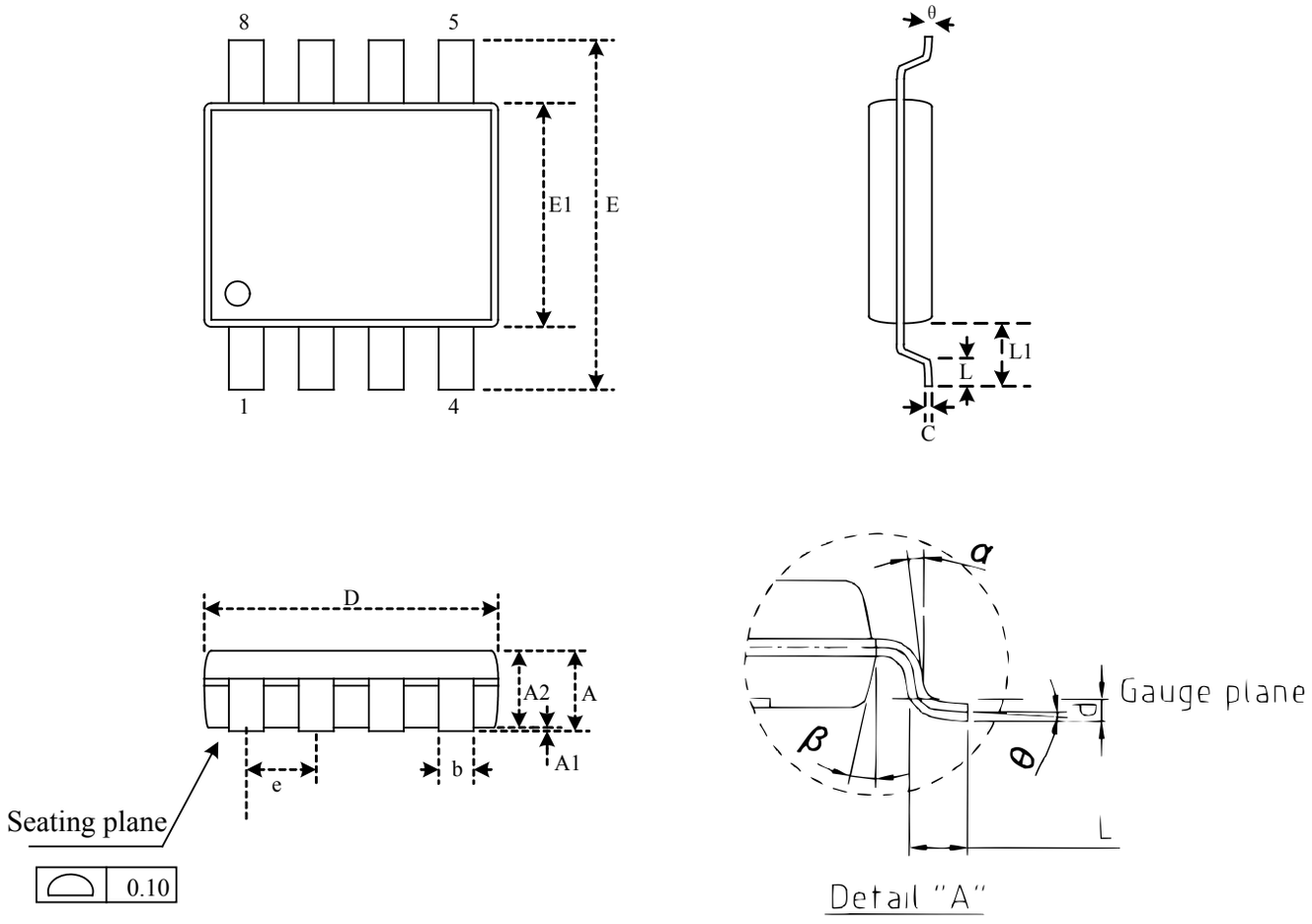


9. ORDERING INFORMATION



10. PACKAGE INFORMATION

10.1 Package SOP8 150MIL

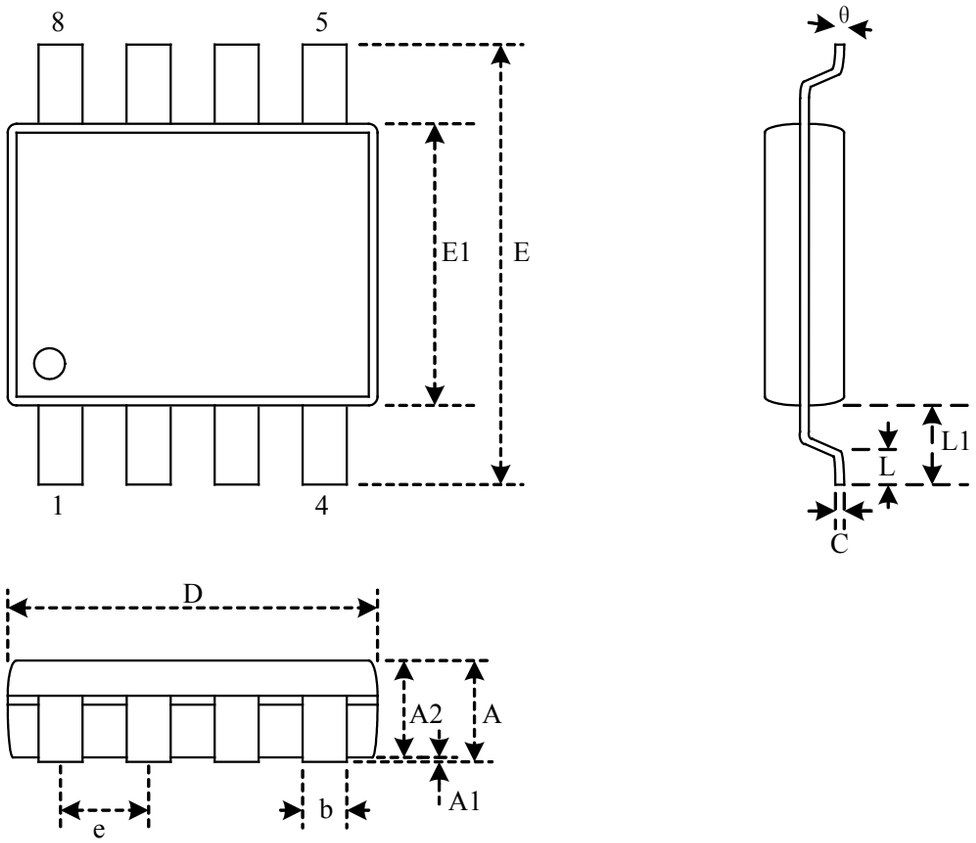


Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	θ	α	ß
mm	Min	1.35	0.05	1.35	0.31	0.15	4.77	5.80	3.80	-	0.40	0.85	0°	6°	11°
	Nom	-	-	-	-	-	4.90	6.00	3.90	1.27	-	1.06	-	7°	12°
	Max	1.75	0.25	1.55	0.51	0.25	5.03	6.20	4.00	-	0.90	1.27	8°	8°	13°
Inch	Min	0.053	0.002	0.053	0.012	0.006	0.188	0.228	0.149	-	0.016	0.033	0°	6°	11°
	Nom	-	-	-	0.016	-	0.193	0.236	0.154	0.050	0	0.042	-	7°	12°
	Max	0.069	0.010	0.061	0.020	0.010	0.198	0.244	0.158	-	0.035	0.050	8°	8°	13°

Note: Both package length and width do not include mold flash.

10.2 Package SOP8 208MIL

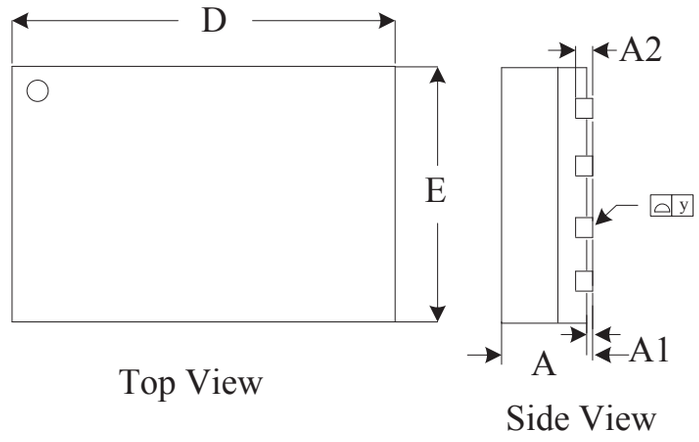


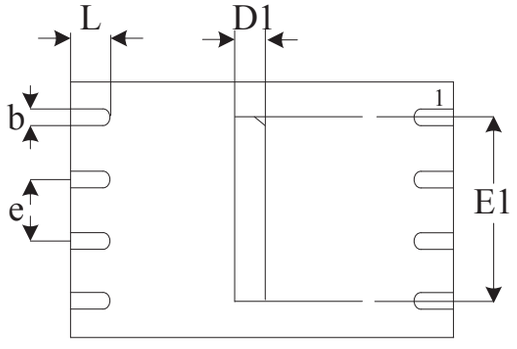
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	1.70	0.31	0.18	5.13	7.70	5.18	-	0.50	1.21	0°
	Nom	-	0.15	1.80	0.41	0.21	5.23	7.90	5.28	1.27	0.67	1.31	5°
	Max	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38	-	0.85	1.41	8°
Inch	Min	-	0.002	0.067	0.012	0.007	0.202	0.303	0.204	-	0.020	0.048	0°
	Nom	-	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	5°
	Max	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212	-	0.033	0.056	8°

Note: Both package length and width do not include mold flash.

10.3 Package USON8 (3×2mm)





Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.50	-	0.13	0.18	2.90	0.15	1.90	1.50	-	0.00	0.30
	Nom	0.55	-	0.15	0.25	3.00	0.20	2.00	1.60	0.50	-	0.35
	Max	0.60	0.05	0.18	0.30	3.10	0.30	2.10	1.70	-	0.05	0.45
Inch	Min	0.020	-	0.005	0.007	0.114	0.006	0.075	0.059	-	0.000	0.012
	Nom	0.022	-	0.006	0.010	0.118	0.008	0.079	0.063	0.020	-	0.014
	Max	0.024	0.002	0.007	0.012	0.122	0.012	0.083	0.067	-	0.002	0.018

Note: Both package length and width do not include mold flash.