RoboClockII™ Junior, CY7B9930V, CY7B9940V

High Speed Multifrequency PLL Clock Buffer

Features

- 12–100 MHz (CY7B9930V), or 24–200 MHz (CY7B9940V) input/output operation
- Matched pair output skew < 200 ps
- Zero input-to-output delay
- 10 LVTTL 50% duty-cycle outputs capable of driving 50Ω terminated lines
- Commercial temperature range with eight outputs at 200 MHz
- Industrial temperature range with eight outputs at 200 MHz
- 3.3V LVTTL/LV differential (LVPECL), fault-tolerant and hot insertable reference inputs
- Multiply ratios of (1–6, 8, 10, 12)
- Operation up to 12x input frequency
- Individual output bank disable for aggressive power management and EMI reduction
- Output high impedance option for testing purposes
- Fully integrated PLL with lock indicator
- Low cycle-to-cycle jitter (<100 ps peak-peak)
- Single 3.3V ± 10% supply
- 44-pin TQFP package

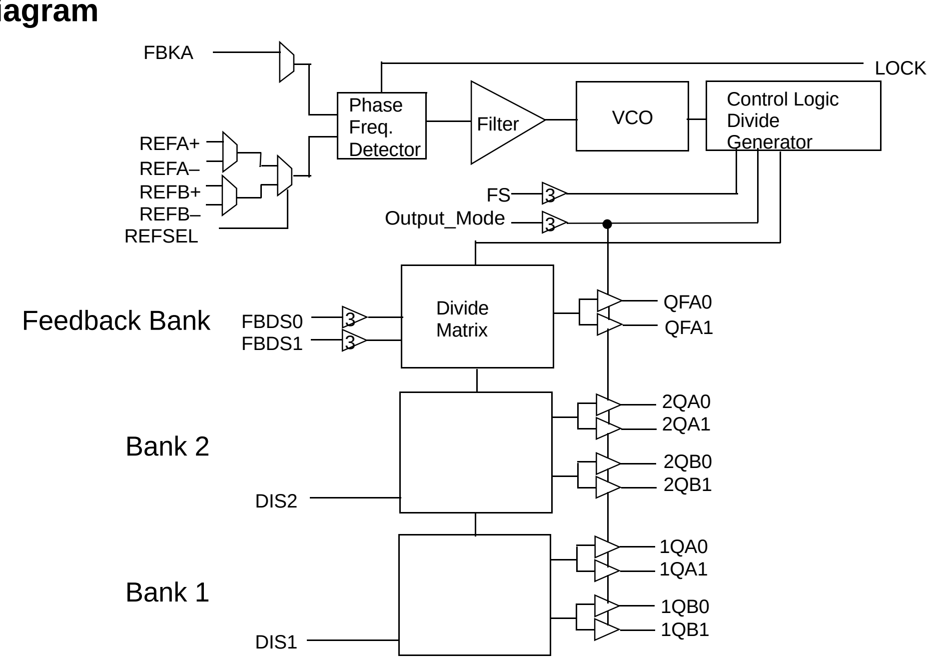
Functional Description

The CY7B9930V and CY7B9940V High-Speed Multifrequency PLL Clock Buffers offer user-selectable control over system clock functions. This multiple output clock driver provides the system integrator with functions necessary to optimize the timing of high performance computer or communication systems.

Ten configurable outputs can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews at LVTTL levels. The outputs are arranged in three banks. The FB feedback bank consists of two outputs, which allows divide-by functionality from 1 to 12. Any one of these ten outputs can be connected to the feedback input as well as driving other inputs.

Selectable reference input is a fault tolerance feature that allows smooth change over to secondary clock source, when the primary clock source is not in operation. The reference inputs are configurable to accommodate both LVTTL or differential (LVPECL) inputs. The completely integrated PLL reduces jitter and simplifies board layout.

Logic Block Diagram



Contents

Logic Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept signals from the REF inputs (REFA+, REFA–, REFB+ or REFB–) and the FB input (FBKA). Correction information is then generated to control the frequency of the Voltage Controlled Oscillator (VCO). These two blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

The RoboClockII™ Junior has a flexible REF input scheme. These inputs allow the use of either differential LVPECL or single ended LVTTL inputs. To configure as single ended LVTTL inputs, leave the complementary pin to 1.5V), then use the other input pin as an LVTTL input. The REF inputs are also tolerant to hot insertion.

The REF inputs can be changed dynamically. When changing from one reference input to the other reference input of the same frequency, the PLL is optimized to ensure that the clock outputs period is not less than the calculated system budget (t_{MIN} = t_{REF} (nominal reference clock period) – t_{CCJ} (cycle-to-cycle jitter) – t_{PDEV} (max. period deviation)) while reacquiring lock.

VCO, Control Logic, and Divide Generator

The VCO accepts analog control inputs from the PLL filter block. The FS control pin setting determines the nominal operational frequency range of the divide by one output (f_{NOM}) of the device. f_{NOM} is directly related to the VCO frequency. There are two versions of the RoboClockII Junior, a low speed device (CY7B9930V) where f_{NOM} ranges from 12 MHz to 100 MHz, and a high speed device (CY7B9940V), which ranges from 24 MHz to 200 MHz. The FS setting for each device is shown in Table 1. The f_{NOM} frequency is seen on “divide-by-one” outputs.

Table 1. Frequency Range Select

FS[1]	CY7B9930V		CY7B9940V	
	f_{NOM} (MHz)		f_{NOM} (MHz)	
	Min.	Max.	Min.	Max.
LOW	12	26	24	52
MID	24	52	48	100
HIGH	48	100	96	200[2]

Divide Matrix

The Divide Matrix is comprised of three independent banks: two banks of clock outputs and one bank for feedback. Each clock output bank has two pairs of low-skew, high fanout output buffers ([1:2]Q[A:B][0:1]), and an output disable (DIS[1:2]).

The feedback bank has one pair of low-skew, high fanout output buffers (QFA[0:1]). One of these outputs may connect to the selected feedback input (FBKA+). This feedback bank also has two divider function selects FBDS[0:1].

The divide capabilities for each bank are shown in Table 2.

Table 2. Output Divider Function

Function Selects		Output Divider Function		
FBDS1	FBDS0	Bank 1	Bank 2	Feedback Bank
LOW	LOW	/1	/1	/1
LOW	MID	/1	/1	/2
LOW	HIGH	/1	/1	/3
MID	LOW	/1	/1	/4
MID	MID	/1	/1	/5
MID	HIGH	/1	/1	/6
HIGH	LOW	/1	/1	/8
HIGH	MID	/1	/1	/10
HIGH	HIGH	/1	/1	/12

Output Disable Description

The outputs of Bank 1 and Bank 2 can be independently put into a HOLD OFF or high impedance state. The combination of the Output_Mode and DIS[1:2] inputs determines the clock outputs' state for each bank. When the DIS[1:2] is LOW, the outputs of the corresponding bank are enabled. When the DIS[1:2] is HIGH, the outputs for that bank are disabled to a high impedance (HI-Z) or HOLD OFF state depending on the Output_Mode input. Table 3 defines the disabled output functions.

The HOLD OFF state is designed as a power saving feature. An output bank is disabled to the HOLD OFF state in a maximum of six output clock cycles from the time when the disable input (DIS[1:2]) is HIGH. When disabled to the HOLD OFF state, outputs are driven to a logic LOW state on its falling edge. This ensures the output clocks are stopped without glitch. When a bank of outputs is disabled to HI-Z state, the respective bank of outputs go HI-Z immediately.

Table 3. DIS[1:2] Pin Functionality

OUTPUT_MODE	DIS[1:2]/FBDIS	Output Mode
HIGH/LOW	LOW	ENABLED
HIGH	HIGH	HI-Z
LOW	HIGH	HOLD-OFF
MID	X	FACTORY TEST

Notes
1. The level to be set on FS is determined by the “nominal” operating frequency (f_{NOM}) of the V_{CO}. f_{NOM} always appears on an output when the output is operating in the undivided mode. The REF and FB are at f_{NOM} when the output connected to FB is undivided.
2. The maximum output frequency is 200 MHz.

Lock Detect Output Description

The LOCK detect output indicates the lock condition of the integrated PLL. Lock detection is accomplished by comparing the phase difference between the reference and feedback inputs. Phase error is declared when the phase difference between the two inputs is greater than the specified device propagation delay limit (t_{PD}).

When in the locked state, after four or more consecutive feedback clock cycles with phase errors, the LOCK output is forced LOW to indicate out-of-lock state.

When in the out-of-lock state, 32 consecutive phase errorless feedback clock cycles are required to allow the LOCK output to indicate lock condition (LOCK = HIGH).

If the feedback clock is removed after LOCK has gone HIGH, a Watchdog circuit is implemented to indicate the out-of-lock condition after a timeout period by deasserting LOCK LOW. This timeout period is based upon a divided down reference clock.

This assumes that there is activity on the selected REF input. If there is no activity on the selected REF input then the LOCK detect pin may not accurately reflect the state of the internal PLL.

Factory Test Mode Description

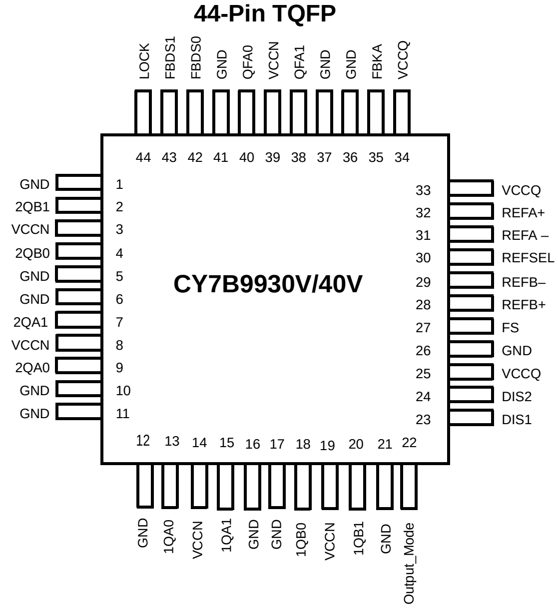
The device enters factory test mode when the OUTPUT_MODE is driven to MID. In factory test mode, the device operates with its internal PLL disconnected; the input level supplied to the reference input is used in place of the PLL output. In TEST mode the selected FB input must be tied LOW. All functions of the device remain operational in factory test mode except the internal PLL and output bank disables. The OUTPUT_MODE input is designed as a static input. Dynamically toggling this input from LOW to HIGH may temporarily cause the device to go into factory test mode (when passing through the MID state).

Factory Test Reset

When in factory test mode (OUTPUT_MODE = MID), the device is reset to a deterministic state by driving the DIS2 input HIGH. When the DIS2 input is driven HIGH in factory test mode, all clock outputs go to HI-Z; after the selected reference clock pin has five positive transitions, all the internal finite state machines (FSM) are set to a deterministic state. The deterministic state of the state machines depends on the configurations of the divide selects and frequency select input. All clock outputs stay in high impedance mode and all FSMs stay in the deterministic state until DIS2 is deasserted. When DIS2 is deasserted (with OUTPUT_MODE still at MID), the device reenters factory test mode.

Pin Configuration

Figure 1. 44-pin TQFP pinout



Pin Definitions

Name	I/O	Type	Description
FBKA	Input	LVTTL	**Feedback Input**.
REFA+, REFA– REFB+, REFB–	Input	LVTTL/ LVDIFF	**Reference Inputs**: These inputs operate as either differential PECL or single ended TTL reference inputs to the PLL. When operating as a single ended LVTTL input, leave the complementary input must be left open.
REFSEL	Input	LVTTL	**Reference Select Input**: The REFSEL input controls reference input configuration. When LOW, it uses the REFA pair as the reference input. When HIGH, it uses the REFB pair as the reference input. This input has an internal pull down.
FS[3]	Input	3 Level Input	**Frequency Select**: Set this input according to the nominal frequency (f_{NOM}). See Table 1.
FBDS[0:1][3]	Input	3 Level Input	**Feedback Divider Function Select**. These inputs determine the function of the QFA0 and QFA1 outputs. See Table 2.
DIS[1:2]	Input	LVTTL	**Output Disable**: Each input controls the state of the respective output bank. When HIGH, the output bank is disabled to the “HOLD OFF” or “HI-Z” state; the disable state is determined by OUTPUT_MODE. When LOW, the [1:4]Q[A:B][0:1] is enabled. See Table 3. These inputs each have an internal pull down.
LOCK	Output	LVTTL	**PLL Lock Indicator**: When HIGH, this output indicates that the internal PLL is locked to the reference signal. When LOW, the PLL is attempting to acquire lock.
Output_Mode[3]	Input	3 Level Input	**Output Mode**: This pin determines the clock outputs’ disable state. When this input is HIGH, the clock outputs disable to high impedance (HI-Z). When this input is LOW, the clock outputs disables to “HOLD OFF” mode. When in MID, the device enters factory test mode.
QFA[0:1]	Output	LVTTL	**Clock Feedback Output**: This pair of clock outputs connects to the FB input. These outputs have numerous divide options. The function is determined by the setting of the FBDS[0:1] pins.
[1:2]Q[A:B][0:1]	Output	LVTTL	**Clock Output**.
VCCN		PWR	**Output Buffer Power**: Power supply for each output pair.
VCCQ		PWR	**Internal Power**: Power supply for the internal circuitry.
GND		PWR	**Device Ground**.

Note
3. For all tri-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.

Absolute Maximum Conditions

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ....–40°C to +125°C

Ambient Temperature with power applied ....–40°C to +125°C

Supply voltage to ground potential ....–0.5V to +4.6V

DC input voltage .... –0.3V to V_{CC}+0.5V

Output current into outputs (LOW) ....40 mA

Static discharge voltage
(MIL-STD-883, Method 3015) .... >2000 V

Latch up current .... >±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ±10%
Industrial	–40 °C to +85 °C	3.3 V ±10%

Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions	Min	Max	Unit
LVTTL Compatible Output Pins (QFA[0:1], [1:4]Q[A:B][0:1], LOCK)						
V_{OH}	LVTTL HIGH voltage	QFA[0:1], [1:2]Q[A:B][0:1]	V_{CC} = Min., I_{OH} = –30 mA	2.4	–	V
		LOCK	I_{OH} = –2 mA, V_{CC} = Min.	2.4	–	V
V_{OL}	LVTTL LOW voltage	QFA[0:1], [1:2]Q[A:B][0:1]	V_{CC} = Min., I_{OL}= 30 mA	–	0.5	V
		LOCK	I_{OL}= 2 mA, V_{CC} = Min.	–	0.5	V
I_{OZ}	High impedance state leakage current			–100	100	μA
LVTTL Compatible Input Pins (FBKA, REFA±, REFB±, REFSEL, DIS[1:2])						
V_{IH}	LVTTL Input HIGH	FBKA+, REF[A:B]±	Min. ≤ V_{CC} ≤ Max.	2.0	V_{CC} + 0.3	V
		REFSEL, DIS[1:2]		2.0	V_{CC} + 0.3	V
V_{IL}	LVTTL Input LOW	FBKA+, REF[A:B]±	Min. ≤ V_{CC} ≤ Max.	–0.3	0.8	V
		REFSEL, DIS[1:2]		–0.3	0.8	V
I_I	LVTTL V_{IN} > V_{CC}	FBKA+, REF[A:B]±	V_{CC} = GND, V_{IN} = 3.63V	–	100	μA
I_{IH}	LVTTL Input HIGH Current	FBKA+, REF[A:B]±	V_{CC} = Max., V_{IN} = V_{CC}	–	500	μA
		REFSEL, DIS[1:2]	V_{IN} = V_{CC}	–	500	μA
I_{IL}	LVTTL Input LOW Current	FBKA+, REF[A:B]±	V_{CC} = Max., V_{IN} = GND	–500	–	μA
		REFSEL, DIS[1:2]		–500	–	μA
3-Level Input Pins (FBDS[0:1], FS, Output_Mode)						
V_{IHH}	Three level input HIGH[4]		Min. ≤ V_{CC} ≤ Max.	0.87 × V_{CC}	–	V
V_{IMM}	Three level input MID[4]		Min. ≤ V_{CC} ≤ Max.	0.47 × V_{CC}	0.53 × V_{CC}	V
V_{ILL}	Three level input LOW[4]		Min. ≤ V_{CC} ≤ Max.	–	0.13 × V_{CC}	V
I_{IHH}	Three level input HIGH current	Three level input pins	V_{IN} = V_{CC}	–	200	μA
I_{IMM}	Three level input MID current	Three level input pins	V_{IN} = V_{CC}/2	–50	50	μA
I_{ILL}	Three level input LOW current	Three level input pins	V_{IN} = GND	–200	–	μA

Note

4. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold the unconnected inputs at V_{CC}/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.

Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description		Test Conditions	Min	Max	Unit
LVDIFF Input Pins (REF[A:B]±)						
V_{DIFF}	Input differential voltage			400	V_{CC}	mV
V_{IHHP}	Highest input HIGH voltage			1.0	V_{CC}	V
V_{ILLP}	Lowest input LOW voltage			GND	$V_{CC} – 0.4$	V
V_{COM}	Common mode range (crossing voltage)			0.8	V_{CC}	V
Operating Current						
I_{CCI}	Internal operating current	CY7B9930V	V_{CC} = Max., f_{MAX}[5]	–	200	mA
		CY7B9940V		–	200	mA
I_{CCN}	Output current dissipation/pair[6]	CY7B9930V	V_{CC} = Max., C_{LOAD} = 25 pF, R_{LOAD} = 50Ω at $V_{CC}/2$, f_{MAX}	–	40	mA
		CY7B9940V		–	50	mA

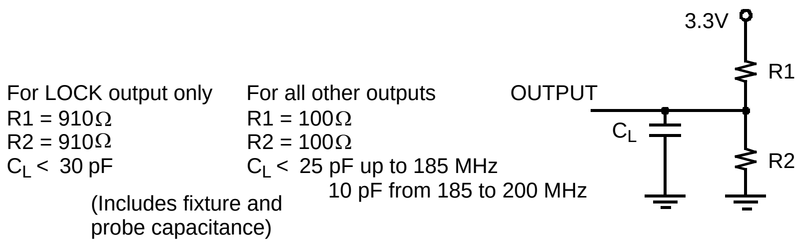
Notes
5. I_{CCI} measurement is performed with Bank1 and FB Bank configured to run at maximum frequency (f_{NOM} = 100 MHz for CY7B9930V, f_{NOM} = 200 MHz for CY7B9940V), and all other clock output banks to run at half the maximum frequency. FS and OUTPUT_MODE are asserted to the HIGH state.
6. This is dependent upon frequency and number of outputs of a bank being loaded. The value indicates maximum I_{CCN} at maximum frequency and maximum load of 25 pF terminated to 50Ω at $V_{CC}/2$.

Capacitance

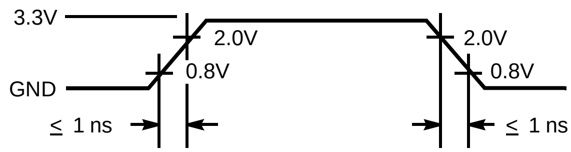
Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	–	5	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveform [7]



(a) LVTTL AC Test Load



(b) TTL Input Test Waveform

Note
7. These figures are for illustration only. The actual ATE loads may vary.

Switching Characteristics

Over the Operating Range [8, 9, 10, 11, 12]

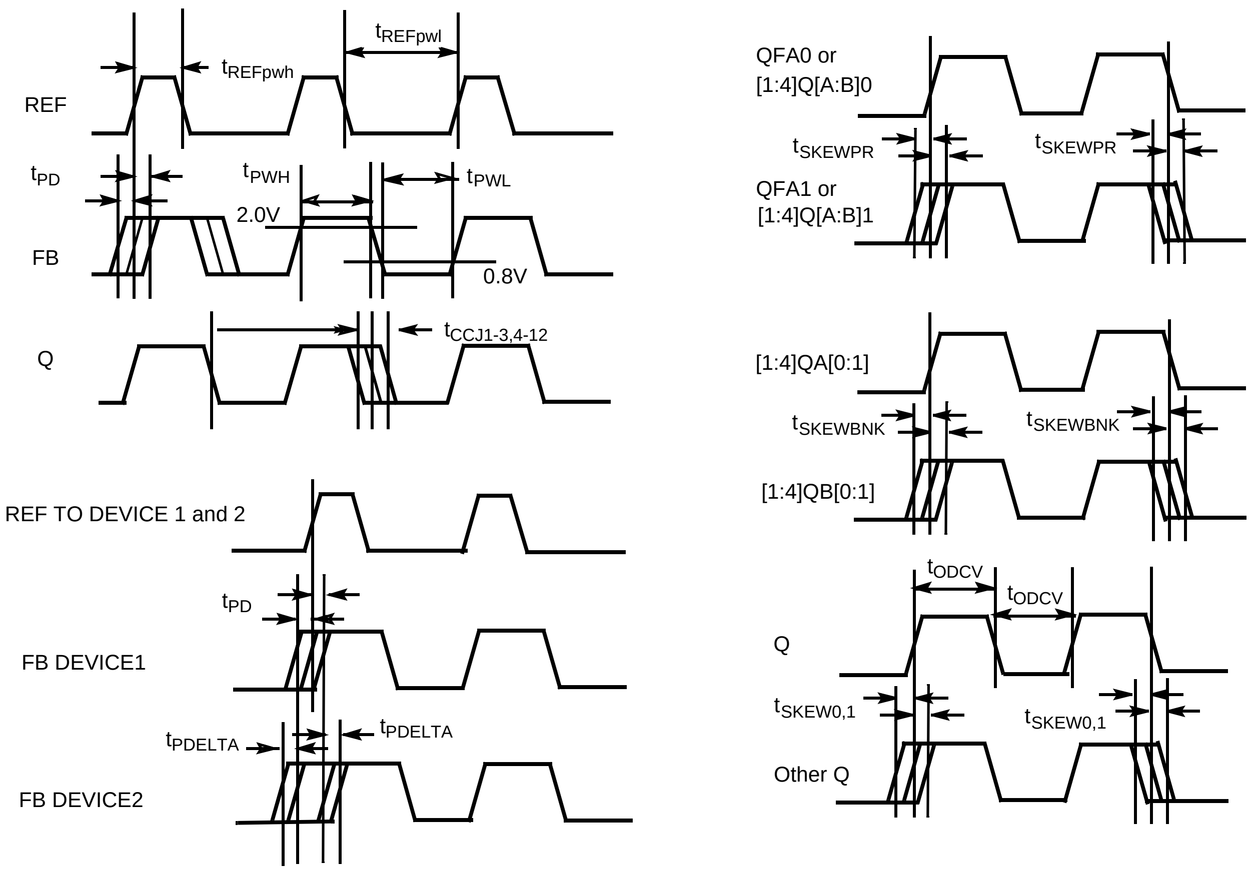
Parameter	Description		CY7B9930/40V-2		CY7B9930/40V-5		Unit
			Min.	Max.	Min.	Max.	
f_{in}	Clock input frequency	CY7B9930V	12	100	12	100	MHz
		CY7B9940V	24	200	24	200	MHz
f_{out}	Clock input frequency	CY7B9930V	12	100	12	100	MHz
		CY7B9940V	24	200	24	200	MHz
t_{SKEWPR}	Matched pair skew [13, 14]		–	185	–	185	ps
$t_{SKEWBNK}$	Intrabank skew [13, 14]		–	200	–	250	ps
t_{SKEW0}	Output-Output skew (same frequency and phase, rise to rise, fall to fall) [13, 14]		–	250	–	550	ps
t_{SKEW1}	Output-Output skew (same frequency and phase, other banks at different frequency, rise to rise, fall to fall) [13, 14]		–	250	–	650	ps
t_{CCJ1-3}	Cycle-to-cycle jitter (divide by 1 output frequency, FB = divide by 1, 2, 3)		–	150	–	150	ps Peak-Peak
$t_{CCJ4-12}$	Cycle-to-cycle jitter (divide by 1 output frequency, FB = divide by 4, 5, 6, 8, 10, 12)		–	100	–	100	ps Peak-Peak
t_{PD}	Propagation delay, REF to FB Rise		–250	250	–500	500	ps
$t_{PDDELTA}$	Propagation delay difference between two devices [15]		–	200		200	ps
t_{REFpwh}	REF input (pulse width HIGH) [16]		2.0	–	2.0	–	ns
t_{REFpwl}	REF input (pulse width LOW) [16]		2.0	–	2.0	–	ns
t_r/t_f	Output rise/fall time [17]		0.15	2.0	0.15	2.0	ns
t_{LOCK}	PLL lock time from power up		–	10	–	10	ms
$t_{RELOCK1}$	PLL relock time (from same frequency, different phase) with stable power supply		–	500	–	500	µs
$t_{RELOCK2}$	PLL Relock Time (from different frequency, different phase) with Stable Power Supply [18]		–	1000	–	1000	µs
t_{ODCV}	Output duty cycle deviation from 50% [12]		–1.0	1.0	–1.0	1.0	ns
t_{PWH}	Output HIGH time deviation from 50% [19]		–	1.5	–	1.5	ns
t_{PWL}	Output LOW time deviation from 50% [19]		–	2.0	–	2.0	ns
t_{PDEV}	Period deviation when changing from reference to reference [20]		–	0.025	–	0.025	UI
t_{OAZ}	DIS[1:2] HIGH to output high impedance from ACTIVE [13, 21]		1.0	10	1.0	10	ns
t_{OZA}	DIS[1:2] LOW to output ACTIVE from output is high impedance [21, 22]		0.5	14	0.5	14	ns

Notes

8. This is for non-three level inputs.
9. Assumes 25 pF Max. Load Capacitance up to 185 Mhz. At 200 MHz the max load is 10 pF.
10. Both outputs of pair must be terminated, even if only one is being used.
11. Each package must be properly decoupled.
12. AC parameters are measured at 1.5V, unless otherwise indicated.
13. Test Load C_L= 25 pF, terminated to $V_{CC}/2$ with 50Ω.
14. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same phase delay has been selected when all outputs are loaded with 25 pF and properly terminated up to 185 MHz. At 200 MHz the max load is 10 pF.
15. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
16. Tested initially and after any design or process changes that may affect these parameters.
17. Rise and fall times are measured between 2.0V and 0.8V.
18. f_{NOM} must be within the frequency range defined by the same FS state.
19. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.
20. UI = Unit Interval. Examples: 1 UI is a full period. 0.1 UI is 10% of period.
21. Measured at 0.5V deviation from starting voltage.
22. For t_{OZA} minimum, C_L = 0 pF. For t_{OZA} maximum, C_L= 25 pF to 18 MHz, 10 pF from 185 to 200 MHz.

AC Timing Diagrams

Figure 3. AC Timing Diagrams [23]



Note
23. AC parameters are measured at 1.5 V, unless otherwise indicated.

Ordering Information

Propagation Delay (ps)	Max Speed (MHz)	Ordering Code	Package Type	Operating Range
Pb-free				
500	100	CY7B9930V-5AXC	44-pin TQFP	Commercial
500	100	CY7B9930V-5AXCT	44-pin TQFP – Tape and Reel	Commercial
500	200	CY7B9940V-5AXC	44-pin TQFP	Commercial
500	200	CY7B9940V-5AXCT	44-pin TQFP – Tape and Reel	
250	200	CY7B9940V-2AXC	44-pin TQFP	Commercial
250	200	CY7B9940V-2AXCT	44-pin TQFP – Tape and Reel	

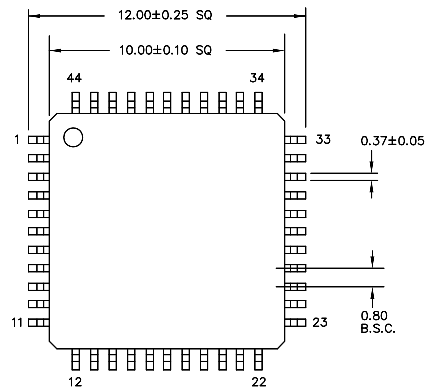
Ordering Code Definitions

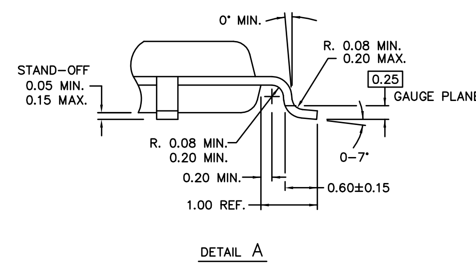
CY 7B99X0 V - A X C X

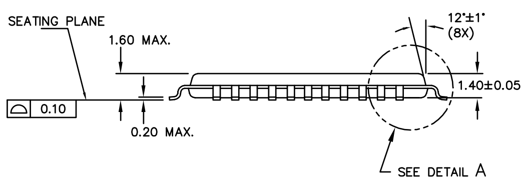
- X blank or T
  blank = Tube; T = Tape and Reel
- Temperature Range: C = Commercial
- X = Pb-free
- Package Type: A = 44-pin TQFP package
- V = 3.3 V
- Base part number: 7B99X0 = 7B9930 or 7B9940
  7B9930 = 12–100 MHz I/O operation clock buffer
  7B9940 = 24–200 MHz I/O operation clock buffer
- Company ID: CY = Cypress

Package Diagram

Figure 4. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064







NOTE:

1. JEDEC STD REF MS–026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *E

Acronyms

Acronym	Description
EMI	Electromagnetic Interference
LVPECL	Low-Voltage Positive-Referenced Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	Phase-Locked Loop
TQFP	Thin Quad Flat Pack
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: RoboClockII™ Junior, CY7B9930V, CY7B9940V, High Speed Multifrequency PLL Clock Buffer Document Number: 38-07271				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	110536	12/02/01	SZV	Change from Spec number: 38-01141
*A	115109	7/03/02	HWT	Add 44TQFP package for both CY7B9930/40V – Industrial Operating Range
*B	128463	7/29/03	RGL	Added clock input frequency (f_{in}) specifications in the switching characteristics table. Added Min. values for the clock output frequency (f_{out}) in the switching characteristics table.
*C	1346903	8/8/07	WWZ / VED / ARI	Update the ordering info to reflect the current status and Pb-free part numbers. Implemented new template. Updated the package diagram.
*D	2894960	03/18/2010	KVM	Added Table of Contents Removed part numbers CY7B9930V-5AC, CY7B9930V-5AI, CY7B9940V-5AC, CY7B9940V-5AI, CY7B9930V-2AC, CY7B9930V-2AI and CY7B9940V-2AI in ordering information table. Updated package diagram Added Sales, Solutions, and Legal Information
*E	2906750	04/07/2010	KVM	Removed inactive part from Ordering Information table.
*F	3053421	10/08/2010	CXQ	Removed inactive parts CY7B9940V-2AXI, CY7B9940V-2AXIT from Ordering Information table. Added Ordering Code Definition.
*G	3859773	01/07/2013	AJU	Updated Ordering Information (Updated part numbers). Updated Package Diagram: spec 51-85064 – Changed revision from *D to *E.
*H	4177300	10/29/2013	CINM	Added Acronyms and Units of Measure. Updated in new template. Completing Sunset Review.

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