# AN8133FHP (Under development)

## High Speed Low Power Consumption Bi-CMOS 10-Bit A/D Converter

### ■ Overview

The AN8133FHP is a 10-bit A/D converter for image processing which employs the Bi-CMOS process to realize the low power consumption.

### ■ Features

- 10-bit resolution
- Maximum conversion rate : 40 MSPS (min.)
- Low power consumption : 200 mW (typ.)
- Operation on single power supply of 5 V
- S/H circuit not required
- Input/Output form : TTL level compatible

### ■ Application Field

- Digital video broadcasting such as D-STB
- Image equipment such as HDTV
- OA equipment such as image scanner
- Medical equipment such as ultrasonic diagnosis device

Note) Since the AN8133FHP is under development, the description here may be modified without any prior notice. When the final design is reviewed, refer to the up-to-date product standards.

Unit : mm

48-pin QFP Package (QFH048-P-0707)
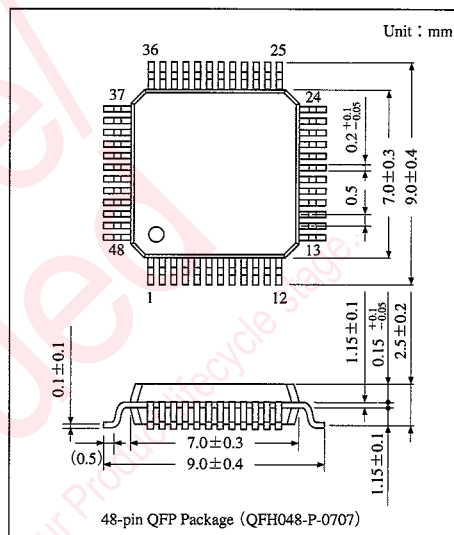
### ■ Block Diagram
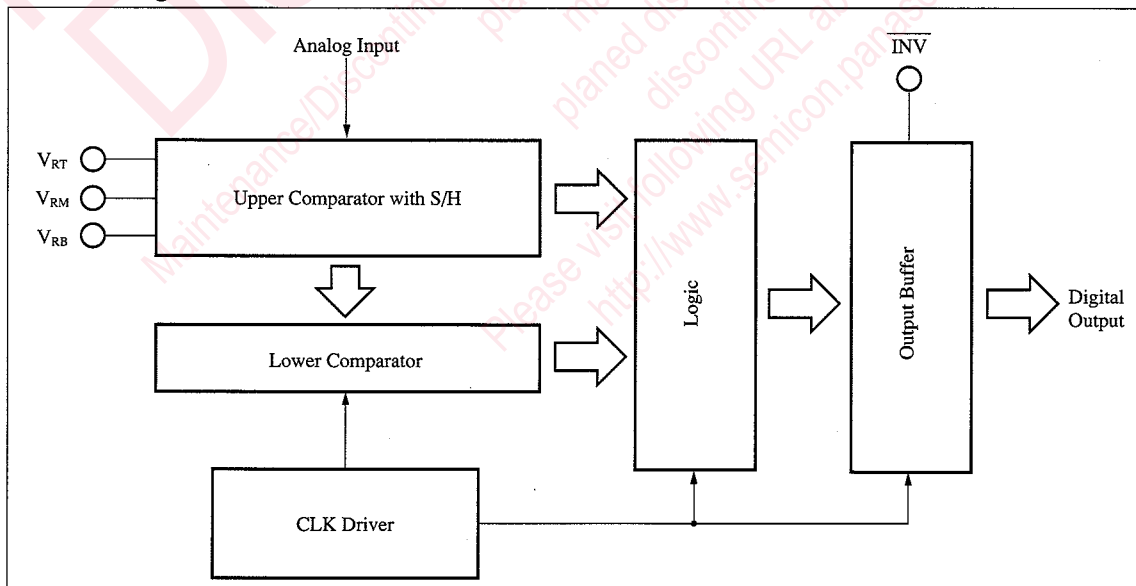
■ **Absolute Maximum Rating** (Ta＝25℃)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | $-0.5$ to $+6.0$ | V |
| Analogue input voltage | $V_{IN}$ | 0 to $V_{CC}+0.3$ | V |
| Digital input voltage | $V_{CLK}$ | $-0.5$ to $V_{CC}+0.5$ | V |
| Digital output current | $I_{OVF}/I_{D0}$ to $I_{D9}$ | $-15$ | mA |
| Reference voltage | $V_{RT}/V_{RB}$ | 0 to $V_{CC}+0.5$ | V |
| Power dissipation | $P_D$ | 700 (Ta＝75℃) | mW |
| Operating ambient temperature | $T_{opr}$ | 0 to 75 | ℃ |
| Storage temperature | $T_{stg}$ | $-55$ to $+150$ | ℃ |

■ **Recommended Operating Conditions** (Ta＝25℃)

| Parameter | Symbol | Condition | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 4.75 | 5.0 | 5.25 | V |
| Reference voltage | $V_{RT}$ | | —— | 4.25 | —— | V |
| | $V_{RB}$ | | —— | 2.25 | —— | V |
| Analogue input voltage | $V_{IN}$ | | $V_{RB}$ | —— | $V_{RT}$ | V |
| Digital input voltage | $V_{IH}$ | | 2 | —— | 4 | V |
| | $V_{IL}$ | | —— | —— | 0.8 | V |
| Digital output current | $I_{OH}$ | $V_{OH}=2.7V$ | —— | $-0.4$ | —— | mA |
| | $I_{OL}$ | $V_{OL}=0.4V$ | —— | 1.6 | —— | mA |
| Clock input pulse width | | | —— | 50 | —— | % |

■ **Electrical Characteristics** ($V_{CC}=5V$, Ta＝25℃)

| Parameter | Symbol | Condition | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$ | | —— | 40 | —— | mA |
| Reference resistive current | $I_{RT}$ | $V_{RT}=4.25V$ | —— | 2.4 | —— | mA |
| | $I_{RB}$ | $V_{RB}=2.25V$ | —— | $-2.4$ | —— | mA |
| Input bias current | $I_{IN}$ | $V_{IN}=3.2V$ | —— | —— | 150 | $\mu$A |
| Clock input current | $I_{IH}$ | $V_{CLK}=2.7V$ | —— | 1 | —— | $\mu$A |
| | $I_{IL}$ | $V_{CLK}=0.4V$ | —— | 1 | —— | $\mu$A |
| Digital output voltage | $V_{OH}$ | $I_{OH}=-400\mu A$ | 2.7 | 3.4 | —— | V |
| | $V_{OL}$ | $I_{OL}=1.6mA$ | —— | —— | 0.4 | V |
| Linearity error | $E_L$ | $V_{IN}=2V_{P-P}$ | —— | $\pm1$ | —— | LSB |
| Differential linearity error | $E_D$ | $V_{IN}=2V_{P-P}$ | —— | —— | 1.0 | LSB |
| Maximum conversion rate | $F_C$ | $V_{IN}=2V_{P-P}$ | 40 | —— | —— | MSPS |
| Quantization noise | S/N | $f_{CLK}=40MHz$, $f_{IN}=1MHz$ | —— | 55 | —— | dB |
| | | $f_{CLK}=40MHz$, $f_{IN}=15MHz$ | —— | 50 | —— | dB |
| Difference gain | DG | IRE standard 15Kz Sawtooth 40%subcarrier $f_{CLK}=20MHz$, Nolock | —— | 0.5 | 1.0 | % |
| Differential phase | DP | | —— | 0.5 | 1.0 | ℃ |
| Input band | BW | $V_{IN}=2V_{P-P}$, $-3dB$ | 50 | —— | —— | MHz |
| Digital output delay | $\tau_d$ | $f_{CLK}=40MHz$ | —— | 20 | —— | ns |
| Input capacitance | $C_{IN}$ | $V_{IN}=3.25V$ | —— | 10 | —— | pF |

## ■ Pin Description

| Pin No. | Symbol | Pin name | Standard waveform | Voltage level | Description |
|---|---|---|---|---|---|
| 42 | $\overline{\text{INV}}$ | Digital output invert pin | | TTL | Setting $\overline{\text{INV}}$ pin to "L" level inverts all the data outputs (D0-D9) but not the overflow output. This pin is set to "L" level with no connection and operates a synchronously with clock. |
| 24,30 39,40 43,47 | DVCC | Digital power supply pin | | 5V | It is a power supply pin for digital circuit block. Connect tantalum capacitor of several $\mu$F and ceramic capacitor of $0.1 \mu$F as near as possible to this pin between this pin and DGND. |
| 21,23 31,38 41,46 | DGND | Digital ground | | 0V | Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip. |
| 37 | OVF | Overflow pin | | TTL | When overflow occurs, it becomes "H." This pin is not affected by $\overline{\text{INV}}$ pin. |
| 25 26 27 28 29 32 33 34 35 36 | D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 | Digital output (LSB) Digital output Digital output Digital output Digital output Digital output Digital output Digital output Digital output Digital output (MSB) | Refer to the timing chart. | TTL | It is an output pin of TTL Level. In order to prevent the digital noise to entering the analogue circuit, suppress the ringing as far as possible. |
| 3,6 8,10 13,15 18,45 48 | AGND | Analogue ground | | 0V | Connect the AGND and DGND with the possible lowest impedance at one point as near as the chip. |
| 11 12 14 16 17 | $V_{RT}$ $V_{RTS}$ $V_{RM}$ $V_{RBS}$ $V_{RB}$ | Reference voltage high level, Reference voltage middle point level, Reference voltage low level | | 4.25V 3.25V 2.25V | It is used to set the reference voltage for comparator. Normally, $V_{RT}$ is given 4.25V and $V_{RB}$ is given 2.25V. Connect tantalum capacitor of several $\mu$F and ceramic capacitor of $0.1 \mu$F in parallel between each pin and analogue ground. $V_{RM}$ is provided for linearity compensation, which gives middle point potential between $V_{RT}$ and $V_{RB}$. However, it is normally opened. $V_{RTS}$ and $V_{RBS}$ are sense pin of $V_{RT}$ or $V_{RB}$ respectively. |
| 9 | $V_{IN}$ | Analogue input pin | | 2.25V~4.25V | It is an input pin of analogue signal for A/D conversion circuit. |
| 1,2 7,19 44 | AVCC | Analogue power supply pin | | 5.0V | It is a power supply pin for analogue circuit block. Connect tantalum capacitor of several $\mu$F and ceramic capacitor of $0.1 \mu$F as near as possible to this pin between this pin and AGND. |
| 22 | CLK | Clock input | Refer to the timing chart. | TTL | It is a clock for sampling. For their timing, refer to the timing chart. |

Pin No.4 , 5 , 20 ： NC

A/D and D/A Converters

■ **Output Code**

| Step | Input signal | | | Digital output | | | |
|------|------|------|------|------|------|------|------|
| | 2.000VFS | 1.953mV | STEP | $\overline{\text{INV}}$=H | | $\overline{\text{INV}}$=L | |
| | | | | M        L | | M        L | |
| | | | | OVF9876543210 | | OVF9876543210 | |
| 000 | | 4.250000 | | 0 | 0000000000 | 0 | 1111111111 |
| 001 | | 4.248047 | | 0 | 0000000001 | 0 | 1111111110 |
| . | | . | | | . | | . |
| . | | . | | | . | | . |
| . | | . | | | . | | . |
| 511 | | 3.251953 | | 0 | 0111111111 | 0 | 1000000000 |
| 512 | | 3.250000 | | 0 | 1000000000 | 0 | 0111111111 |
| 513 | | 3.248047 | | 0 | 1000000001 | 0 | 0111111110 |
| . | | . | | | . | | . |
| . | | . | | | . | | . |
| . | | . | | | . | | . |
| 1023 | | 2.251953 | | 0 | 1111111111 | 0 | 0000000000 |
| 1024 | | 2.250000 | | 1 | 1111111111 | 1 | 0000000000 |

■ **Timing Chart**
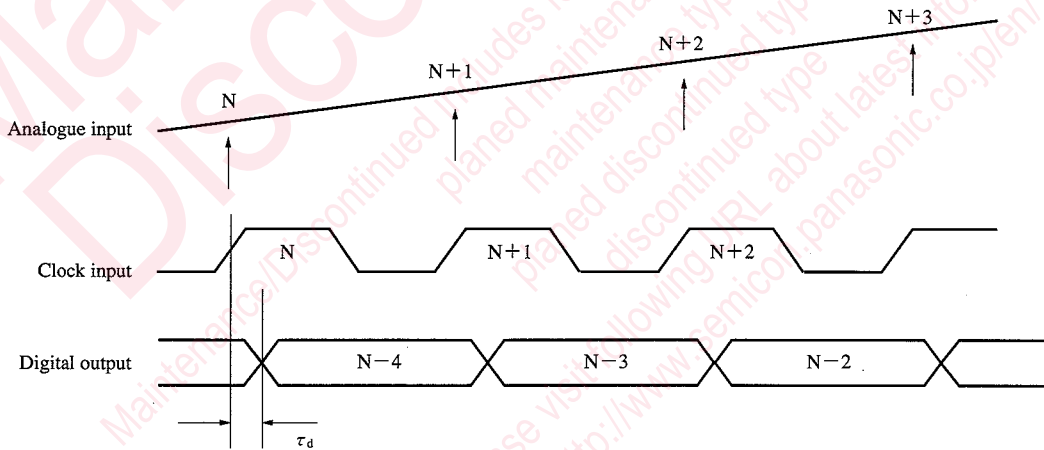
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