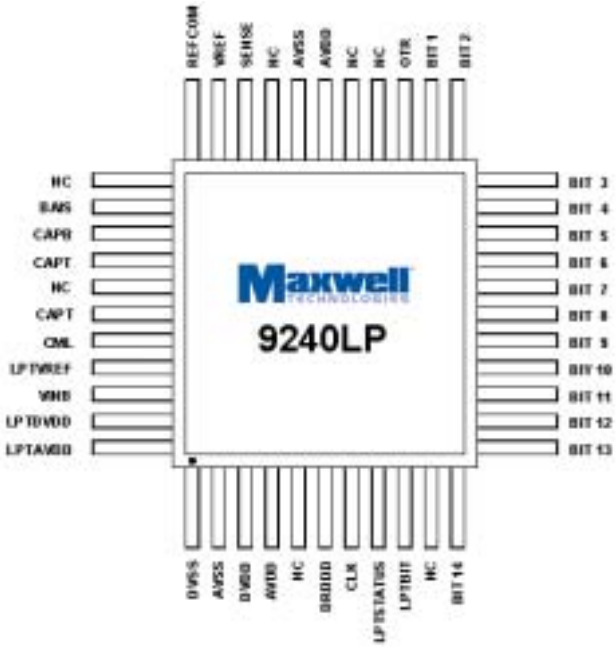
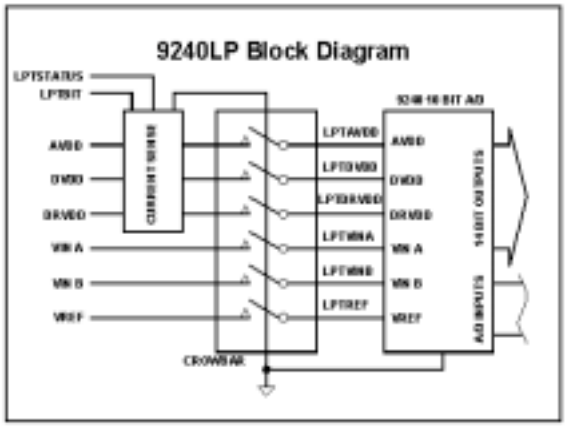
9240LP

14-Bit, 10 MSPS Monolithic A/D Converter with LPT ASIC





FEATURES:

- RAD-PAK® radiation-hardened against natural space radiation
- Low power dissipation: 230 mW
- Single 5 V supply
- Integral nonlinearity error: 2.5 LSB
- Differential nonlinearity error: 0.6 LSB
- Input referred noise: 0.36 LSB
- Complete: On-chip sample-and-hold amplifier and voltage reference
- Signal-to-noise ratio: 77 dB
- Spurious-free dynamic range: 90 dB
- Out-of-range indicator
- Straight binary output data
- Total dose hardened to 100 Krads (Si), dependent on orbit and mission duration
- Single Event Latchup (SEL) protected

DESCRIPTION:

Maxwell Technologies' 9240LP is a 14-bit, analog-to-digital converter that operates at a 10 MSPS rate. Manufactured with a high speed CMOS process, this monolithic ADC contains an on-chip, high performance, low noise, sample-and-hold amplifier and programmable voltage reference.

The 9240LP offers single supply operation and dissipates only 230mW with a 5 volt supply. This device provides no missing codes and excellent temperature drift performance over the full operating temperature range.

The 9240LP utilizes Maxwell's LPT™ Latchup Protection Circuit.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides protection to 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. 9240LP PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	DVSS	Digital Ground
2, 29	AVSS	Analog Ground
3	DVDD	5V Digital Supply
4, 28	AVDD	5V Analog Supply
5	NC	No Connect
6	DRVDD	Digital Output Driver Supply
7	CLK	Clock Input Pin
8	LPTSTATUS	A 0 to 5V pulse is output during the decision time and protect time. Normally low.
9	LPTBIT	The LPT circuit will crowbar the power supplies to the 9240LP for as long as a logic high is applied. Used to verify operation of the LPT. Normally a logical low or ground is applied to this input.
10	NC	No Connect
11	BIT 14	Least Significant Data Bit (LSB)
12-23	BIT 13-BIT 2	Data Output Bits
24	BIT 1	Most Significant Data Bits (MSB)
25	OTR	Out of Range
26, 27, 30	NC	No Connect
31	SENSE	Reference Select
32	V_{REF}	Reference I/O
33	REFCOM	Reference Common
34, 38	NC	No Connect
35	BIAS	Power/Speed Programming
36	CAPB	Noise Reduction Pin
37	CAPT	Noise Reduction Pin
39	CML	Common-Mod Level (Midsupply)
40	$LPTV_{REF}$	Protected Reference I/O
41	$V_{IN}A$	Analog Input Pin (+)
42	$V_{IN}B$	Analog Input Pin (-)
43	LPTDVDD	Protected 5V Digital Supply
44	LPTAVDD	Protected 5V Analog Supply

TABLE 2. 9240LP ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	SYMBOL	WITH RESPECT TO	MIN	MAX	UNIT
+5 V Analog Supply	AVDD	AVSS	-0.3	6.5	V
+5 V Digital Supply	DVDD	DVSS	-0.3	6.5	V
Analog Ground	AVSS	DVSS	-0.3	0.3	V
+5 V Analog Supply	AVDD	DVDD	-6.5	6.5	V
Digital Output Driver Supply	DRVDD	DRVSS	-0.3	6.5	V
Digital Output Driver Ground	DRVSS	AVSS	-0.3	0.3	V
Reference Common	REFCOM	AVSS	-0.3	0.3	V
Clock Input Pin	CLK	AVSS	-0.3	AVDD	V
Digital Outputs	Data Out Bits	DRVSS	-0.3	DVDD	V
Analog Inputs	$V_{IN}A$, $V_{IN}B$	AVSS	-0.3	AVDD	V
Reference I/O	V_{REF}	AVSS	-0.3	AVDD	V
Reference Select	Sense	AVSS	-0.3	AVDD	V
Noise Reduction Pins	CAPB, CAPT	AVSS	-0.3	AVDD	V
Power/Speed Programming	BIAS	AVSS	-0.3	AVDD - 0.6	V
Junction Temperature	T_J		--	150	˚C
Operating Temperature	T_A		-55	125	°C
Storage Temperature	T_{STG}		-65	150	˚C
Lead Temperature (10 sec)	T_L		--	300	˚C

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{CC}	±10% OF SPECIFIED VALUE IN TABLE 4

TABLE 4. 9240LP DC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, R_{BIAS} = 2 kΩ, V_{REF} = 2.5V, $V_{IN}A = V_{IN}B$ = ± 2.5V DIFFERENTIAL INPUT CENTERED ON VREF(1.25V TO 3.75V ABSOLUTE), T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP[1]	MAX	UNIT
RESOLUTION	1	14	--	--	Bits
MAX REFERRED NOISE[1]					
V_{REF} = 1 V		--	0.9	--	LSB rms
V_{REF} = 2.5V		--	0.36	--	LSB rms
ACCURACY[2]	1, 2, 3				
Integral Nonlinearity (INL)	1, 2, 3	-3.0	±2.5	+3.0	LSB
Differential Nonlinearity (DNL)	1, 2, 3	--	±0.6	±1.0	LSB
INL [3]		--	±2.5	--	LSB
DNL [3]		--	±0.7	--	LSB
No Missing Codes	1	--		14	Bits Guaranteed
Zero Error (@ 25 °C)	1	.3	--	+.3	% FSR
Gain Error (@ 25 °C) [4,1]	--	1.5	--	1.5	% FSR
Gain Error (@ 25 °C) [5]	1	0.75	--	0.75	% FSR
TEMPERATURE DRIFT	1, 2, 3				
Zero Error		--	3.0	--	ppm/°C
Gain Error [4]		--	20.0	--	ppm/°C
Gain Error [5]		--	5.0	--	ppm/°C
POWER SUPPLY REJECTION	1, 2, 3	--	--	±0.1	% FSR
ANALOG INPUT[1]					
Input Span (with V_{REF} = 1.0 V)[1]		2	--	--	V p-p
(with V_{REF} = 2.5 V)	1, 2, 3	--	--	5	V p-p
Input ($V_{IN}A$ or $V_{IN}B$) Range		0	--	AVDD -.25	V
Input Capacitance[1]	--	--	16		pF
INTERNAL VOLTAGE REFERENCE[1]	--				
Output Voltage (1V mode)		--	1	--	Volts
Output Voltage Tolerance (1 V Mode)		--	--	±14	mV
Output Voltage (2.5 V Mode)		--	2.5	--	Volts
Output Voltage Tolerance (2.5 V Mode)		--	--	±35	mV
Load Regulation V_{REF}[6]		--	10	--	mV
Load Regulation $LPTV_{REF}$[1, 6, 7]		--	--	10.0	mV
REFERENCE INPUT RESISTANCE	1, 2, 3	--	5	--	kΩ

TABLE 4. 9240LP DC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, R_{BIAS} = 2 kΩ, V_{REF} = 2.5V, $V_{IN}A = V_{IN}B$ = ± 2.5V DIFFERENTIAL INPUT CENTERED ON VREF(1.25V TO 3.75V ABSOLUTE), T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP[1]	MAX	UNIT
LPT ASIC	1, 2, 3				
RDS ON					
- V_{REF}		--	8	15	ohm
		--	8	--	ohm
- V_{IN} A		--	105	--	ohm
- V_{IN} B			105	--	ohm
LATCHUP PROTECTION					
- Decision Time		--	10	--	µs
- Protect Time		--	70	--	µs
- AVDD Trip Current		--	75	--	mA
- AVDD Trip Current Tolerance		--	±15	--	mA
- DVDD Trip Current		--	28	--	mA
- DVDD Trip Current Tolerance		--	±5	--	mA
POWER SUPPLIES					
Supply Voltages					
- AVDD		--	5	--	V (±5% AVDD Operating)
- DVDD		--	5	--	V (±5% DVDD Operating)
- DRVDD		--	5	--	V (±5% DRVDD Operating)
Supply Current					
- IAVDD	1, 2, 3	--	43	55	mA
- IDVDD	1, 2, 3	--	3	16	mA
POWER CONSUMPTION[8]	1, 2, 3		230	355	mW

1. Guaranteed by design.
2. Tested using external V_{REF} with servo control
3. V_{REF} = 1V
4. Including internal reference.
5. Excluding internal reference.
6. Load regulation with 1 mA load current.
7. LPTV_{REF} should not be capacitively loaded above 0.1 µF.
8. Calculated from I_{DD}

TABLE 5. 9240LP AC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, f_{SAMPLE} = 10 MSPS, R_{BIAS} = 2 kΩ, V_{REF} = 2.5V, A_{IN} = -0.5 dBFS, AC COUPLED/DIFFERENTIAL INPUT, T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)					
f_{INPUT} = 500 KHz		--			dB
			76.0	--	dB
f_{INPUT} = 1.0 MHz		--	76	--	dB
f_{INPUT} = 5.0 MHz		--	74.5	--	dB
EFFECTIVE NUMBER OF BITS (ENOB)[1]					
f_{INPUT} = 500 KHz		12	--	--	Bits
		--	12.5	--	Bits
f_{INPUT} = 1.0 MHz		--	12.3	--	Bits
f_{INPUT} = 5.0 MHz		--	11.9	--	Bits
SIGNAL-TO-NOISE RATIO (SNR)	4, 5, 6				
f_{INPUT} = 500 KHz		74.5	77	--	dB
		--	77	--	dB
f_{INPUT} = 1.0 MHz		--	77	--	dB
f_{INPUT} = 5.0 MHz		--	77	--	dB
TOTAL HARMONIC DISTORTION (THD)					
f_{INPUT} = 500 KHz		--	-83	--	dB
f_{INPUT} = 1.0 MHz		--	-83.0	--	dB
f_{INPUT} = 5.0 MHz		--	-75.0	--	dB
SPURIOUS FREE DYNAMIC RANGE	4, 5, 6				
f_{INPUT} = 500 KHz		--	90.0	--	dB
f_{INPUT} = 1.0 MHz		--	90.0	--	dB
f_{INPUT} = 5.0 MHz		--	80.0	--	dB
DYNAMIC PERFORMANCE[2]					
Full Power Bandwidth		--	70	--	MHz
Small Signal Bandwidth		--	70	--	MHz
Aperture Delay		--	1	--	ns
Aperture Jitter		--	4	--	ps rms
Acquisition to Full-Scale Step (0.0025%)		--	45	--	ns
Overvoltage Recovery Time		--	167	--	ns
MAX CONVERSION RATE	9, 10, 11	10	--	--	MBits

1. ENOB calculated from SNR.
2. Guaranteed by design.

TABLE 6. 9240LP DIGITAL SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
CLOCK INPUT		1, 2, 3				
High Level Input Voltage[1]	V_{IH}		--	--	3.5	V
Low Level Input Voltage[1]	V_{IL}		--	--	1.0	V
High Level Input Current (V_{IN} = DVDD)	I_{IH}		--	--	±10	µA
Low Level Input Current (V_{IN} = 0V)	I_{IL}		--	--	±10	µA
Input Capacitance	C_{IN}		--	5	--	pF
LOGIC OUTPUTS (with DRVDD = 5V)		1, 2, 3				
High Level Output Voltage (I_{OH} = 50 µA)	V_{OH}		4.5	--	--	V
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}		2.4	--	--	V
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}		--	--	0.4	V
Low Level Output Voltage (I_{OL} = 50 µA)	V_{OL}		--	--	0.1	V
Output Capacitance[1]	C_{OUT}		--	5	--	pF

1. Guaranteed by design.

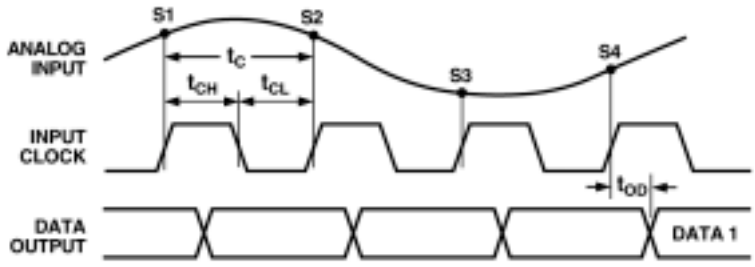
TABLE 7. 9240LP SWITCHING CHARACTERISTICS[1]

(T_A = -55 TO +125°C WITH AVDD = 5V, DVDD = 5V, DRVDD = 5V, R_{BIAS} = 2 kW, C_L = 20 pF)

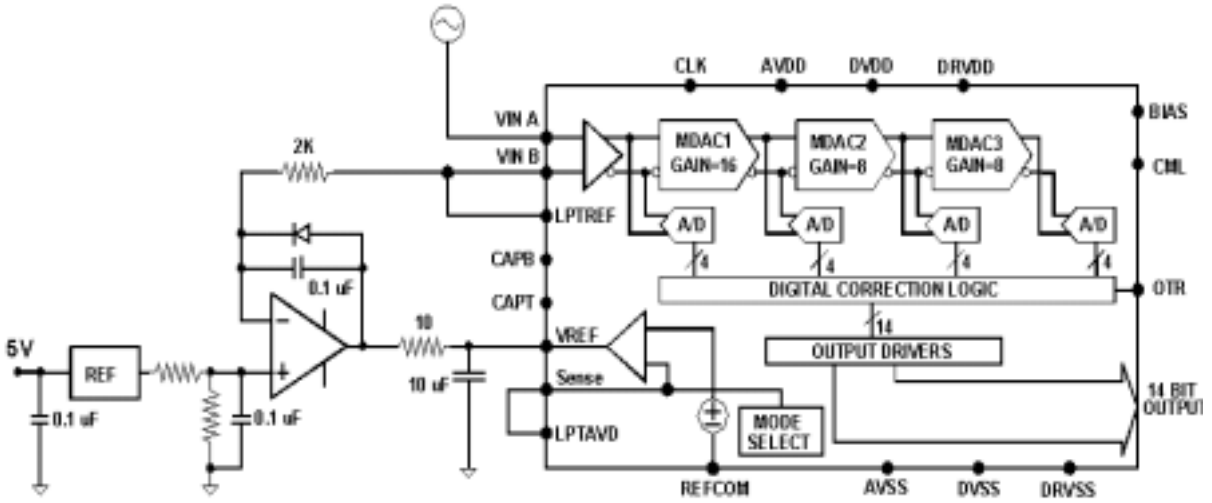
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock Period	t_C	100	--	--	ns
CLOCK Pulse width High	t_{CH}	45	--	--	ns
CLOCK Pulse width Low	t_{CL}	45	--	--	ns
Output Delay	t_{OD}	8	13	19	ns
Pipeline Delay (Latency)		--	3	--	Clock Cycles

1. Guaranteed by design.

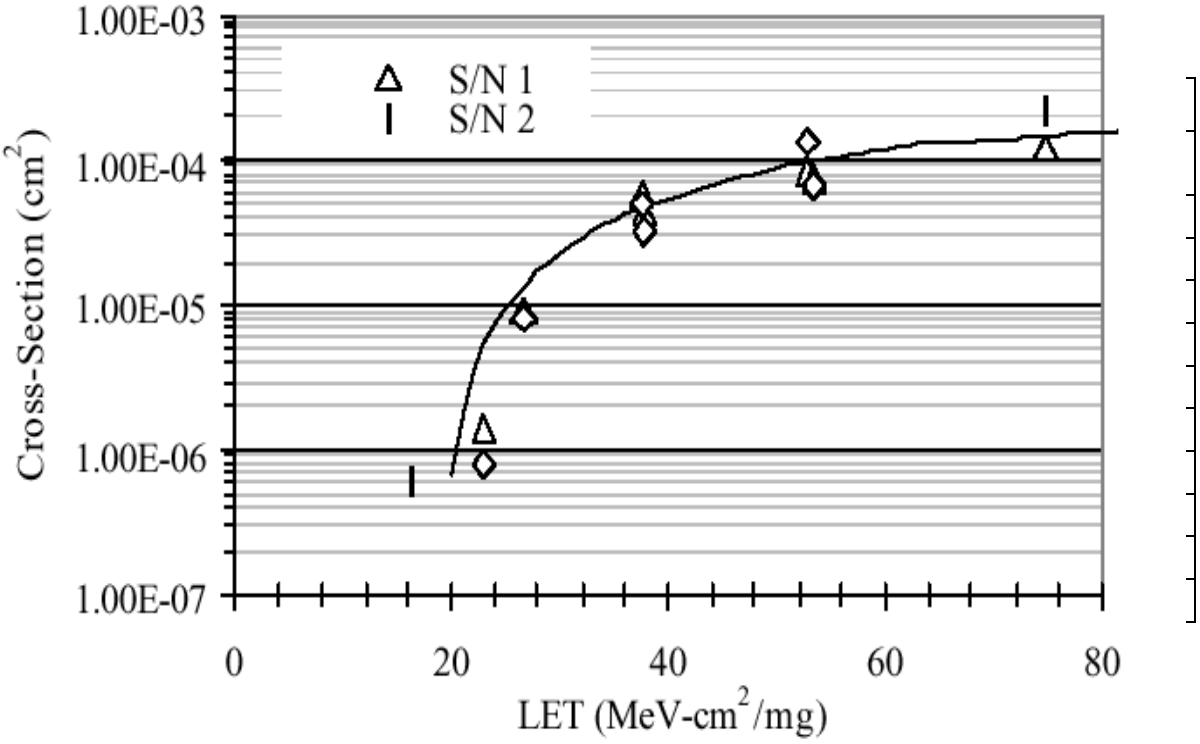
TIMING DIAGRAM



RECOMMENDED EXTERNAL REFERENCE



SEL CROSS SECTION



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