STL33N60M2

N-channel 600 V, 0.115 Ω typ., 22 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

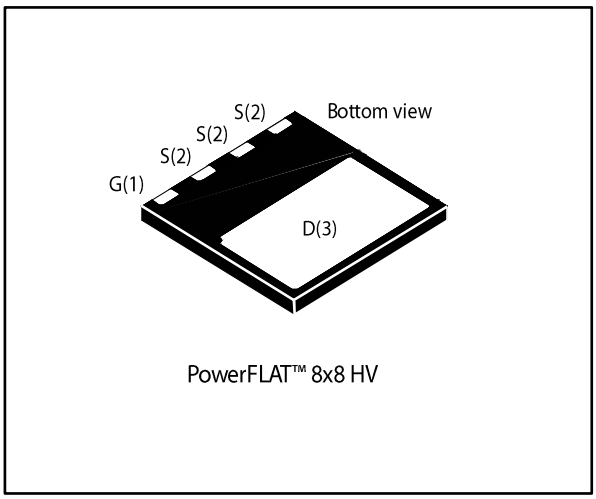
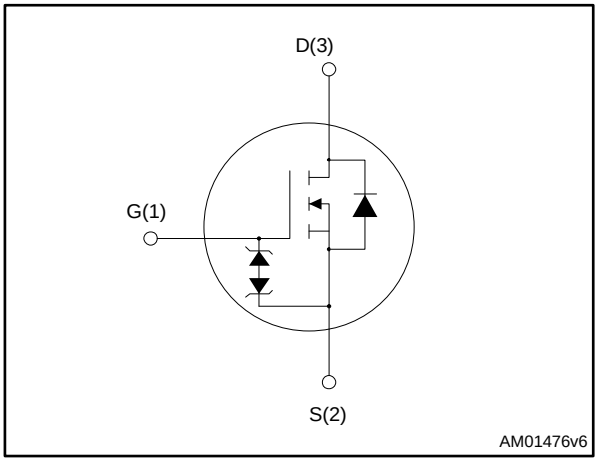


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)max}$	I_D
STL33N60M2	650 V	0.135 Ω	22 A

- Extremely low gate charge
- Excellent output capacitance (Coss) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the MDmesh™ M2 technology. Thanks to the strip layout associated to an improved vertical structure, the device exhibits both low on-resistance and optimized switching characteristics. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL33N60M2	33N60M2	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	22	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	13.8	A
I_{DM} (1)(2)	Drain current (pulsed)	88	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	190	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	1100	mJ
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1)The value is rated according to $R_{thj\text{-}case}$ and limited by package.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 22 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, VDD = 400 V.

(4)V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.66	°C/W
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient max	45	°C/W

Notes:

(1)When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 11 A		0.115	0.135	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1781	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	135	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 26 A V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	45.5	-	nC
Q_{gs}	Gate-source charge		-	9.9	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

Notes:

(1) Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 13 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"*)	-	16	-	ns
t_r	Voltage rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	109	-	ns
t_f	Current fall time		-	9	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
I_{SDM} (1)	Source-drain current (pulsed)		-		88	A
V_{SD} (2)	Forward on voltage	I_{SD} = 26 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 17: " Unclamped inductive load test circuit"*)	-	375		ns
Q_{rr}	Reverse recovery charge		-	5.6		µC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: " Unclamped inductive load test circuit"*)	-	478		ns
Q_{rr}	Reverse recovery charge		-	7.7		µC
I_{RRM}	Reverse recovery current		-	32.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

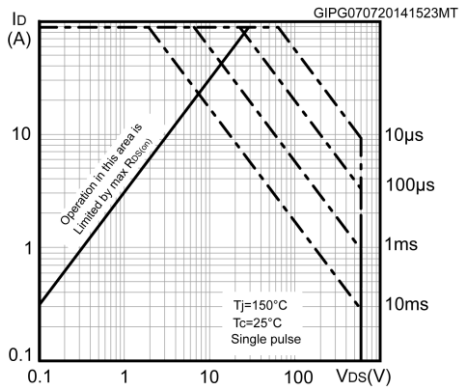


Figure 3: Thermal impedance

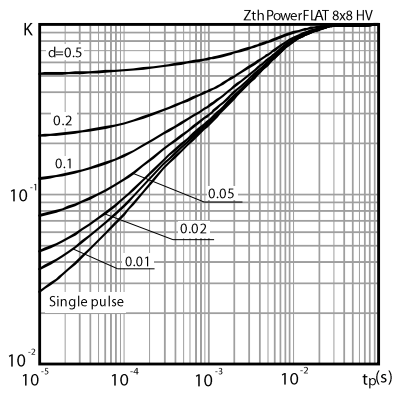


Figure 4: Output characteristics

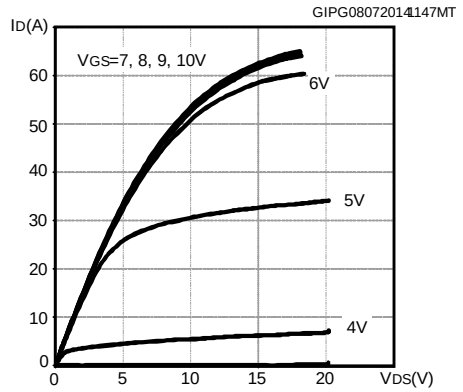


Figure 5: Transfer characteristics

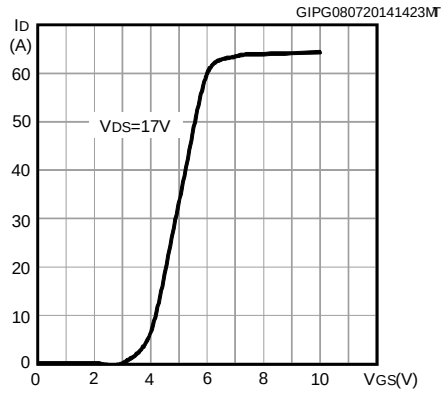


Figure 6: Gate charge vs gate-source voltage

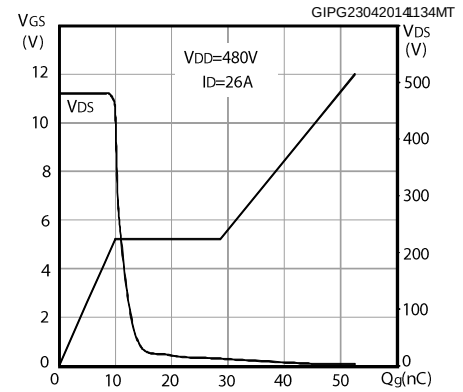


Figure 7: Static drain-source on-resistance

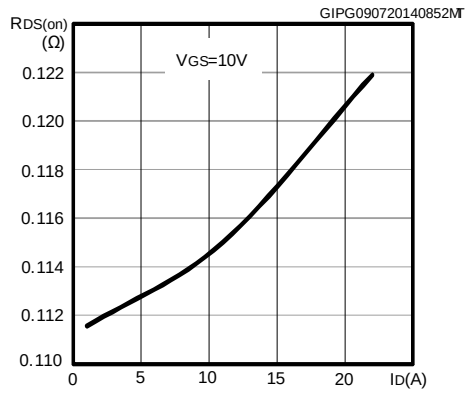


Figure 8: Capacitance variations

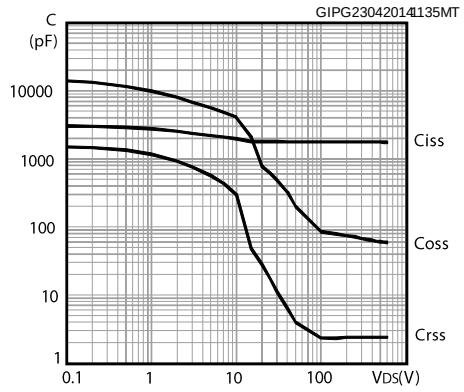


Figure 9: Normalized gate threshold voltage vs temperature

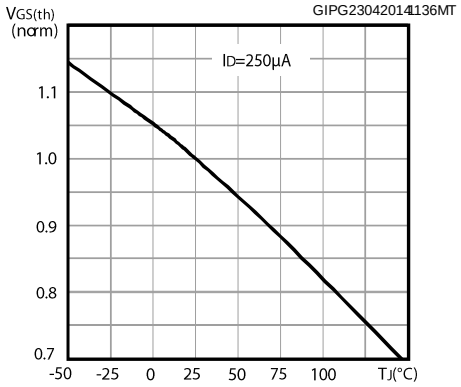


Figure 10: Normalized on-resistance vs temperature

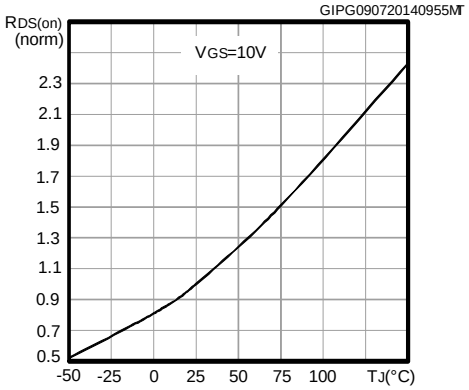


Figure 11: Normalized V(BR)DSS vs temperature

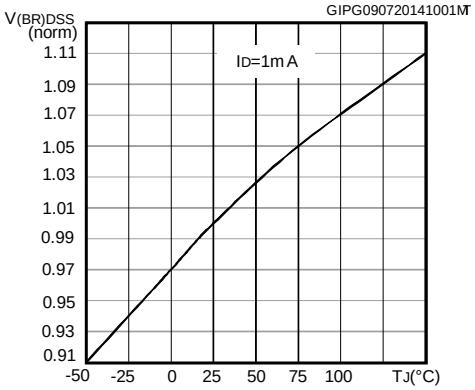


Figure 12: Source-drain diode forward characteristics

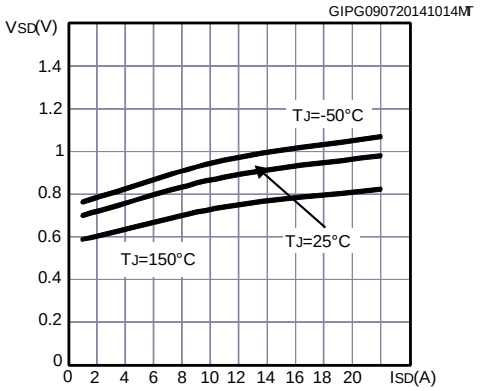
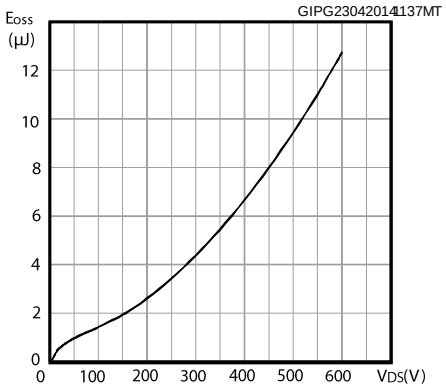


Figure 13: Output capacitance stored energy



3 Test circuits

Figure 14: Switching times test circuit for resistive load

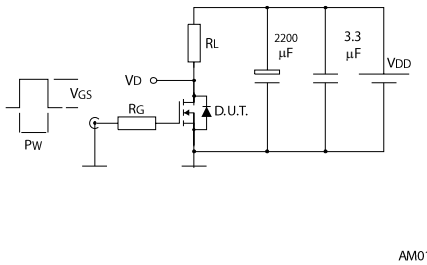


Figure 15: Gate charge test circuit

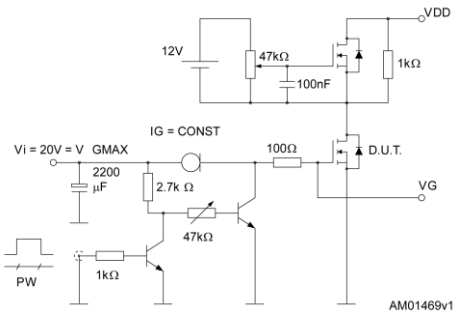


Figure 16: Test circuit for inductive load switching and diode recovery times

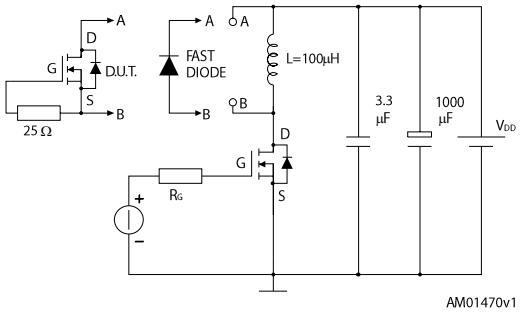


Figure 17: Unclamped inductive load test circuit

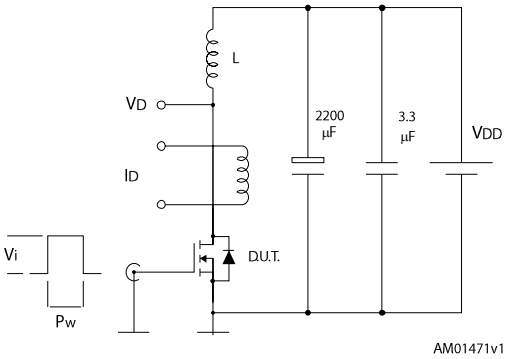


Figure 18: Unclamped inductive waveform

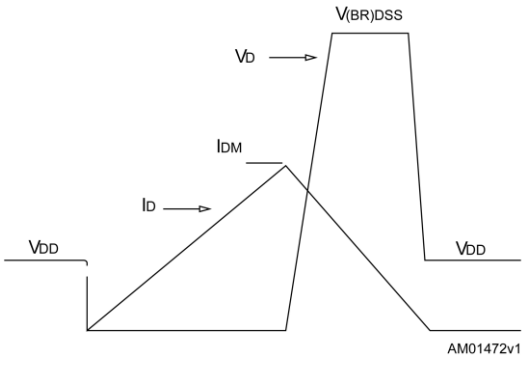
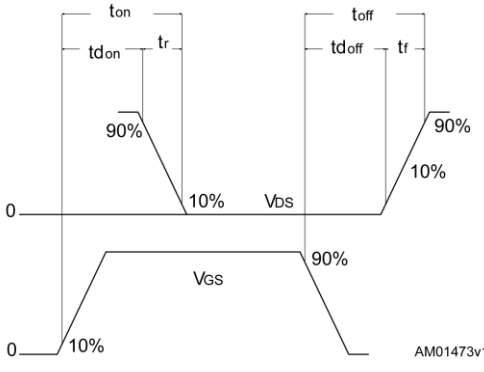


Figure 19: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package mechanical data

Figure 20: PowerFLAT™ 8x8 HV drawing mechanical data

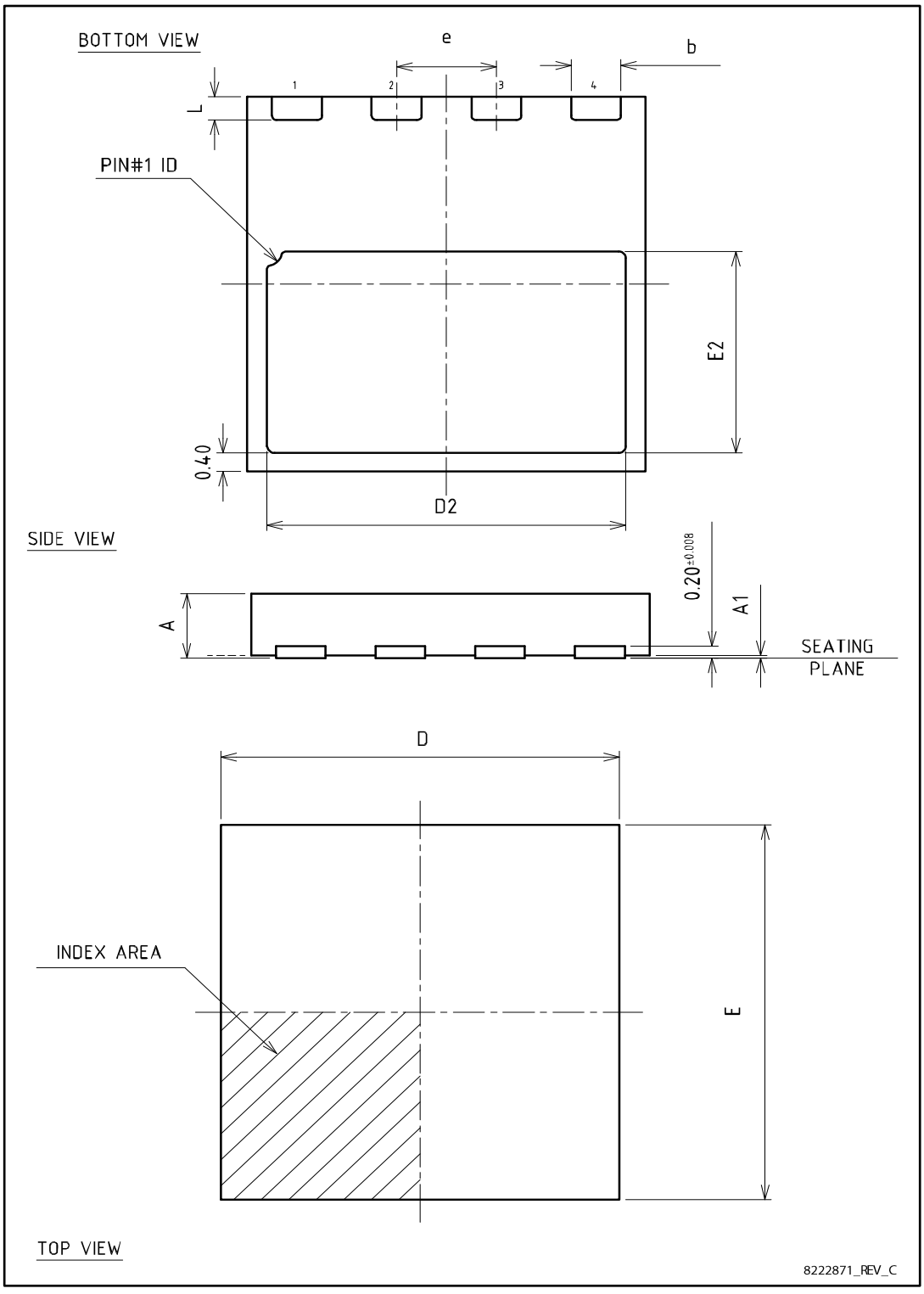
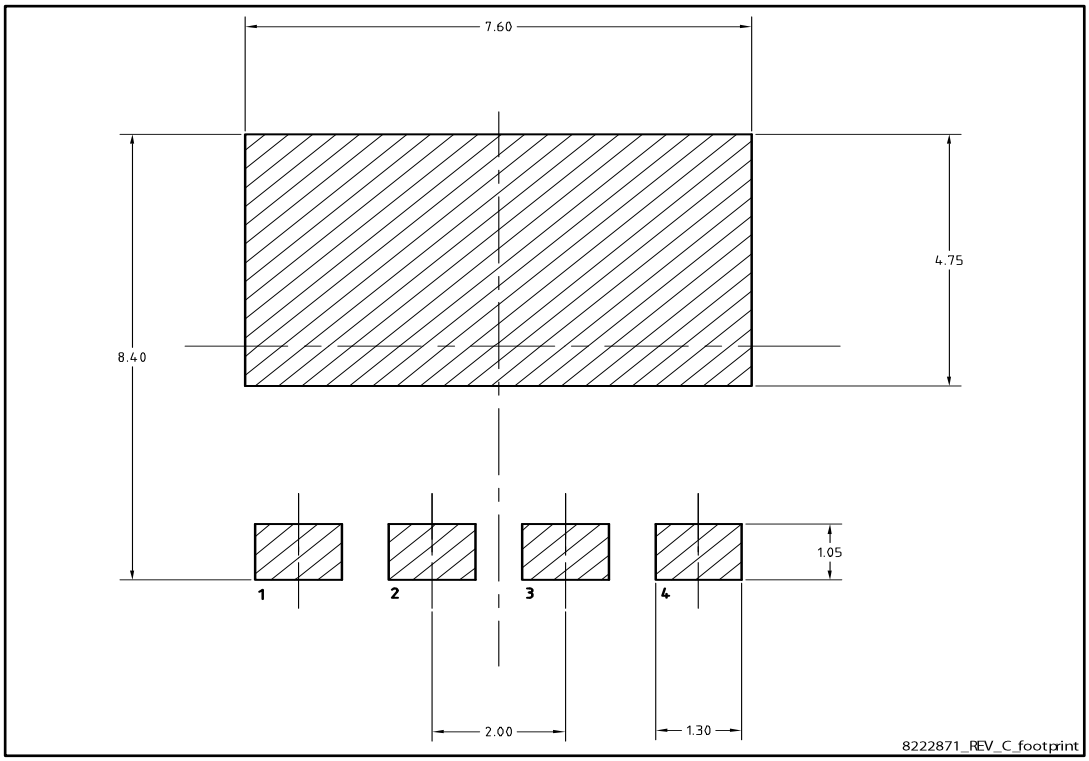


Table 8: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 21: PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

5.1 PowerFLAT™ 8x8 HV packaging mechanical data

Figure 22: PowerFLAT™ 8x8 HV tape

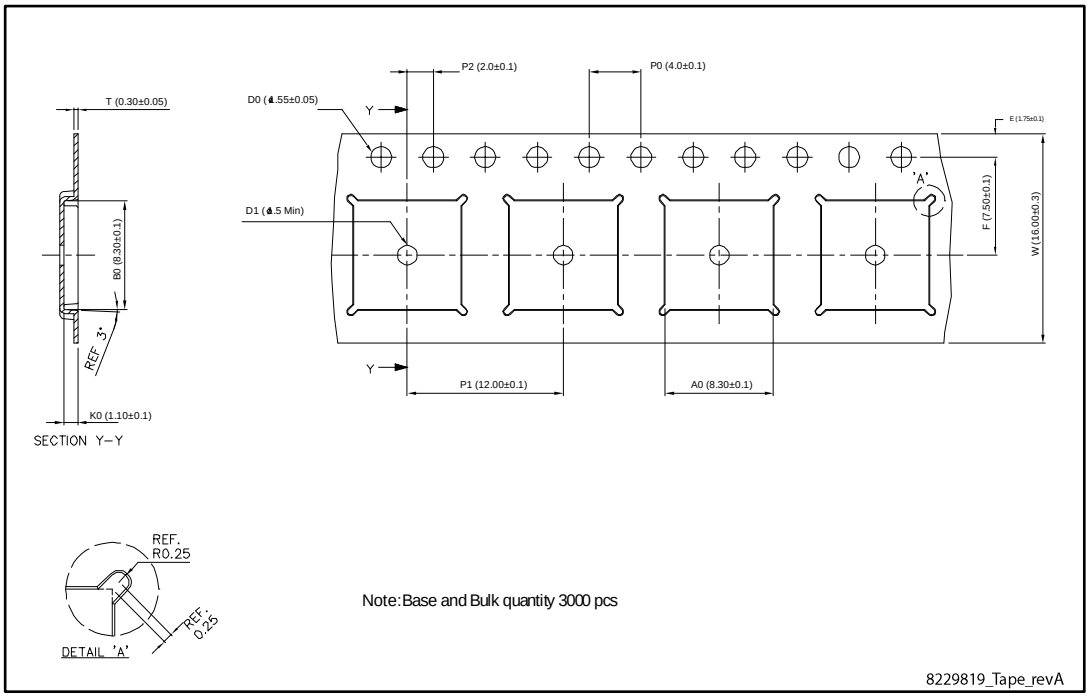


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape.

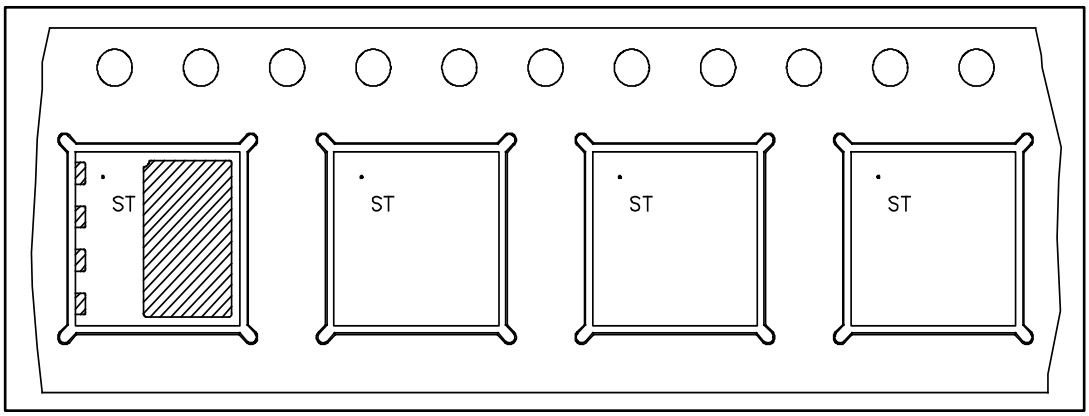
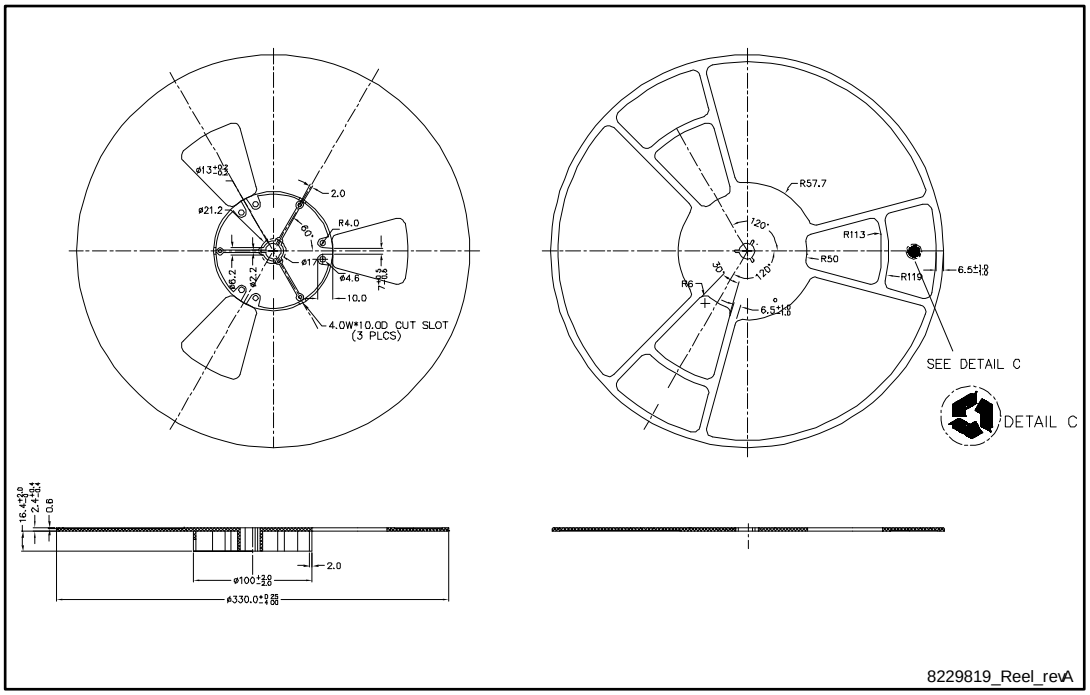


Figure 24: PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release.
23-Jul-2014	2	Updated the title, the features and the description in cover page. Document status promoted from preliminary data to production data. Updated *Figure 1: "Internal schematic diagram"*,*Section 1: "Electrical ratings"* , *Section 2: "Electrical characteristics"*. Added *Section 2.1: "Electrical characteristics (curves)"* Updated *Section 3: "Test circuits"*, *Section 4.1: "PowerFLAT™ 8x8 HV package mechanical data"*.

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