

STEVAL-IME003V1

STEVAL-IME003V1 demonstration board based on the STHV748 high voltage pulser

Data brief

Features

- 4-channel outputs: high voltage and low voltage BNC connectors
- Load simulator using signal equivalent circuits
- Possibility to set up own load simulator
- 16 preset waveforms
- USB connector to connect STM32 with PC and supply power to it
- 4 MB serial Flash memory to host FPGA code and waveforms
- Memory expansion connector to add external serial Flash
- Connectors to supply high voltage and low voltage to the STHV748 output stage
- LEDs to monitor the power management stage
- Human machine interface to select, start and stop the generation of the preset waveforms
- 25 LEDs to monitor board behavior
- RoHS compliant

Description

The STEVAL-IME003V1 demonstration board is designed around the STHV748 4-channel high voltage pulser, a state-of-the-art device designed for ultrasound imaging applications.

The output waveforms can be displayed directly on an oscilloscope by connecting the scope probe to the relative BNCs. 16 preset waveforms are available to test the HV pulser under varying conditions.



STEVAL-IME003V1

Schematic diagrams STEVAL-IME003V1

1 Schematic diagrams

NSD SS THSD_EN EN I DATAOUT[0:15] +VFPGA_IO_3V3 +VFPGA_CORE_1V2 ►HVM1 HVP1 FPGA_BLK HVP0 VDDM VDDP **♦** DVDD MCU_FPGA_PHOGAMCU_FPGA_MIT_B MCU_FPGA_MODEI FPGA_MCU_DONE MCU_FPGA_OSC_EN FPGA_MCU_AWAKE MCU_FPGA_SUSPEND USB_DP USB_DM ♦USB_DM USB_DISCONNECT USB_DISCONNECT STM32_FLASH_BLK BOARD_POWER MCU 3V3 € FLASH_3V3 FLASH_3V3 BOARD_POWER_BLK STM32_FLASH

Figure 1. STEVAL-IME003V1 hierarchical blocks

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J2 Details The S 2X(193-0564)
Phoenix Contact (Mfg Code MKDS 1.5/2-5.08) HIGH VOLTAGE LOW POWER HIGH VOLTAGE Phoenix Contact (Mfg Code MKDS 1.5/3-5.08) (Mfg Code MKDS 1.5/3-5.08) GND_SHIELD HVM1 HVM0 GND VDDP GND VDDM HVP1 HVP0 GND Σ ξ ≥ J3 Details: RS (193-0570) Phoenix Contact J1 Details RS (193-0570) R123 5 잌 ವ 22000n 16V C1, C2, C9, C10 Details: GND POWER Digikey (445-5217-2-ND) - TDK (CKG57NX7S2A226M) Package 6.5mm x 5.5 mm STHV748 Power Management C4, C5, C6 Details: Digikey (445-1436-2-ND) - TDK (C3225X5R1C226M) Package 1210 - EIA 3225 GND_POWER 9 16V HVM1 <u>Z</u>2000n 100√ 22000n 100V GND POWER \aleph 9 100 낊 # Pzygon 16V pzygon 16V GND ဗ 100 100 හි 5 >+VFPGA_CORE_1V2 22000n 100V 22000n 100V S VDDM DVDD A HVM HVM0 A HVP1 V MCU_3V3 2.2uH C14 Detail TDK (C2012X7R1A106K) - DIGIKEY (445-6857-2-ND) Dimension 0805 - EIA 2012 ·USB_DISCONNECT ·USB_DM ·USB_DP Ξ W 56 D L1 Detail TDK (VLF4012AT-2R2M1R5) - RS (614-3147) MCU Kingbright KP2012SURC RS: 466-3829 Farnell: 8529930 LED 0805 FB/Vo SΜ Power Management +VFPGA_IO_3V3 GND 5 USB_DISCONNECT FLASH_3V3 DigiKey (478-2552-2-ND) - AVX (TACL225M006XTA) Package 0603 క్ర Ä Ш C7 Details: Digikey (445-4998-2-ND) - TDK (C1005X5R0J105K) Package 0402 C13 4u7 6.3V 6DP USB ON U1 SOTT323-6L D26 RED 7 23 Grd 3.3V FPGA 3.3V 5 D2 D28 C12 and C13 Detail
TDK (C1608X5R0J475K) - Digikey (445-5178-2-ND)
Dimension 0603 - EIA 1608 R90 56R ⋛ 2 ON_1b COM_1b ON_2b USBDM 3 USB_DISCONNECT USBDP USB_3V3 C8 Details: C8 2.2uF 6.3V NOT ASSEMBLY RS (515-1995) Molex (54819-0572) 4 J4 Details Y Phoenix Contact (Mfg Code MPT 0.5/2-2.54) RS (220-4260) ON_1a LDS3985M33R C12 4u7 6.3V COM_1a MMS228 USB_miniB EXT_3V3 ON_2a O nc GND SHELL SHELL SHELL SHELL VBUS DM DP L O SND ပ SW1 Details: SW1 MI RS 711-8329 KNITTER-SWITCH (MMS228T) ន 4 កក HNI 3 BYPS 33nF 2 Ζ DP D 3V3 Connector FLASH_3V3 Ξ₹ USB_3V3 EXT_3V3 USB_5V USB_5V USB AM010079v1

Figure 2. STEVAL-IME003V1 FPGA bank 0 configuration

STEVAL-IME003V1 Schematic diagrams

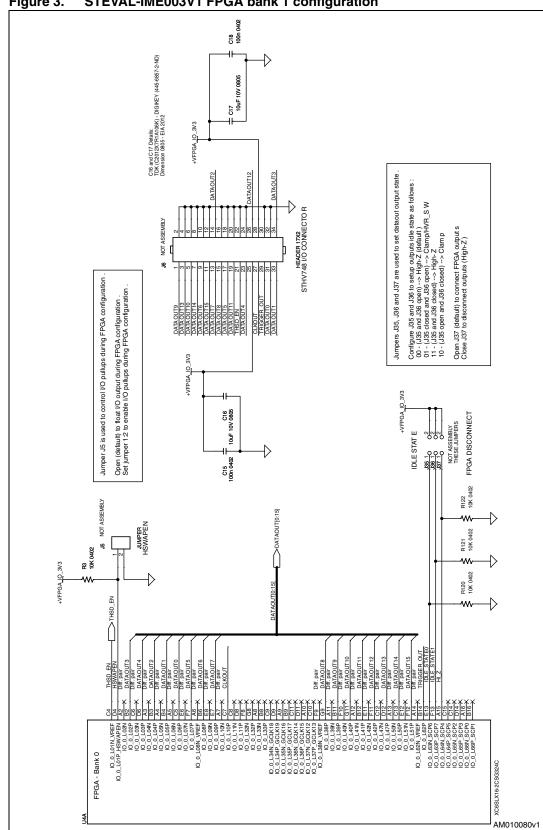


Figure 3. STEVAL-IME003V1 FPGA bank 1 configuration

R5 10K 0402 R9 10K 0402 ERROR signal IDLE SW PUSHBUTTON-DPST 22 100nF C24 100nF R12 WW 56R 0402 ξξ € \$ R4 10K 0402 R8 10K 0402 **PUSHBUTTONS** C23 100nF CTRL LED C26, C27, C30 and C31 Detail
HEADER 6X2 TDK (C2013X7R1A106K) - DIGIKEY (445-6857-2-ND)
Dimension 0805 - ElA 2012 C28 100nF 282 100nF 020 10n 1 C19 100nF 8 C31 10uF 10V 0805 : GND GND 66MHZ EXTERNAL OSCILLATOR PERIPHERRAL MODULE (PMOD) 9 9 C26 10uF 10V 0805 C30 10uF 10V 0805 PMOD1 PMOD2 š ă C25 100nF C29 100nF BACKUP OF U5 Voc OE ST WCU_FPGA_OSC_EN FPGA USER I/O NOT ASSEMBLY FPGA - Bank 1

STEVAL-IME003V1 FPGA bank 2 configuration Figure 4.

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Figure 5. STEVAL-IME003V1 FPGA bank 3 configuration PROG 13 \$ 82 PROG 4 D14 YELLOW PROG 5 D16 YELLOW PROG 3 £ ₹ ₹ ≩ R39 NA 0402 R40 NA 0402 MCU_FPGA_MODE1 MCU_FPGA_INIT_B SPI MISO1 SPI MISO1 SPI SEL SPI SEL SPI MISO2 SPI MISO3 FPGA PROG R18 2K43 0402 DNP C33 Details: TDK (C2012X7F14 106K) - DIGIKEY (445-6857 2-ND) Dimension 0805 - EIA 2012 R22 2K43 0402 When FPGA_INIT_8 (hidrectional open-drain) is Low the configuration and open-drain of search.

When held Low, the start of configuration is delayed.

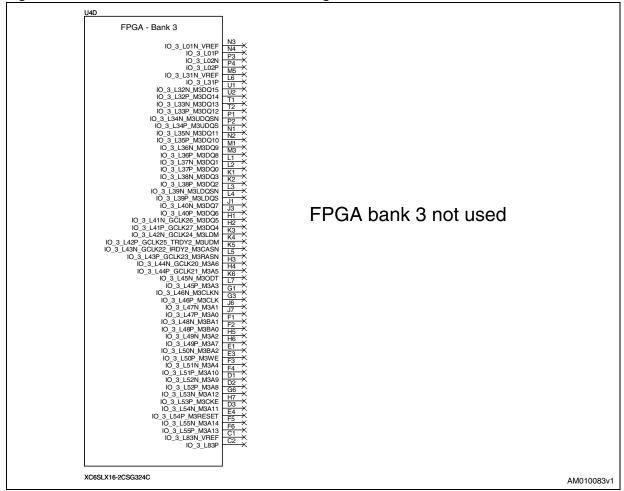
When red Low, the start of configuration is delayed. 100 F ₩ 0402 DNP R17 2K43 0402 55 84 84 10 E Place R38 close to the FPGA device Configuration mode selection: FPGA_MODE0 = Parallel (Low) or Serial (High) FPGA_MODE1 = Master (Low) or Slave (High) SPI FLASH CTRL SIGNALS FPGA CONFIGURATION +VFPGA_IO_3V3 R16 10K 0402 R38 CON 10 R127 5 EXT SPI FLASH 9 SPI EXTERNAL PROGRAMMING HEADER ₹ <u>₹</u> ∏ -FPGA_SPI_MISO3 0.2.143 N.0.2.143 N.0.2.14 D 2 LON NO CORPORED

O 2 LOS VORPORED

O 3 LOS V FPGA - Bank 2

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Figure 6. STEVAL-IME003V1 FPGA bank 3 configuration



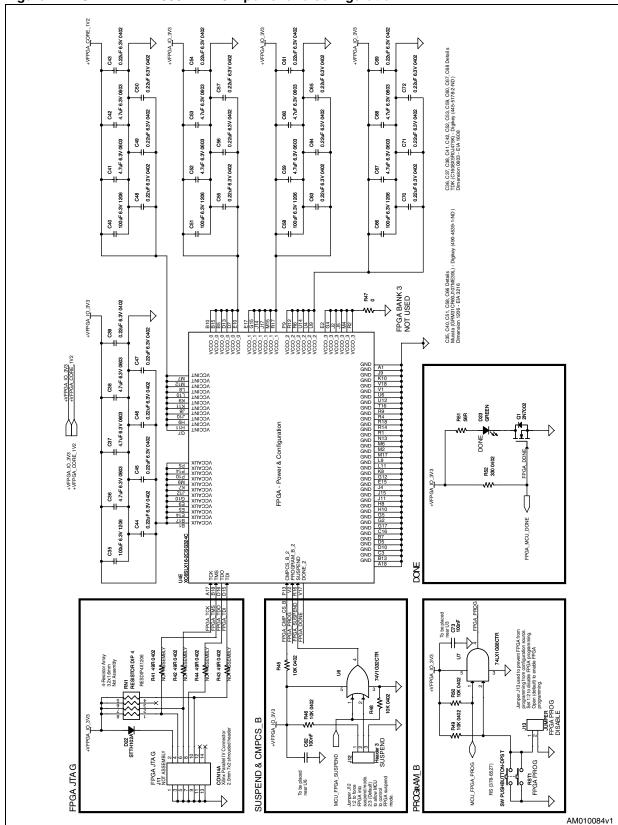


Figure 7. STEVAL-IME003V1 FPGA power and configuration

C77, C80, C111, C112 Detaib Digikey (490-1462-2-ND) Murata (GRM188R72A271KA01D) J16, J17, J22, J23, J25, J26, J29 and J30 Details Tyco Electronics (1-1337482-0) - RS (420-5401) D1, D2, D3, D4, D5, D6, D7, D8 diode DFLS1200 rs-code 708-2334 J16, J17, J22, J23, J25, J26, J29 and J30 Detail Tyco Electronics (1-1337482-0) - RS (420-5401) 759 100k ₹ 1 2 8 3 4 -w ₹ C91 HE H C101 88 20p 0805 20p 0805 HVM0 HVM1 POINT C75 C115 통류□ STHV748 8 <u></u> § - Pig sg XDCR_C BZS J15 82S J19 ES 128 ES 132 ES 134 N3C HVP0_D HVP0 D3E A DFLS1200 N1_D IN2 D IN2_C IN3 D IN3_C MDDM HS & S VDDM GNDPW XDCR_D XDCR_C HVM0 LVOUT D LVOUT_C LVOUT_A D31 KDFLS1200 D33 VDFLS1200 LVOUT_B BNC Das Pofls1200 XDCR_B • C78 220n C108 220n ⌽ 22 GNDPW VDDF VDDP IN3_A IN3_B IN2_B NZA A HVOUT_B HVM0_B HVM1_B 2 0 0 1 828 JI8 HVP1_B 2 0 0 1 B2S J14 -IVM1-A -TVOVF HVM0_A D_CTRL XDCR_B 88 20p 0805 S S -**⊕**≌ ≅ 20p 0805 19 19 19 19 C74 8 19 19 C114 1000 0603 88 80 C100 220n 80 N/A C110 Hos Soll NA Be ¥83 THSD_EN THSD_EN AM010050v1

Figure 8. STEVAL-IME003V1 configuration of the STHV748

OSCILLATOR FLASH READY RESET# Male Connector 2x5 Pitch 1.27 mm SAMTEC FTSH-105-01-F-D-K STM32F103 FLASH_3V3 JUMPER ₹ 5 ₩ ₩ MCU_3v3 PC14-OSC32_IN PC15-OSC32_OUT PC13-Tamper-RTC _ 6 3 VDDA BOOT0 PB2-BOOT1 JTAG/SW D MCU NRST RESET# Use J38 to enable/disable power for SPI flash device. J38 must be open when using external spi flash device on connecto J10. Default value dosed. INT SPI FLASH 200 C123 8H// FLASH DISABLE C123 Details: Digikey (445-4998-2-ND) - TDK (C1005X5R0J105K) Package 0402 R128 26 OPTIONAL FPGA CONFIGURATION SIGNAL S ğ - N vss H64 1131 C116 1 **OPTIONAL FPGA I/O** SPI FLASH

Figure 9. STEVAL-IME003V1 configuration of the STM32



AM010051v1

STEVAL-IME003V1 Revision history

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
11-Aug-2011	1	Initial release.

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