



**CHILIN TECHNOLOGY CO., LTD.**

## Product Specifications

<b>Customer</b>	
<b>Description</b>	<b>5.7" TFT LCD Module</b>
<b>Model Name</b>	<b>LQ057AC111</b>
<b>Date</b>	<b>2007/01/24</b>
<b>Doc. No.</b>	
<b>Revision</b>	<b>12</b>

<b>Customer Approval</b>	
<b>Date</b>	
The above signature represents that the product specifications, testing regulation, and warranty in the specifications are accepted	

<b>Engineering</b>			
<b>Check</b>	<b>Date</b>	<b>Prepared</b>	<b>Date</b>

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## RECORD OF REVISIONS

Revision	Date	Page	Description
00	2006/04/13	all	New Creation
01	2006/06/06	18	Viewing angle
02	2006/06/08	5	VCOM Voltage
03	2006/06/14	27	Add: Quality Assurance
04	2006/06/20	30	Add: Precaution
05	2006/06/23	6,29	Add: LED_B/L schematic; Packing
06	2006/06/30	26	Change: Cable length & color; Add: FPC thickness
07	2006/07/26	19	Modify: Optical Characteristics
08	2006/09/04	5 5 16	Add: Operating current Modify: Power Sequence Modify: SPI timing interface definition
09	2006/11/09	26	Modify: Outline Drawing
10	2006/11/24	7 8-21 29	AC Characteristics Waveform OUTLINE DRAWING
11	2006/12/04	5	ELECTRICAL CHARACTERISTICS
12	2007/01/23	6	DC CHARACTERISTICS

## 1. SUMMARY

This technical specification applies to 5.7" color TFT-LCD panel. The 5.7" color TFT-LCD panel is designed for industry, vehicle application and other electronic products which require high quality flat panel displays. This module follows RoHS.

## 2. FEATURES

High Resolution: 230,400 Dots (320 RGB x 240). Image Reversion: Up/Down and Left/Right.

## 3. GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen size		5.7(Diagonal)	inch
Display Format		320 RGB x 240	Dot
Active area		115.25(H) x 86.4(V)	mm
Pixel size		120 x 360	um
Surface treatment		Anti-glare	
Pixel Configuration		RGB-Stripe	
Outline dimension		126.00(W) x 101.55(H) x 5.70(D)	mm
Weight		(85)	g
View Angle direction		6 o'clock	
Temperature Range	Operation	-20~70	°C
	Storage	-30~80	°C

## 4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power Voltage	VDD,AVDD	GND=0	-0.3	7.0	V	
	V <sub>GH</sub>	GND=0	-0.3	32.0	V	
	V <sub>GL</sub>	GND=0	-22.0	0.3	V	
	V <sub>GH</sub> -V <sub>GL</sub>	GND=0	-0.3	+45.0	V	
Input Signal Voltage	V <sub>in</sub>	GND=0	-0.3	VDD+0.3	V	
Logic Output Voltage	V <sub>OUT</sub>	GND=0	-0.3	+0.7	V	

Note : Device is subject to be damaged permanently if stresses beyond those absolute Maximum ratings listed above

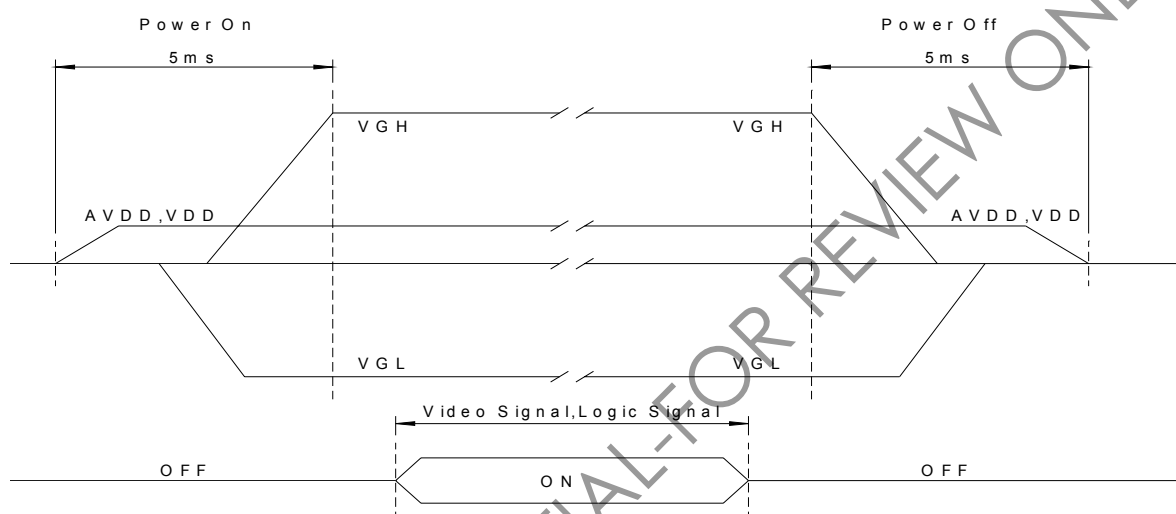
## 5. ELECTRICAL CHARACTERISTICS

### 5.1. Operating conditions:

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Voltage	VDD	3.0	3.3	3.6	V	
	AVDD	3.8	5	5.5	V	
	VGH	10	-	30	V	
	VGL	-17	-	-5	V	

### 5.2 Power Sequence

Sequence for power on/off and Signal on/off



Note 1: AVDD, VDD, VGH and VGL could be OFF at the same time within the designated period (5ms).

To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

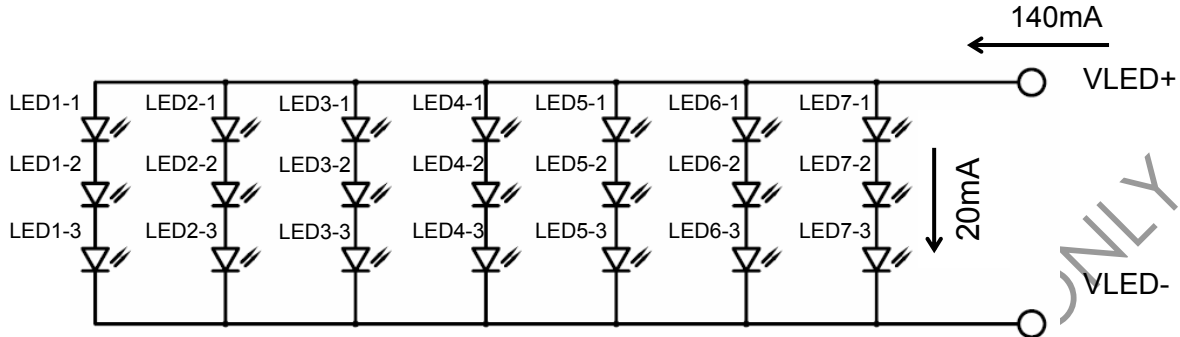
Power ON : AVDD, VDD → VGL → Input Signals → VGH

Power OFF : VGH → Input Signals → VGL → AVDD, VDD

### 5.3 LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	$I_{LED}$		140	210	mA	Note 1
LED voltage	$V_{LED}$	9.9	-	10.5	V	
LED Life Time	-	(10,000)	-	-	Hr	Note 2,3

Note 1: There are 7 Groups LED shown as below,  $V_{LED}=9.9V$  (min.).



Note 2:  $T_a = 25^\circ C$ ,

Note 3: Brightness to be decreased to 50% of the initial value.

### 6. DC CHARACTERISTICS

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Low level input voltage	$V_{IL}$	0	-	0.3 VDD	V	SPCL, SPDA, UD, LRC, IF1, IF2
Hight level input voltage	$V_{IH}$	0.7 VDD	-	VDD	V	
Analog operating current	$I_{AVDD}$	-	(7)	(12)	mA	AVDD=5V
Digital operating current	$I_{VDD}$	-	(5)	(8)	mA	VDD=3.3V
Gate voltage "H" level current	$I_{VGH}$	-	-	(100)	$\mu A$	VGH=15V
Gate voltage "L" level current	$I_{VGL}$	-	-	(100)	$\mu A$	VGL=-10V
VCOM High Voltage	VcomH	4	4.6	5.2	V	Note1
VCOM Low Voltage	VcomL	-1.4	-0.8	-0.2	V	Note1

Note 1: VcomH & VcomL : Adjust the color with gamma data.

## 7. AC CHARACTERISTICS

### 7.1 Input signal characteristics

#### 7.1.1 Digital Parallel RGB interface

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
CLK period		T <sub>osc</sub>	-	156	-	ns
Data setup time		T <sub>su</sub>	12	-	-	ns
Data hold time		T <sub>HD</sub>	12	-	-	ns
IHS period		T <sub>H</sub>	-	408	-	T <sub>osc</sub>
IHS pulse width		T <sub>HS</sub>	5	30	-	T <sub>osc</sub>
IHS setup time		T <sub>Cr</sub>	12	-	-	ns
IHS hold time		T <sub>Cf</sub>	12	-	-	ns
IVS pulse width		T <sub>VS</sub>	1	3	5	T <sub>H</sub>
IVS setup time		T <sub>Vr</sub>	12	-	-	ns
IVS hold time		T <sub>Vf</sub>	12	-	-	μs
IVS-DEN time	NTSC	T <sub>VSE</sub>	-	18	-	T <sub>H</sub>
	PAL	T <sub>VSE</sub>	-	26	-	T <sub>H</sub>
IHS-DEN time		T <sub>HE</sub>	36	68	88	T <sub>osc</sub>
DEN pulse width		T <sub>EP</sub>	-	320	-	T <sub>osc</sub>
DEN-STH time		T <sub>DES</sub>	-	1	-	T <sub>osc</sub>
IVS period	NTSC	-	-	262.5	-	T <sub>H</sub>
	PAL	-	-	312.5	-	T <sub>H</sub>

Note: When SYNC mode is used, 1<sup>st</sup> data start from 68<sup>th</sup> CLK after IHS falling.

#### 7.1.2 CCIR601/656 Interface

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
CLK period		T <sub>OSC</sub>	-	37	-	ns
Data setup time		T <sub>SU</sub>	12	-	-	ns
Data hold time		T <sub>HD</sub>	12	-	-	ns

#### 7.1.3 Hardware reset timing

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
RESET low pulse width		T <sub>RSB</sub>	10	-	-	μs

**7.2. Output signal characteristics for Digital input signal**

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Rising time	$T_r$	-	-	10	ns
Falling time	$T_f$	-	-	10	ns
Internal STH setup time	$T_{SUS}$	12	-	-	ns
Internal STH hold time	$T_{HDS}$	12	-	-	ns
Internal data setup time	$T_{SUD}$	60	-	-	ns
Internal data hold time	$T_{HDD}$	40	-	-	ns
OEH pulse width	$T_{OEH}$	-	1248	-	ns
OEV pulse width	$T_{OEV}$	-	4992	-	ns
CKV pulse width	$T_{CKV}$	-	3744	-	ns
Hsync – DEH time	$T_1$	-	4368	-	ns
Hsync – CKV time	$T_2$	-	2496	-	ns
Hsync – OEV time	$T_3$	-	624	-	ns
Hsync – POL time	$T_4$	-	4368	-	ns
Vsync – setup time	$T_{SUV}$	-	1872	-	ns
Vsync – pulse time	$T_{STV}$	-	1	-	$T_H$
Vsync – STV time	NTSC	-	19	-	$T_H$
	PAL	-	27	-	$T_H$
OEH – STV time	$T_{HE}$	-	2	-	$T_H$
Output settling time	$T_{OES}$	-	12	20	$\mu s$

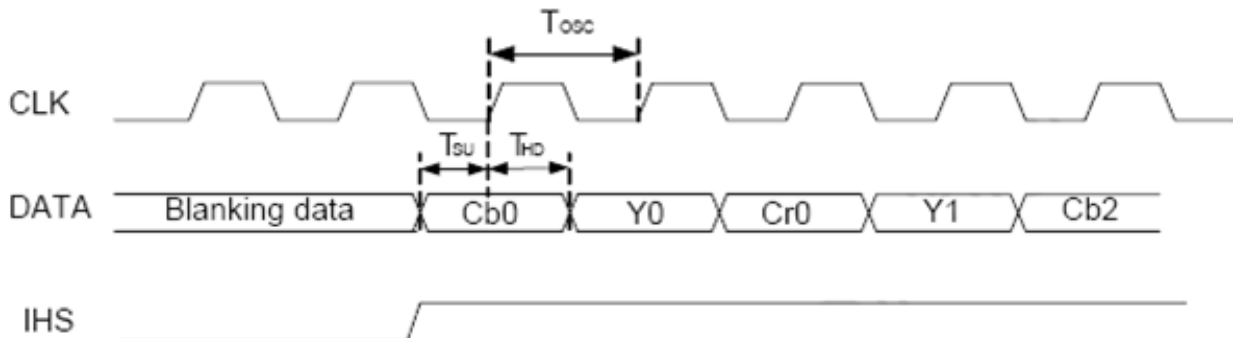
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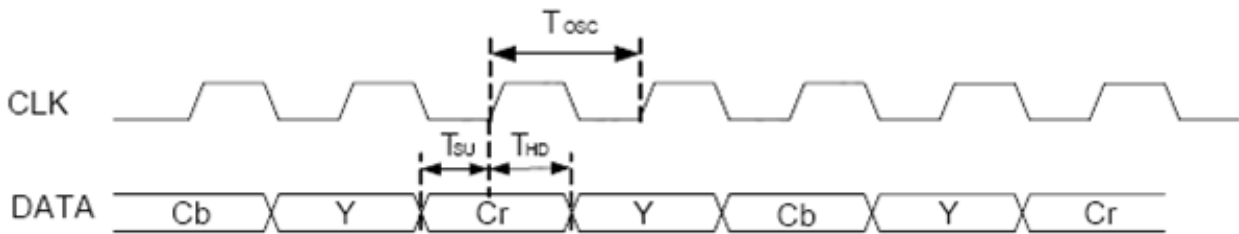
### 7.3 Waveform

#### 7.3.1 Timing Controller Timing Chart

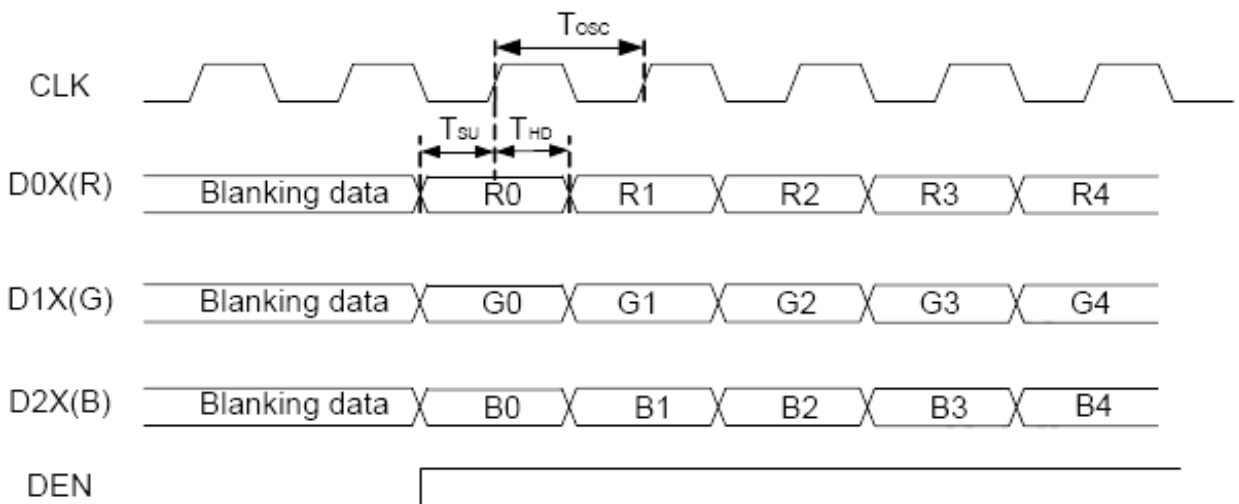
##### 7.3.1.1 Clock and Data waveform



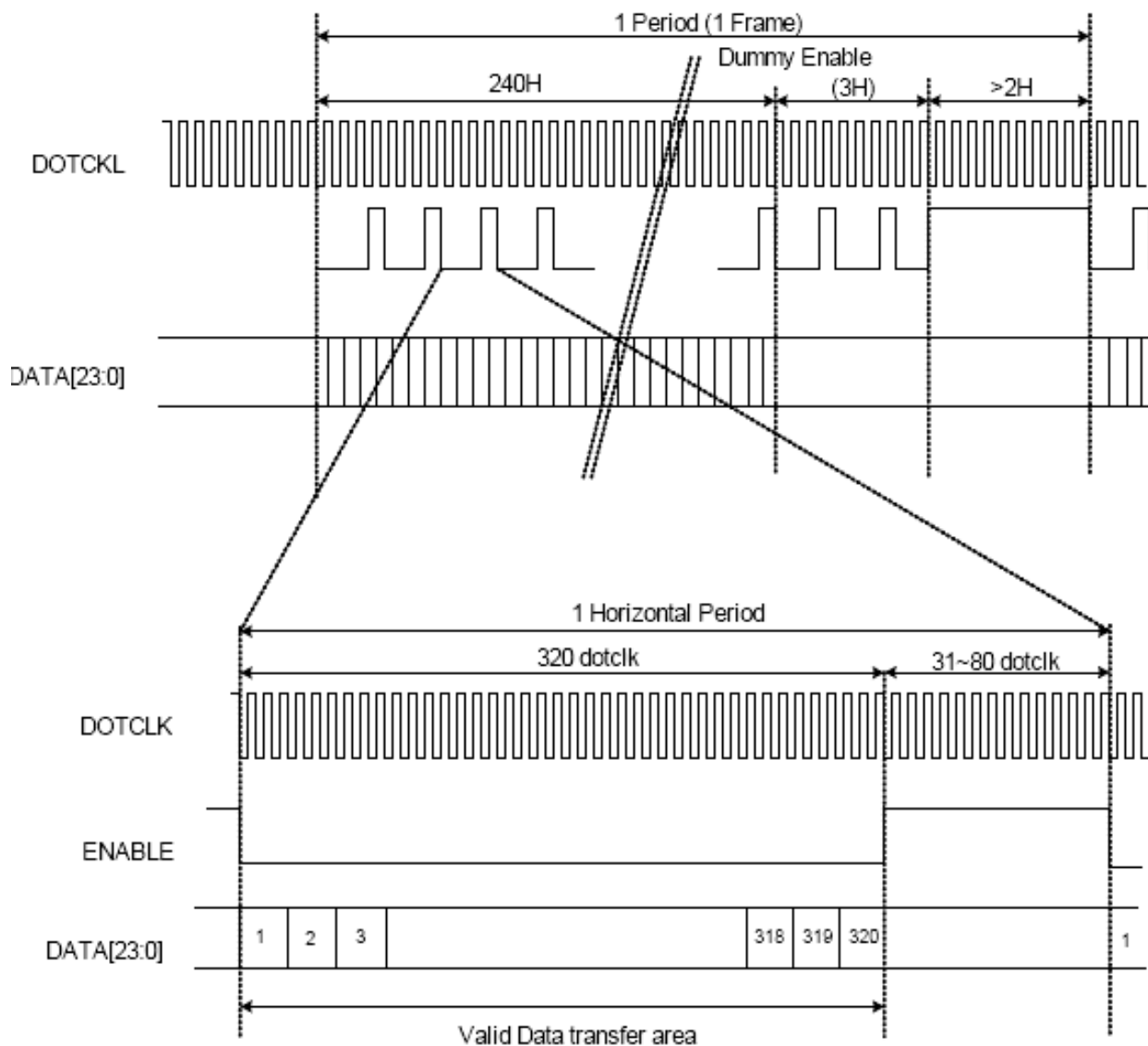
#### ●CCIR656



#### ●Digital Parallel RGB

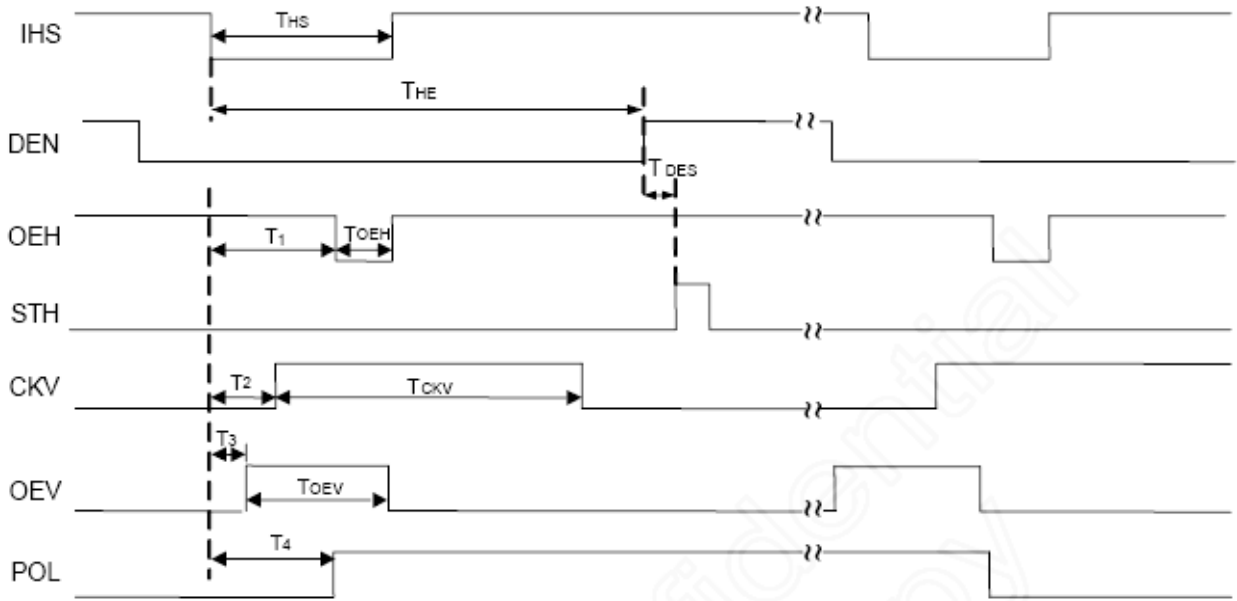


7.3.1.2 Digital RGB timing waveform  
7.3.1.2.1 DE Only Mode

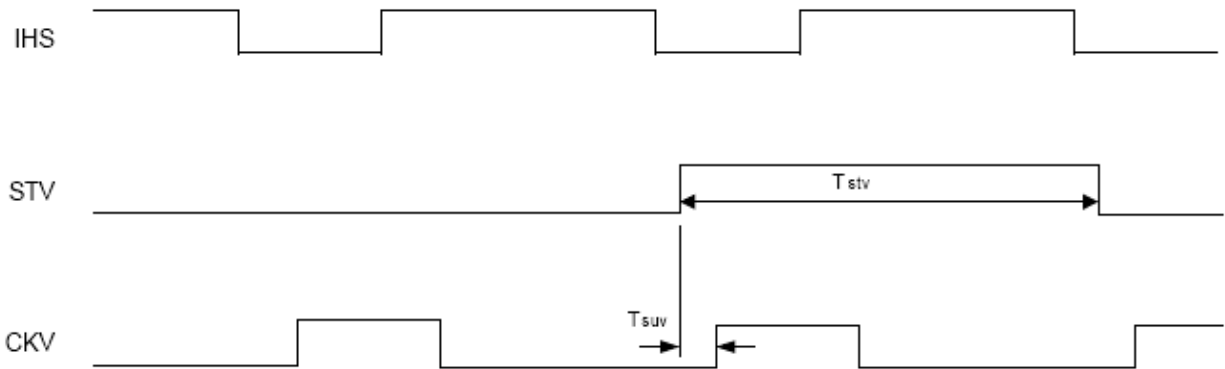


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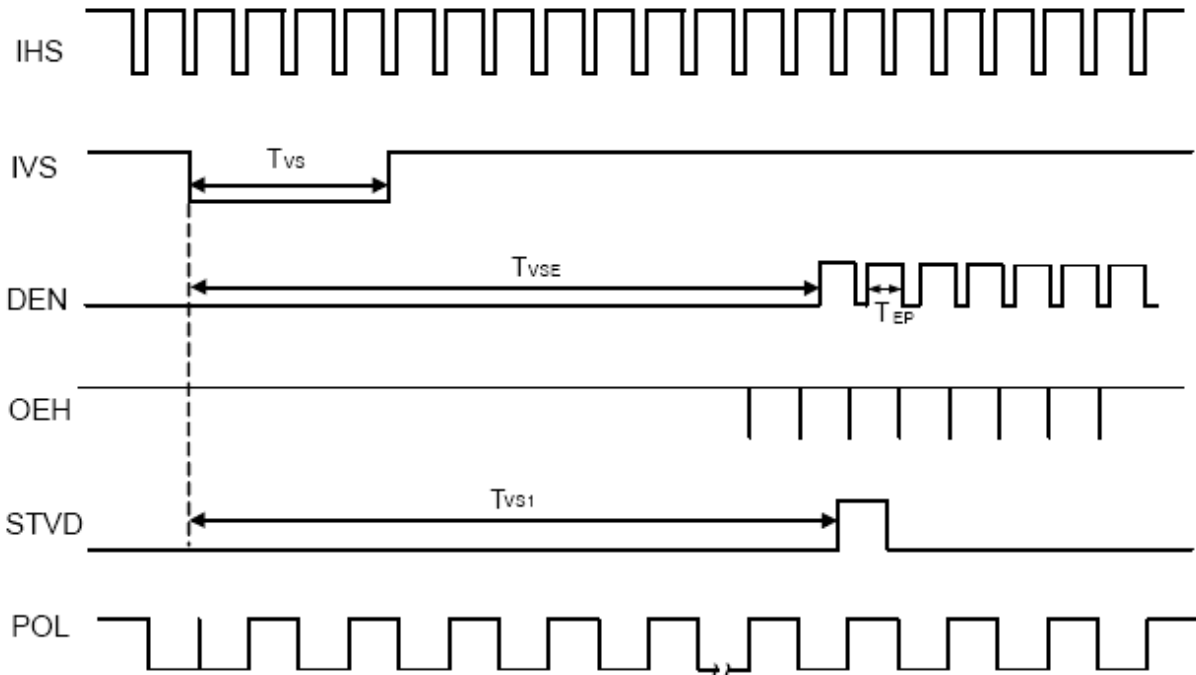
7.3.1.2.2 IHS and horizontal control timing waveforms



7.3.1.2.3 IHS and vertical shift clock timing waveforms



7.3.1.2.4 IHS and vertical control timing waveforms

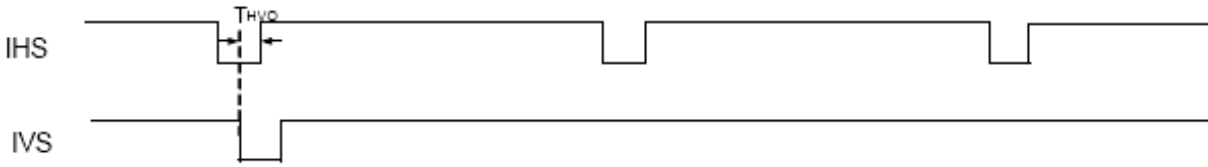


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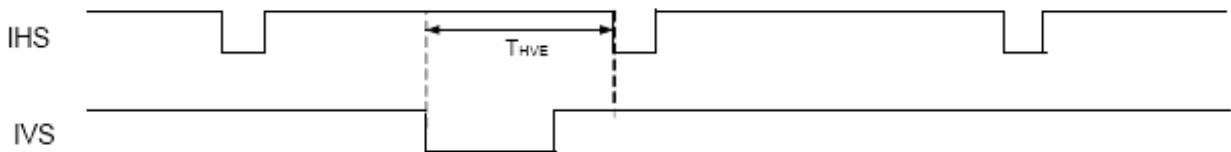
7.3.1.3 CCIR601 timing waveform VS\_POL=H, HS\_POL=L in Register R2)

7.3.1.3.1 IHS and IVS timing

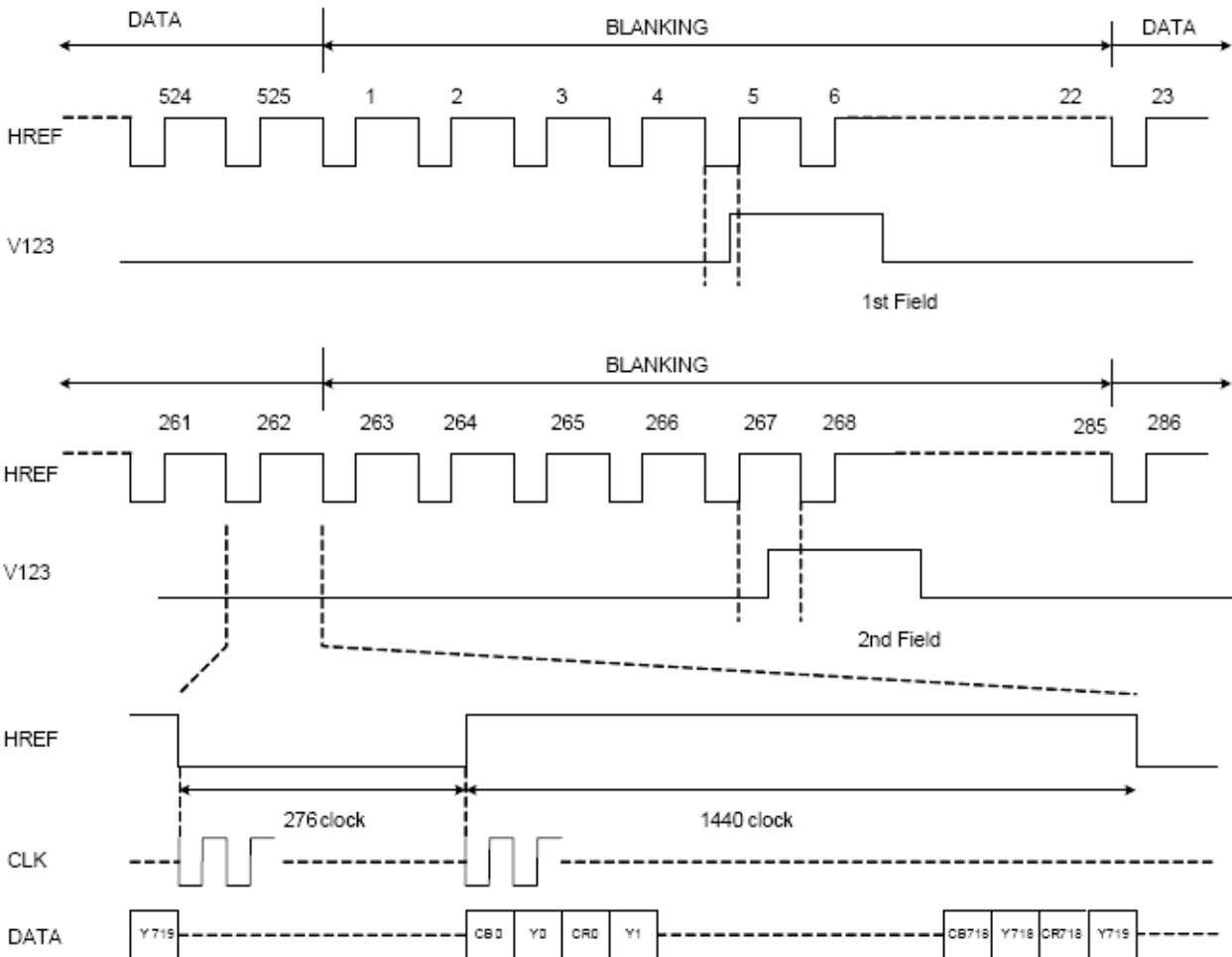
● Odd field

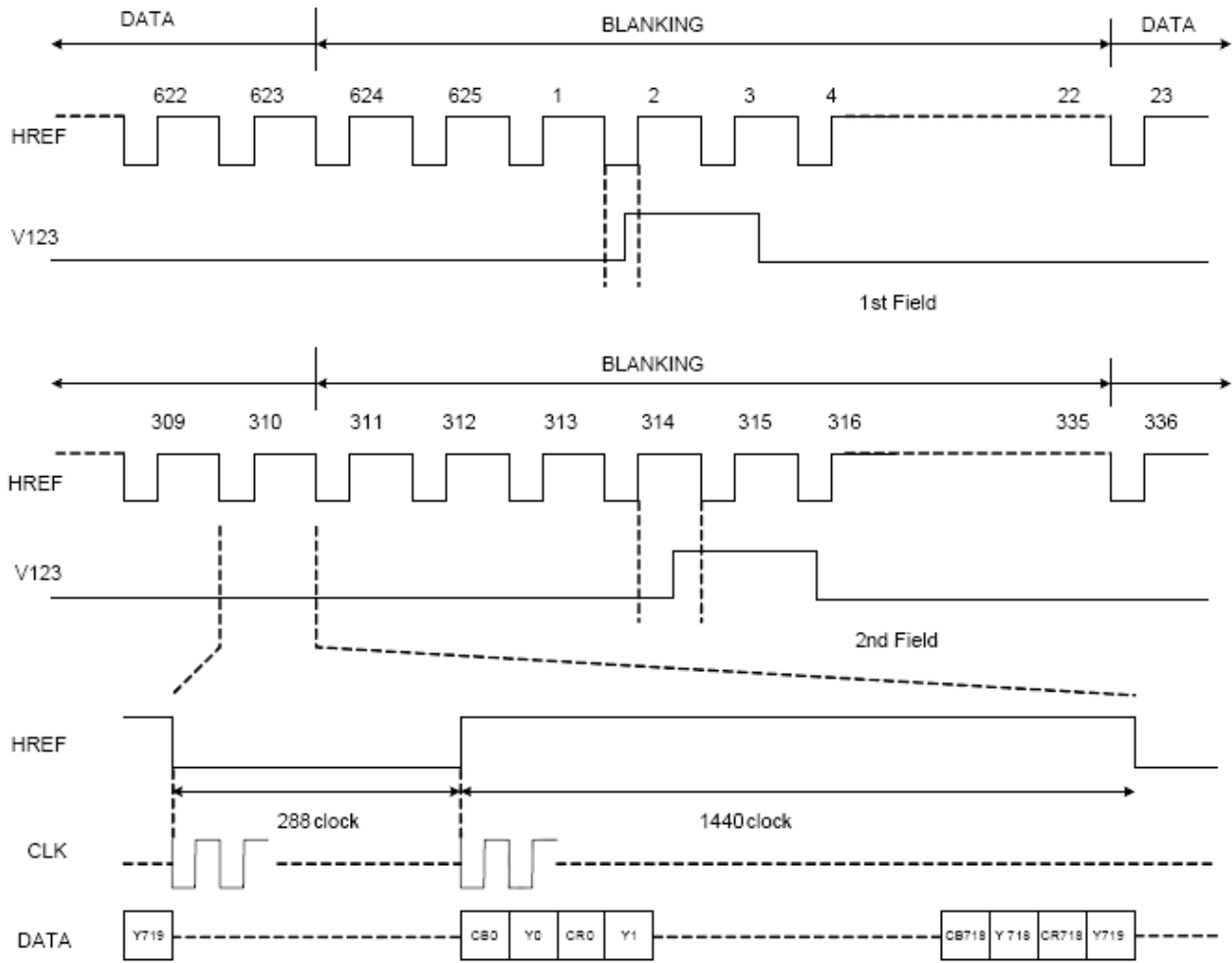


● Even field



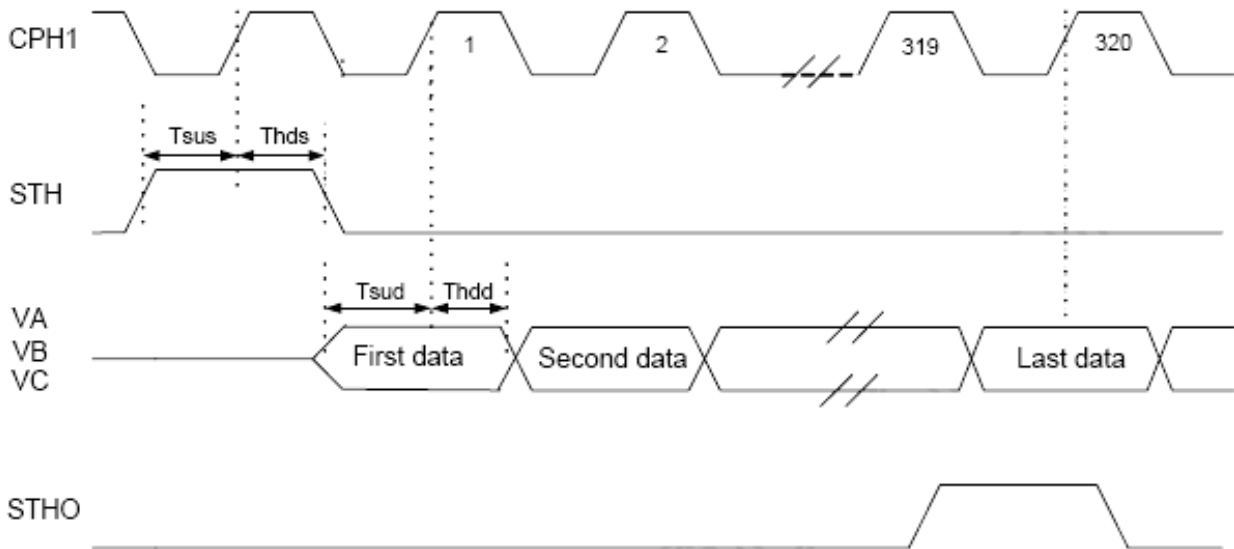
7.3.1.3.2 IHS and IVS timing



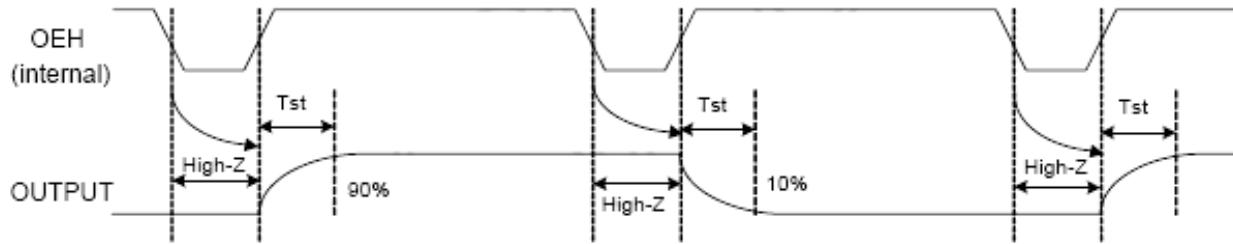


### 7.3.2 Source Driver Timing Chart

#### 7.3.2.1 Clock and Start Pulse timing waveform



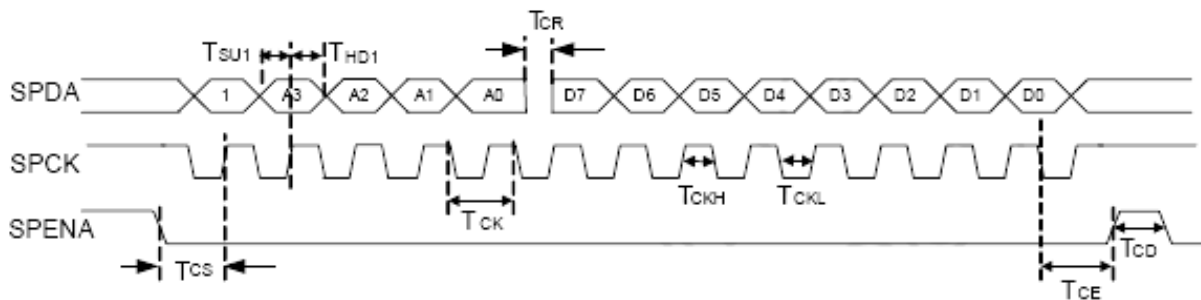
### 7.3.2.2 OEH and Data Output timing waveform



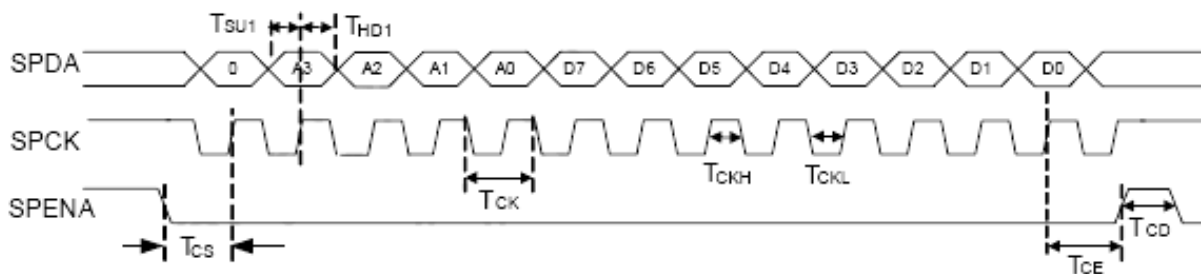
### 7.3.3 SPI timing characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SPCK period	$T_{CK}$	60	-	-	ns
SPCK high width	$T_{CKH}$	30	-	-	ns
SPCK low width	$T_{CKL}$	30	-	-	ns
Data setup time	$T_{SU1}$	12	-	-	ns
Data hold time	$T_{HD1}$	12	-	-	ns
SPENA to SPCK setup time	$T_{CS}$	20	-	-	ns
SPENA to SPDA hold time	$T_{CE}$	20	-	-	ns
SPENA high pulse width	$T_{CD}$	50	-	-	ns
SPDA output latency	$T_{CR}$		1/2	-	$T_{CK}$

#### ● SPI read timing



#### ● SPI read timing



## 7.3.4 SPI Register Description

## ● Register R0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	STHD1	STHD0	STHP4	STHP3	STHP2	STHP1	STHP0
Default	0	0	0	0	0	0	0	0

STHD [1:0]: adjust start pulse position by dot. (RGB mode only)

STHD1	STHD0	STH position adjust by dot
1	1	-1
1	0	-2
0	0	0
0	1	+1

STHP [4:0]: adjust start pulse position by pixel

STHP4	STHP3	STHP2	STHP1	STHP0	STH position adjust by pixel
1	1	1	1	1	-1
1	1	1	1	0	-2
1	1	1	0	1	-3
1	1	1	0	0	-4
1	1	0	1	1	-5
1	1	0	1	0	-6
1	1	0	0	1	-7
1	1	0	0	0	-8
1	0	1	1	1	-9
1	0	1	1	0	-10
1	0	1	0	1	-11
1	0	1	0	0	-12
1	0	0	1	1	-13
1	0	0	1	0	-14
1	0	0	0	1	-15
1	0	0	0	0	-16
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	0	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15



## ●Register R1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STVP3	STVP2	STVP1	STVP0	STVNT1	STVNT0	STVPAL1	STVPAL0
Default	0	0	0	0	0	0	0	0

STVP [3:0]: adjust first line position by line

STVP3	STVP2	STVP1	STVP0	STH position adjust by pixel
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7
1	0	0	0	-8
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7

STVNT[1:0]: Adjust the relationship of first line of active video in Odd/Even Field in NTSC mode.

00: The first line of active video in Even Field = The first line of active video in Odd Field

01: The first line of active video in Even Field = The first line of active video in Odd Field + 1

10: No Use

11: The first line of active video in Even Field = The first line of active video in Odd Field - 1

STVPAL[1:0]: Adjust the relationship of first line of active video in Odd/Even Field in PAL mode.

00: The first line of active video in Even Field = The first line of active video in Odd Field

01: The first line of active video in Even Field = The first line of active video in Odd Field + 1

**●Register R2**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LPF	RGBVPOL	OEHCTL	OVER	VS_POL	HS_POL	NPC_IN	NPC_SET
Default	1	0	1	0	1	0	1	0

LPF: Low pass filter function enable/disable in CCIR656/CCIR601 mode

LPF="L", Low pass filter function disable

LPF="H", Low pass filter function enable

RGBVPOL: RGB mode VS polarity setting

RGBVPOL ="L", negative polarity.

RGBVPOL ="H", positive polarity

OEHCTL: OEH signal control in PAL mode

OVER: Sets display period in ITU-R BT. 656 or 601 modes.

0 => 50.3us of active data is displayed on the panel.

1 => 53.3 us of active data is displayed on the panel.

VS\_POL: VS polarity setting.

VS\_POL=L, negative polarity.

VS\_POL=H, positive polarity.

HS\_POL: HS polarity setting.

HS\_POL=L, negative polarity.

HS\_POL=H, positive polarity.

NPC\_IN: Define the NTSC/PAL mode by SPI.

NPC\_IN=L, PAL.

NPC\_IN=H, NTSC.

NPC\_SET: Set the NTSC/PAL auto detection or define by NPC\_IN.

NPC\_SET=L, auto detection.

NPC\_SET=H, define by NPC\_IN.

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## ●Register R3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTO_DP	DISP_ON	A_TIME	A_TIME0	reserved	POL_OUT	DE_POL	DE_SEL
Default	1	0	0	1	0	0	0	0

AUTO\_DP: When power on, select black image display time decided by A\_TIME (bit5, 4) or DISP\_ON (bit6).

AUTO\_DP = "L", Black image display time decided by DISP\_ON (bit6).

AUTO\_DP = "H", Black image display time decided by A\_TIME (bit5, 4).

DISP\_ON: When AUTO\_DP (bit7) = "L", and DISP\_ON = "H", black image display off, then display normal image.

A\_TIME: When AUTO\_DP (bit7) = "H", the black image display time is decided by A\_TIME

00: black image display time is 0.166s (10 fields)

01: black image display time is 0.332s (20 fields)

10: black image display time is 0.664s (40 fields)

11: black image display time is 1.328s (80 fields)

POL\_OUT: POL phase select

POL\_OUT=L, POL and VCOM are in phase.

POL\_OUT=H, POL and VCOM are reverse.

DE\_POL: DE signal polarity setting.

When DE\_SEL=L:

DE\_POL =L, positive polarity.

DE\_POL =H, negative polarity.

When DE\_SEL=H:

DE\_POL =L, negative polarity.

DE\_POL =H, positive polarity.

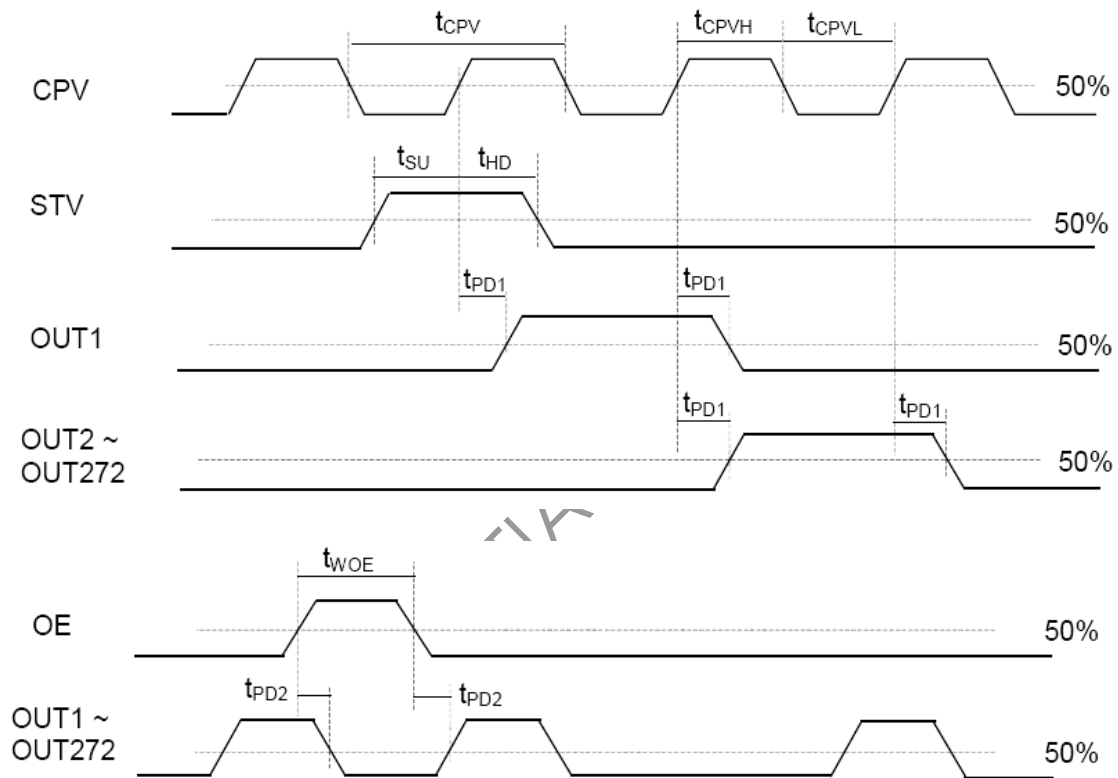
DE\_SEL: DE mode select.

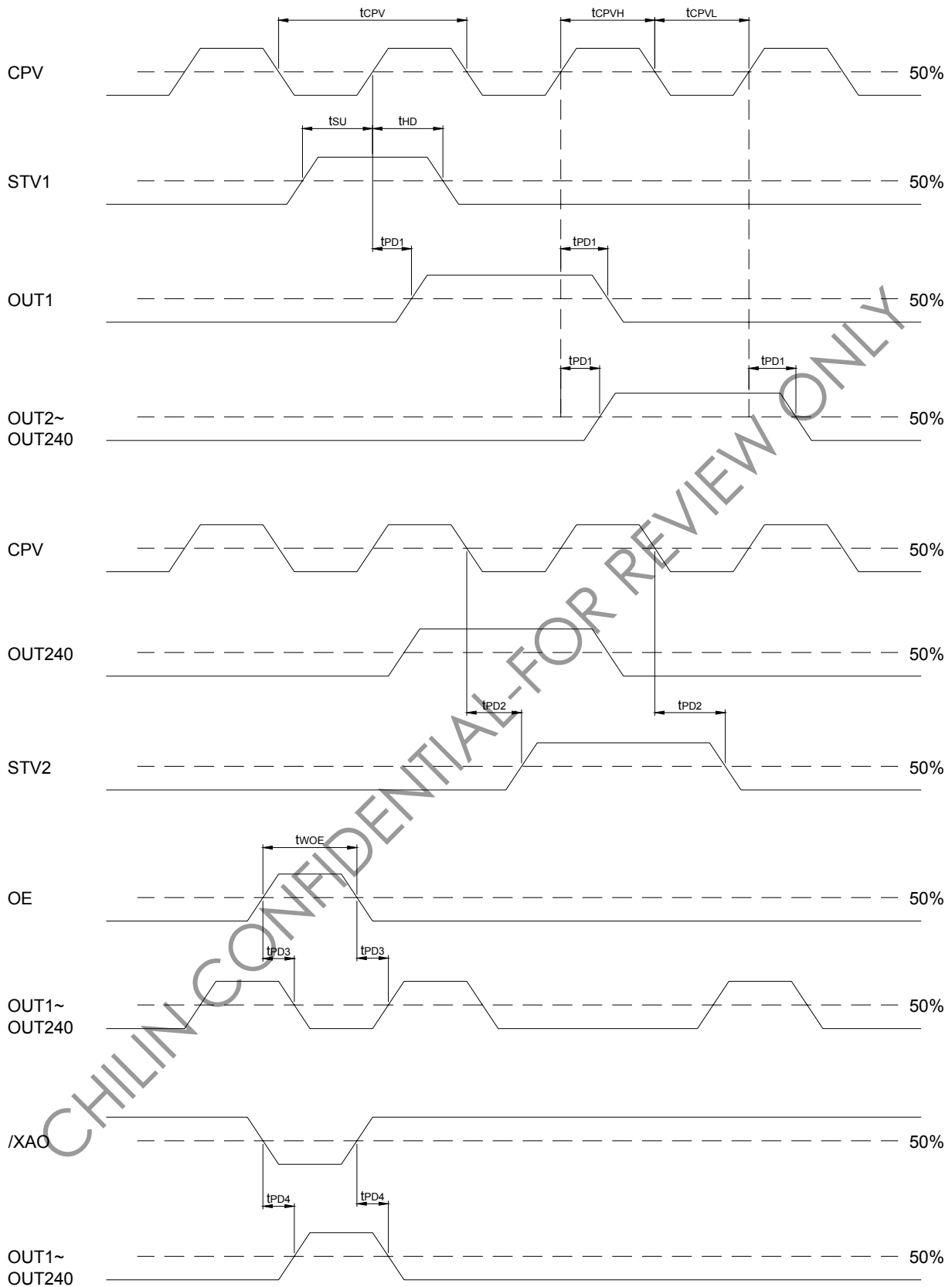
DE\_SEL=L, DE signal with HS and VS signal

DE\_SEL=H, DE signal only

**7.4 Gate Driver Timing Chart**

Parameter	Symbol	Condition	Spec		Unit
			Min.	Max.	
Operation frequency	$t_{CPV}$		5	-	$\mu s$
CPV pulse width	$t_{CPVH}, t_{CPVL}$	50% duty cycle	2.5	-	
OE pulse width	$t_{WOE}$		1	-	
Data setup time	$t_{su}$		0.4	-	$\mu s$
Data hold time	$t_{hd}$		0.7	-	
Output delay time	$t_{pd1}$	$CL=300pF$	-	1	
Output delay time	$t_{pd2}$	$CL=300pF$	-	0.8	
Output delay time	$t_{pd3}$	$CL=300pF$	-	0.8	
Output delay time	$t_{pd4}$	$CL=300pF$	-	10	





**8. OPTICAL CHARACTERISTIC**
 $T_a=25\pm 2^{\circ}\text{C}$ ,  $I_{LED}=140\text{mA}$ 

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	
Response time	Tr	$\theta=0^{\circ}$	-	15	30	ms	Note 3,5	
	Tf		-	35	50	ms		
Contrast ratio	CR	At optimized viewing angle	150	200			Note 4,5	
Color Chromaticity	White	$\theta=0^{\circ}$	Wx	(0.25)	(0.30)	(0.35)		Note 2,6,7
			Wy	(0.27)	(0.32)	(0.37)		
Viewing angle	Hor.	$CR\geq 10$	$\Theta_R$	50	65	-	Deg.	Note 1
			$\Theta_L$	50	65	-		
	Ver.		$\Theta_T$	30	50	-		
			$\Theta_B$	50	55	-		
Brightness	-	-	300	350	-	cd/m <sup>2</sup>	Center of display	

Note 1: Definition of viewing angle range

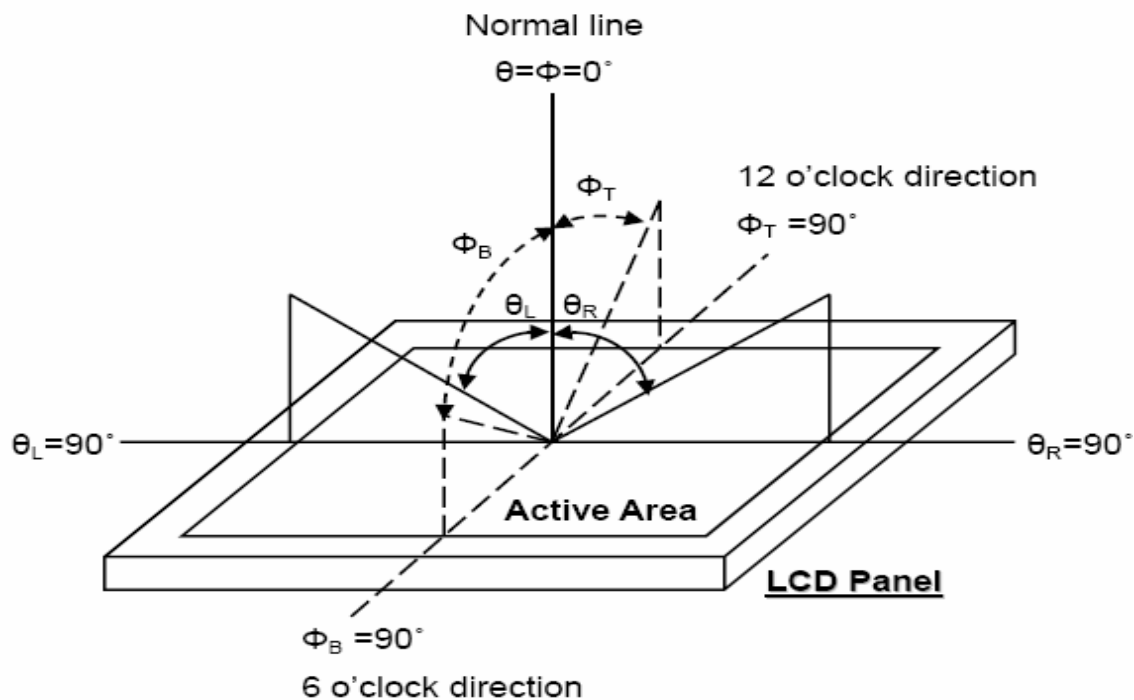


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

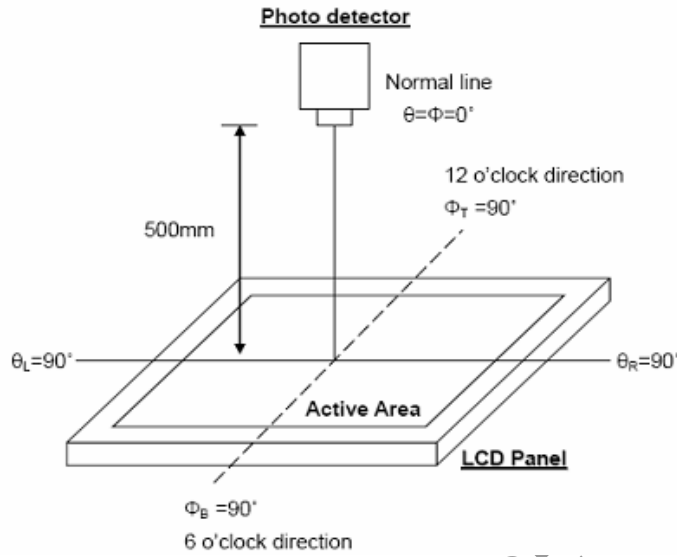


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time,  $T_r$ , is the time between photo detector output intensity changed from 90% to 10%. And fall time,  $T_f$ , is the time between photo detector output intensity changed from 10% to 90%.

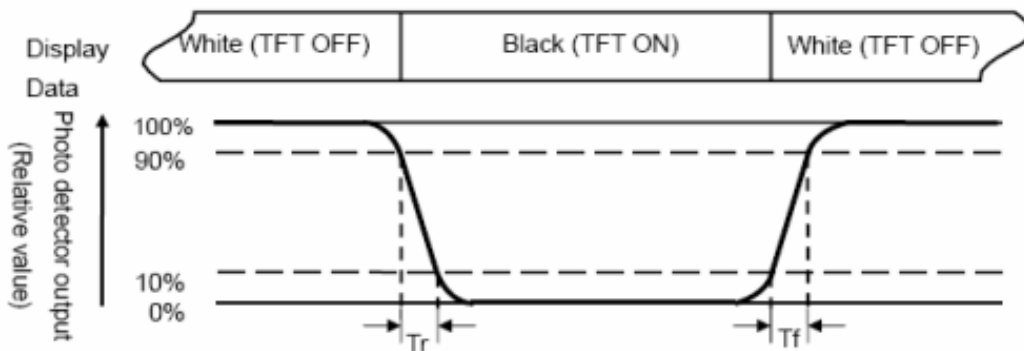


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White  $V_i = V_{i50} \pm 1.5V$

Black  $V_i = V_{i50} \pm 2.0V$

“±” means that the analog input signal swings in phase with VCOM signal.

“±” means that the analog input signal swings out of phase with VCOM signal.

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

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## 9. INTERFACE

### 9.1. LCM PIN Definition

0.5mm Pitch FPC

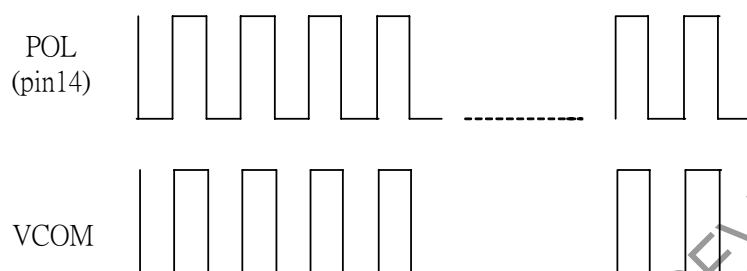
Pin No.	Symbol	I/O	Description	Remark
1	IF1	I	Input data format control (Note1)	Note1
2	IF2	I	Input data format control (Note1)	Note1
3	POL	O	Polarity Signal connect to VCOM driving circuit.	Note3
4	RESET	I	Hardware reset.	
5	SPENA	I	Chip select	Note2
6	SPCL	I	Serial Clock	Note2
7	SPDA	I/O	Serial Data	
8	B0	I	Blue Data bit (LSB)	
9	B1	I	Blue Data bit	
10	B2	I	Blue Data bit	
11	B3	I	Blue Data bit	
12	B4	I	Blue Data bit	
13	B5	I	Blue Data bit	
14	B6	I	Blue Data bit	
15	B7	I	Blue Data bit (MSB)	
16	G0	I	Green Data bit (LSB)	
17	G1	I	Green Data bit	
18	G2	I	Green Data bit	
19	G3	I	Green Data bit	
20	G4	I	Green Data bit	
21	G5	I	Green Data bit	
22	G6	I	Green Data bit	
23	G7	I	Green Data bit (MSB)	
24	R0	I	Red Data bit (LSB)	
25	R1	I	Red Data bit	
26	R2	I	Red Data bit	
27	R3	I	Red Data bit	
28	R4	I	Red Data bit	
29	R5	I	Red Data bit	
30	R6	I	Red Data bit	
31	R7	I	Red Data bit (MSB)	
32	Hsync	I	Horizontal synchronous signal	
33	Vsync	I	Vertical synchronous signal	
34	Data CLK	I	Dot data clock	
35	AVDD(analog)	I	Analog power: 4.5V~5.5V	
36	AVDD(analog)	I	Analog power: 4.5V~5.5V	
37	VDD(Digital)	I	Digital power: 3V~3.6V	
38	VDD(Digital)	I	Digital power: 3V~3.6V	
39	NPC	O	NTSC/PAL mode Auto detection result H:NTSC/L:PAL	
40	VGL	I	Gate off power	
41	VGL	I	Gate off power	
42	UD	I	Up/Down scan setting. H: Reverse scan / L: Normal scan	
43	VGH	I	Gate on power	
44	LRC	I	Shift direction of device internal shift register control.	
45	GND	I	GROUND	
46	VCOM	I	VCOM driving input	Note3
47	VCOM	I	VCOM driving input	
48	ENB	I	Data enable input. Normally pull low.	Note4
49	GND	I	GROUND	
50	GND	I	GROUND	

Note:

- Control the input data format.

IF2,IF1	Input data format
L,L(default)	Serial RGB
L,H	Parallel RGB
H,L	CCIR601
H,H	CCIR656

- Pin 5、Pin 6 usually pull high.
- The polarity of VCOM (Pin 46,47) should be generated from POL (Pin 3).
- For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If ENB signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used.
- The phase of POL ( pin 3 ):

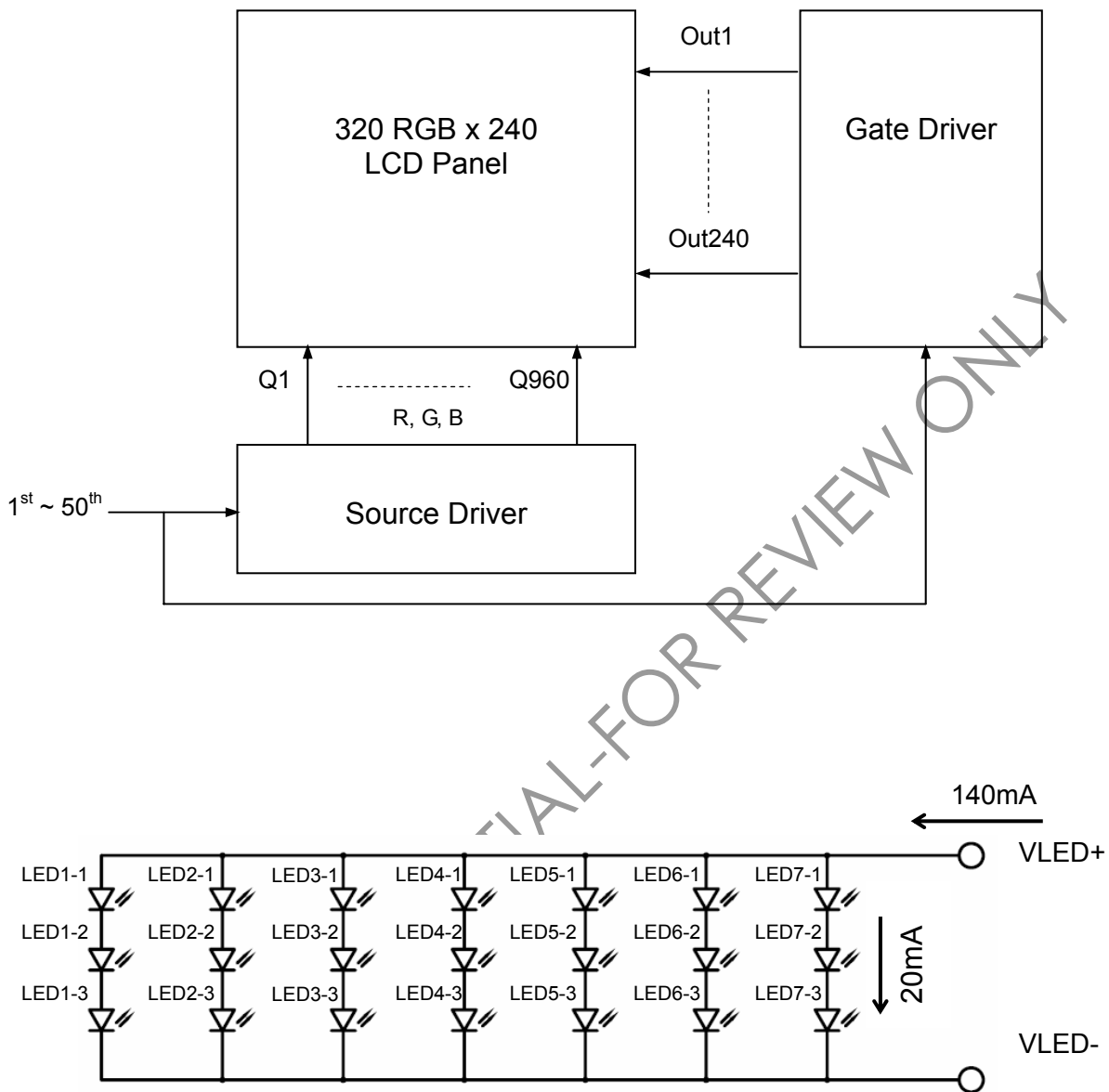


## 9.2. Backlight PIN Definition

Pin No.	Symbol	I/O	Description
1	VLED+	I	Red, LED_Anode
2	VLED-	I	White, LED_Cathode

Note: The backlight interface connector is a model **PHR-2** manufactured by JST or equivalent.  
 The matching connector part number is **S 2B-PH-K-S** manufactured by JST or equivalent.

10. BLOCK DIAGRAM



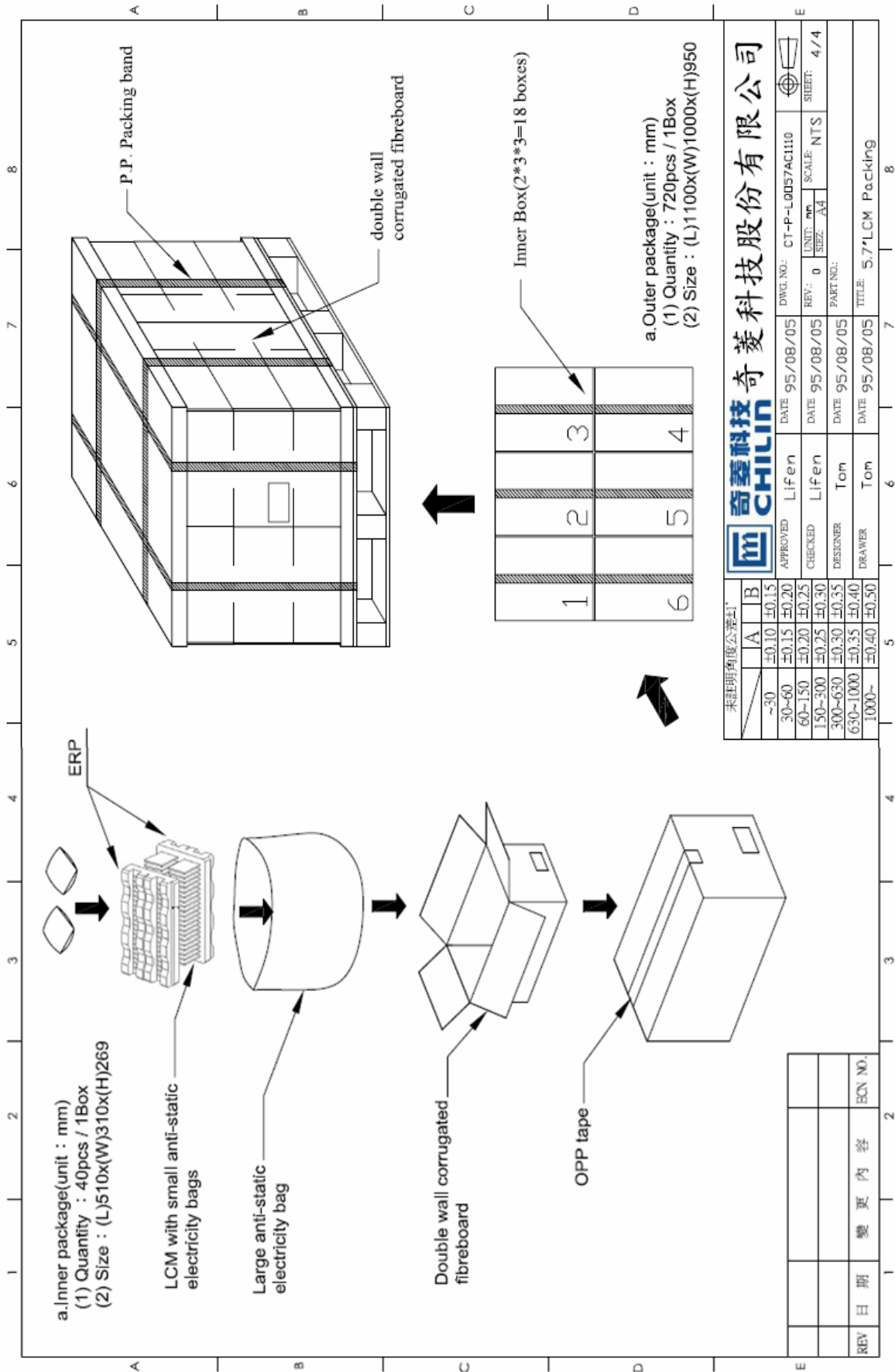
**11. QUALITY ASSURANCE**

No.	Test Items	Test Condition	REMARK
1	High Temperature Storage Test	Ta=80°C 50%RH 240h	
2	Low Temperature Storage Test	Ta=-30°C Dry 240h	
3	High Temperature Operation Test	Ta=70°C 50%RH 240h	
4	Low Temperature Operation Test	Ta=-20°C Dry 240h	
5	High Temperature and High Humidity Operation Test	Ta=60°C 90%RH 240h	
6	Electro Static Discharge Test	-Panel Surface/Top_Case: 150pF ±15kV 150Ω (direct discharge, five times) -FPC input terminal:100pF, ±200V 0Ω	
7	Shock Test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces (i.e. run 180G 2ms for all six faces)	
8	Vibration Test (non-operating)	Sine wave, 10 ~ 500 ~ 10Hz, 1.5G, 0.37oct/min 3 axis, 1hour/axis	
9	Thermal Shock Test	-30°C (0.5h) ~ 80°C (0.5h) / 100 cycles	

\*\*\*\*\* Ta= Ambient Temperature



**13. PACKAGE INFORMATION**



## 14. PRECAUTIONS

Please pay attention to the following when you use this TFT LCD module.

### 14.1 MOUNTING PRECAUTIONS

- (1) You must mount a module using arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.  
And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach a transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not describe because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are determined to the polarizer)
- (7) When the surface becomes dusty, please wipe gently with adsorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

### 14.2 OPERATING PRECAUTIONS

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :  $V=\pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower)  
And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

### 14.3 ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

### 14.4 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

#### 14.5 STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

#### 14.6 HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) The protection film is attached to the polarizer with a small amount of glue. Is apt to remain on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.
- (3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- (4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

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