HIGH-SPEED A/D-D/A CONVERTER

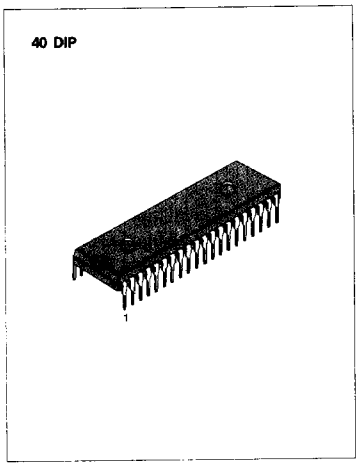
Samsung KSV3100A, VLSI circuit in CI (Collector Implanted) technology, consists of a high-speed flash-type 8-bit A/D converter and a high-speed low-glitch 10-bit D/A converter designed as an R-2R network with switched current sources. Also, the various auxiliary circuits, as reference voltage sources, pre-amplifier, input clamping circuit and feed-in output amplifier are integrated on the single chip.

KSV3100A has been developed for use in all applications which call for a high-speed A/D-D/A converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcast.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although KSV3100A was initially designed as high-speed codecs for the video range, it can be used with equal benefits for lower frequencies, even down to zero.



BLOCK DIAGRAM

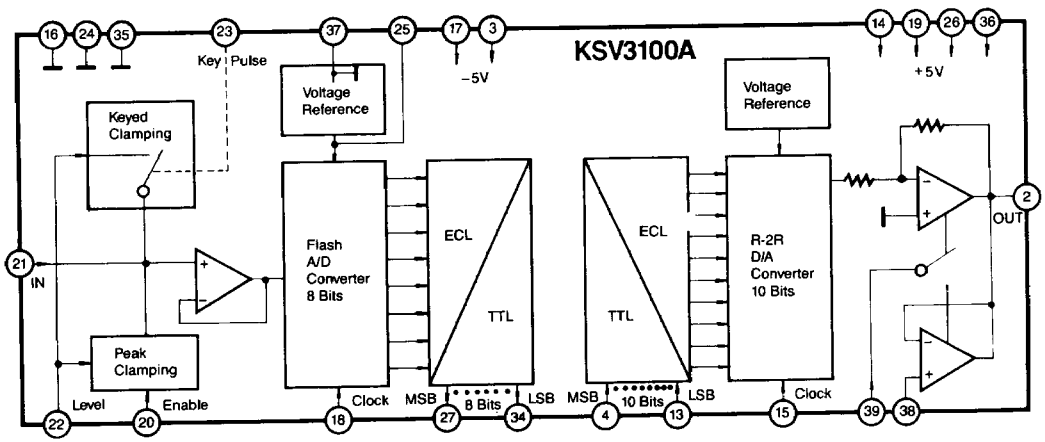


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input, in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping or peak clamping or without clamping. Also the D/A converter's reference voltage is generated on-chip, and a gated amplifier is arranged at the output of the D/A converter so that an external analog signal can be fed-in instead of the signal delivered by the D/A converter.

Separate clock inputs are provided for the A/D converter and the D/A converter thus enabling the application of time compression procedures.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	No Connection	21	Analog Input A/D Converter
2	Analog Output D/A Converter	22	Clamping Level Input
3	−5V Supply D/A Converter-Analog	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	−5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	No Connection

TEST CIRCUIT

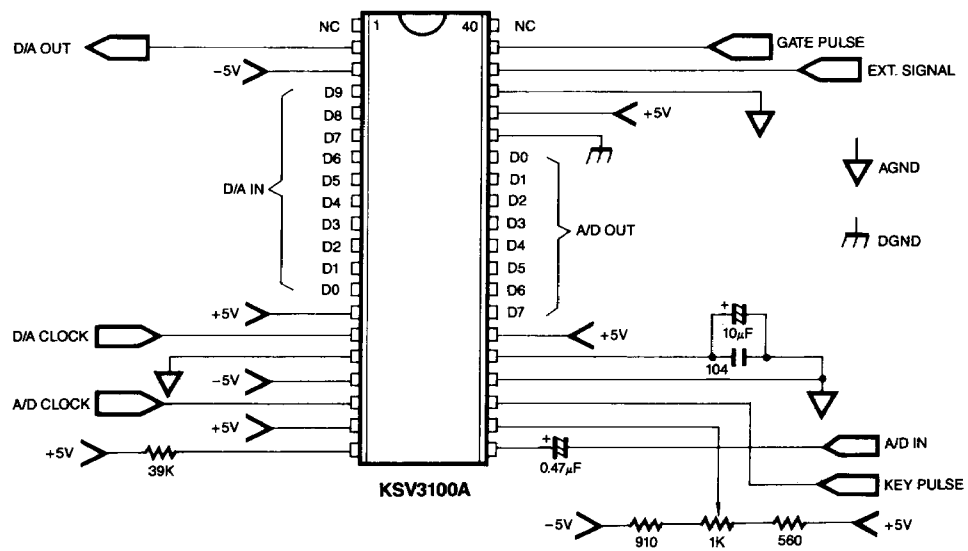


Fig. 2

B. R-2R Ladder D/A Converter

A second popular technique for D/A convertion is the R-2R ladder method. As shown in figure 11, the network consists of series resistor of value R and shunt resistors of value 2R. The bottom of each shunt resistor has a singlepole duble-throw electronic switch which connects the resistor to either ground or the output current summing line.

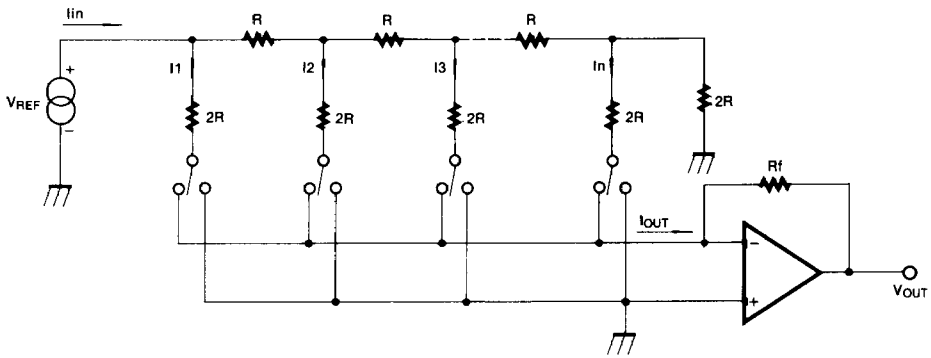


Fig. 11 R-2R Ladder D/A Converter

The operation of the R-2R ladder network is based on the binary division of current as it flows down the ladder. Examination of the ladder configuration reveals that at point a looking to the right, one measures a resistance of 2R; therefore the reference input to the ladder has a resistance of R. At the reference input the current splits into two equal parts since it sees equal resistances in either direction. Likewise, the current flowing down the ladder to the right continues to divide into two equal parts at each resistor junction.

The result is binary weighted currents flowing down each shunt resistor in the ladder. The digitally controlled switches direct the currents to either the summing line or ground. Assuming all bits are on as shown in the diagram, the output current is

$$I_{OUT} = \frac{V_{REF}}{R} \ (1/2 + 1/4 + 1/8 \ldots\ldots + 1/2^n)$$

which is a binary series. The sum of all currents is then

$$I_{OUT} = \frac{V_{REF}}{R} \ (1 - 2^{-n})$$

where the 2 term physically represents the portion of the input current flowing through the 2R terminating resistor to ground at the far right.

As in the previous circuit, the output current summing line goes to an operational amplifier which converts current to voltage.

$$V_{OUT} = -Rf\ I_{OUT}$$

The advantage of the R-2R ladder technique is that only two values of resistors are required, with the resultant ease of matching or trimming and excellent temperature tracking. In addition, for high speed applications relatively low resistor values can be used. Excellent results can be obtained for high resolution D/A converters by using laser-trimmed thin film resistor networks.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{EE} = −5V, f_{15} = 20MHz, f_{18} = 20MHz, Ta = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC} I_{EE}	— —	90 −80	120 −110	mA mA
Power Dissipation	P_{TOT}	—	—	1.2	W
Total Transfer Time A/D-D/A	t_{TOT}	See Fig. 3			—
A/D Converter					
Input Current Pin 21	I_I	—	2	—	μA
Input Capacitance Pin 21	C_I	—	10	—	pF
Input Impedance Pin 21					
at f = 1KHz	Z_I	—	20	—	MΩ
at f = 10MHz	Z_I	—	100	—	KΩ
3dB Bandwidth of the Input Amp.	—	—	50	—	MHz
Keyed Clamping Active Level	V_{23}	2.0	—	V_{CC}	V
On Resistance of the Clamping Switch Between Pin 21 and 22	R_{ON}	—	300	—	Ohm
Input Current of the Clamping Level Input Pin 22 (V_{20} = 3V, V_{22} = 2V)	I_{22}	—	150	—	μA
Aperture Delay (② in Fig. 3)	t_{AD}	—	—	10	ns
Digital Output Delay (③ in Fig. 3)	t_{DV}	—	25	—	ns
Transfer Time (⑤ in Fig. 3)	t_W	One clock period			—
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	8	—	—
Code of the Digital Output Signal	—	Binary			—
Output CODE at the Input with V_{21} = 0V with V_{21} = V_{ref}	— —	00000000 11111111			— —
Internal Reference Voltage	V_{25}	1.8	2.0	2.2	V
D/A Converter					
Output Impedance Pin 2	Z_O	—	15	—	Ω
Input Current Pin 38 (V_{38} = 2V)	I_{ID}	—	0.6	—	mA
Internal Reference Voltage	V_{ref}	1.8	2.0	2.2	V
Input Resister Hold Time (⑦ in Fig. 3)	t_{IH}	6.0	—	—	ns
Input Resister Setup Time (⑧ in Fig. 3)	t_{IH}	20	—	—	ns
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	10	—	—
Code of the Digital Input Signal	—	Binary			—
Output Signal at the Input with 00000 00000 with 11111 11111	 V_2 V_2	 — —	 0 2	 — —	 V V
Settling Time	t_S	—	50	—	ns

ORDERING INFORMATION

KSV3100A has four kind of version according to the accuracy bit (so called 'Precision') of D/A Converter, and their marking specifications are as follow;

Device	Package	Temperature Range	D/A Converter		A/D Converter
			Accurary Bit	Diff. Nonlinearity	Diff. Nonlinearity
KSV3100ACN-10	40 DIP	0 ~ +70°C	10 bit	± 1/2 LSB	± 1/2 LSB
KSV3100ACN-9			9 bit	± 1 LSB	
KSV3100ACN-8			8 bit	± 2 LSB	
KSV3100ACN-7			7 but	± 4 LSB	

* The accuracy of A/D Converter can be guaranteed as '8 bit' (differential nonlinearity = ± 1/2 LSB) regardless of the D/A Converter's accuracy.

TIMING DIAGRAM

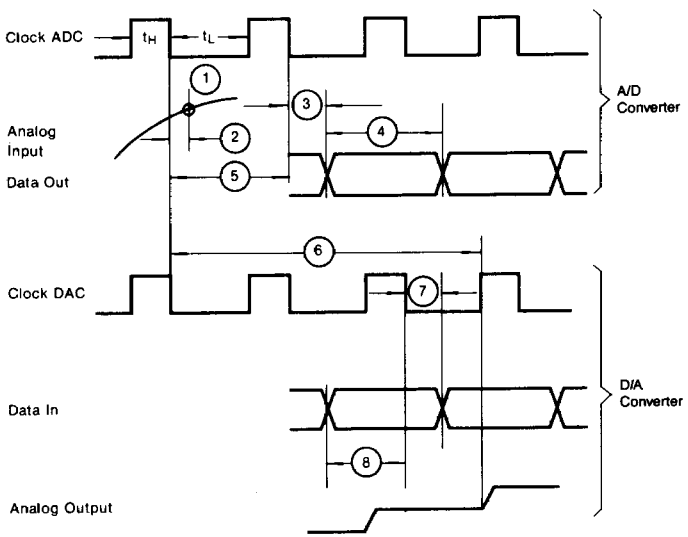


Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

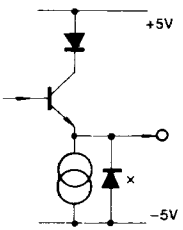


Fig. 4: Pin 2, Output

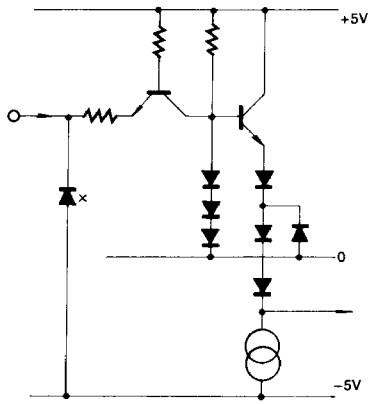


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

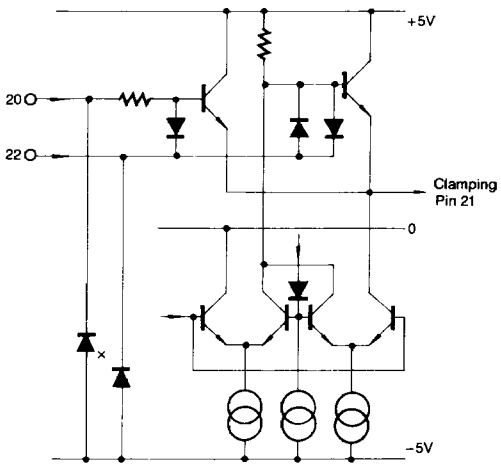


Fig. 6: Pins 20 and 22, Inputs

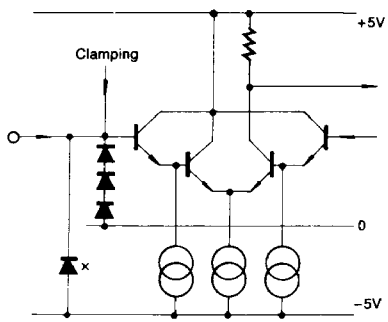


Fig. 7: Pin 21, Input

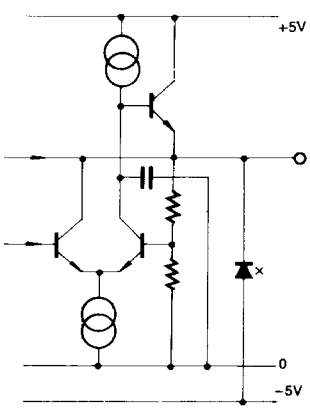


Fig. 8: Pin 25, Reference Voltage Pin

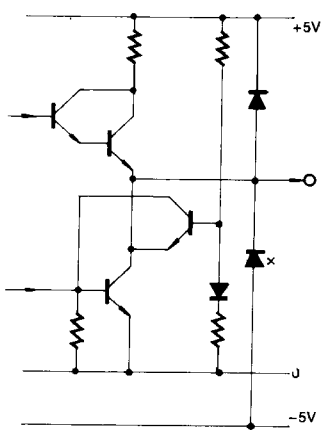


Fig. 9: Pins 27 to 34, Outputs

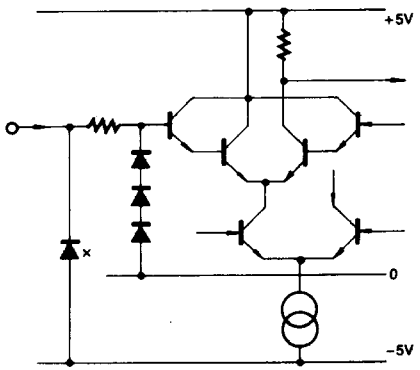


Fig. 10: Pin 38, Input
x = protection diode

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	No Connection
Pin 2	Analog Output D/A Converter This pin whose diagram is shown in Fig. 4, is the output for the processed analog signal either originating from the D/A converter or from the external analog input pin 38.
Pin 3	−5 Volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+5 Volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin whose diagram is shown in Fig. 5 must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.
Pin 17	−5 Volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5. Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+5 Volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via pin 20 whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS (Continued)

Pin No.	Description
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Fig. 5 is the diagram of this input. Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as ground pin for the analog part of the A/D converter.
Pin 25	Reference Voltage A/D Converter This pin whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to pin 37.
Pin 26	+5 Volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 9 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+5 Volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference Voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3100A instead of the D/A-converted signal originating from pin 4 to 13.
Pin 39	Output Signal Switchover Input This pin whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to pin 38.
Pin 40	No Connection

APPENDIX: APPLICATION CIRCUITS

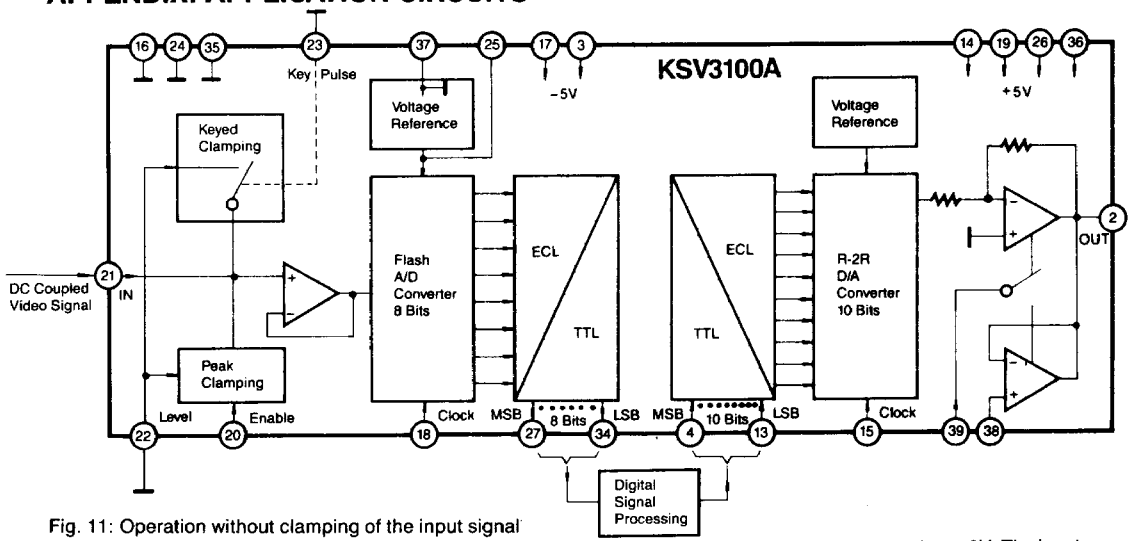


Fig. 11: Operation without clamping of the input signal

Pin 20 (peak clamping enable input) should be opened, while pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 21, without coupling capacitor such that it lies between 0 and +2V.

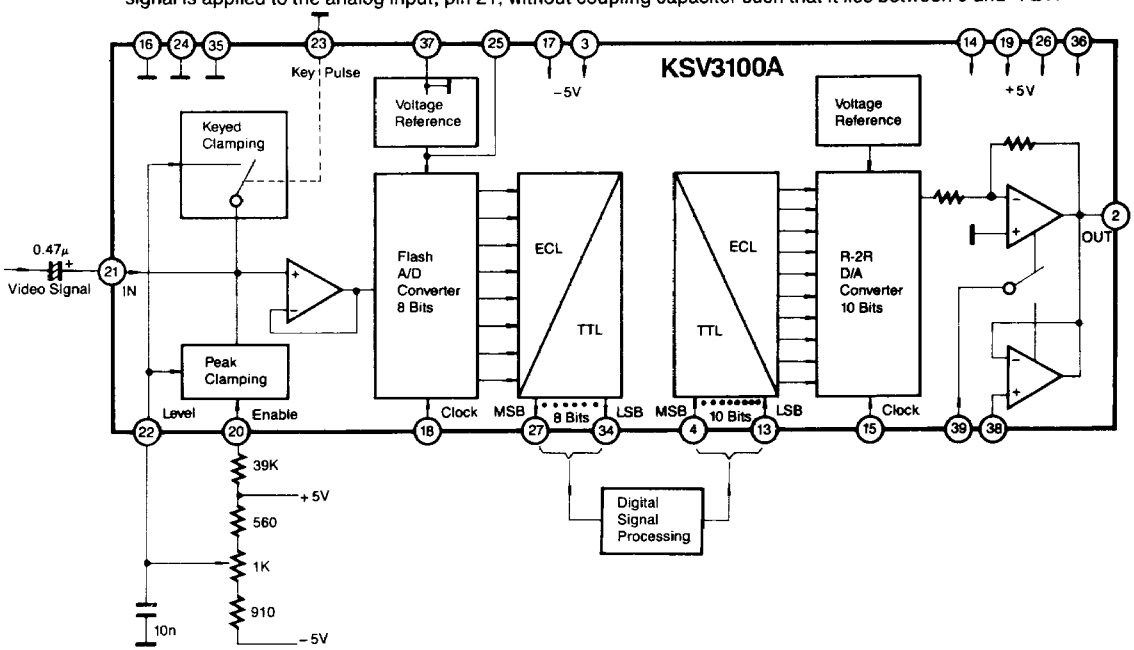


Fig. 12: Operation with peak clamping

The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and pin 22 (clamping level input) is connected, as desired, to zero or a voltage between −1 and +2V. The input signal is fed to pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

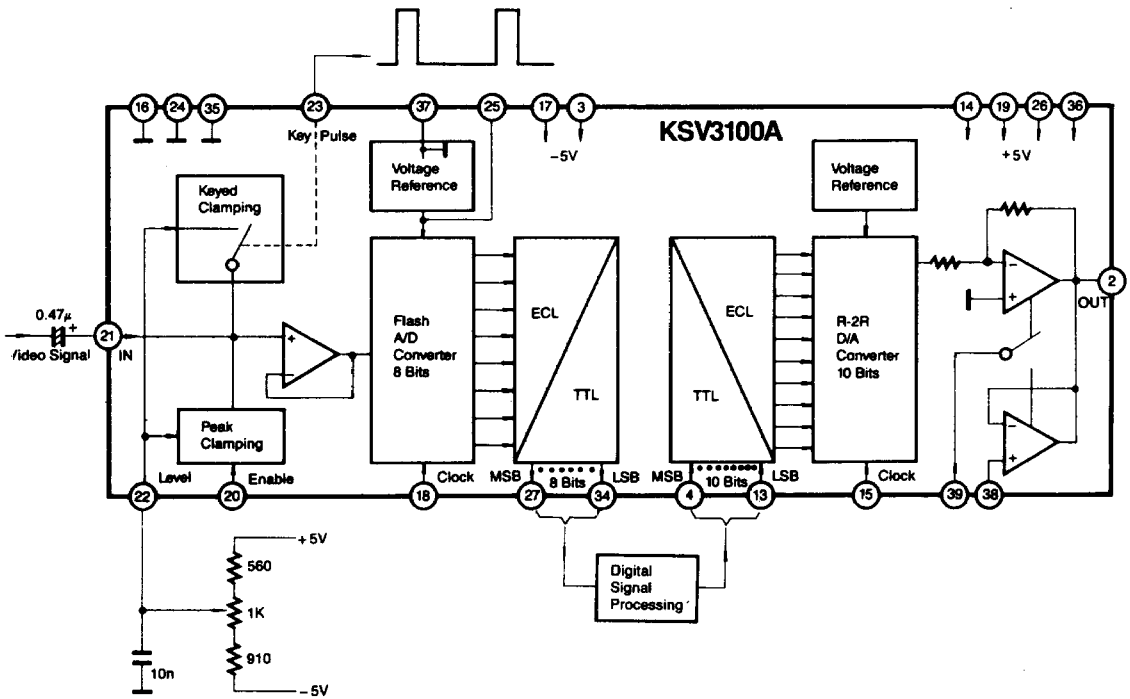


Fig. 13: Operation with keyed clamping

The input signal is applied to pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 23. By this means the clamping switch in the KSV3100A connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between -1 and $+2$V.