FAIRCHILD SEMICONDUCTOR®

September 2012

FDPC1002S

PowerTrench® Power Clip
25V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 7.3 mΩ at V_{GS} = 4.5 V, I_D = 12 A

Q2: N-Channel

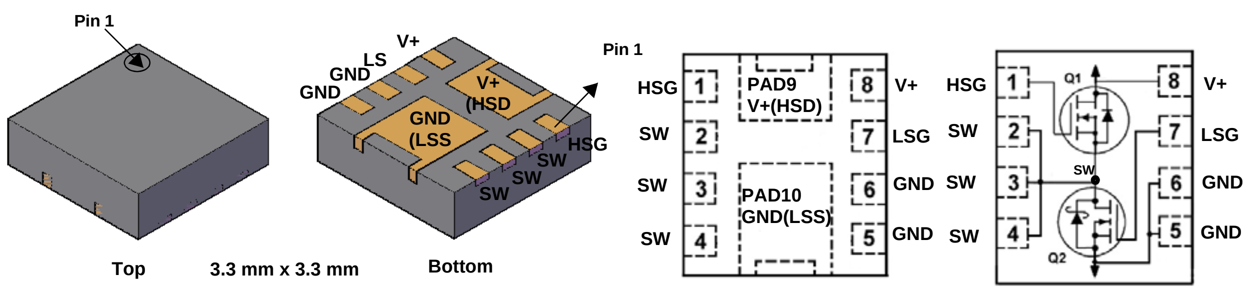
- Max $r_{DS(on)}$ = 2.1 mΩ at V_{GS} = 4.5 V, I_D = 24 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		25	25	V
V_{GS}	Gate to Source Voltage		12	12	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C	20	60	A
	-Continuous	T_A = 25 °C	13[1a]	27[1b]	
	-Pulsed		40	120	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	21	97	mJ
P_D	Power Dissipation for Single Operation	T_A = 25 °C	1.6[1a]	2.0[1b]	W
	Power Dissipation for Single Operation	T_A = 25 °C	0.8[1c]	0.9[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	77[1a]	63[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	151[1c]	135[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.0	3.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
13OD/15OD	FDPC1002S	Power Clip 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		14 24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V V_{DS} = 20 V, V_{GS} = 0 V	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 12 V/-8 V, V_{DS}= 0 V V_{GS} = 12 V/-8 V, V_{DS}= 0 V	Q1 Q2			±100 ±100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA $V_{GS} = V_{DS}$, I_D = 1 mA	Q1 Q2	0.8 1.1	1.2 1.4	2.2 2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-4 -3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 4.5 V, I_D = 12 A V_{GS} = 10 V, I_D = 13 A, T_J =125 °C	Q1		4.6 5.4 5.6	6.0 7.3 7.3	mΩ
		V_{GS} = 10 V, I_D = 27 A V_{GS} = 4.5 V, I_D = 24 A V_{GS} = 10 V, I_D = 27 A, T_J =125 °C	Q2		1.2 1.4 1.7	1.8 2.1 2.4	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A V_{DS} = 5 V, I_D = 27 A	Q1 Q2		97 231		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	Q1: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1240 4335		pF
C_{oss}	Output Capacitance		Q1 Q2		332 1126		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		49 143		pF
R_g	Gate Resistance		Q1 Q2		0.4 0.5		Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 13 V, I_D = 13 A, R_{GEN} = 6 Ω Q2: V_{DD} = 13 V, I_D = 27 A, R_{GEN} = 6 Ω	Q1 Q2		7 13		ns
t_r	Rise Time		Q1 Q2		2 5		ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		20 38		ns
t_f	Fall Time		Q1 Q2		2 4		ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V Q1 V_{DD} = 13 V, I_D = 13 A Q2 V_{DD} = 13 V, I_D = 27 A	Q1 Q2		19 64		nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		9 30		nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		2.6 9.3		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		2.3 7.7		nC

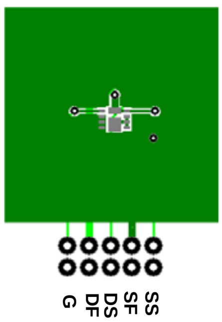
Electrical Characteristics T_J = 25 °C unless otherwise noted

Drain-Source Diode Characteristics

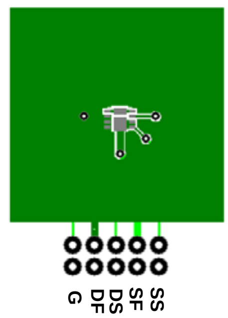
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 2) V_{GS} = 0 V, I_S = 27 A (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 13 A, di/dt = 100 A/µs	Q1 Q2		22 30		ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 27 A, di/dt = 300 A/µs	Q1 Q2		8 32		nC

Notes:

1.$R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 77 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 63 °C/W when mounted on a 1 in^2 pad of 2 oz copper

c. 151 °C/W when mounted on a minimum pad of 2 oz copper

d. 135 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. Q1 :E_{AS} of 21 mJ is based on starting T_J = 25 ^oC; N-ch: L = 1.2 mH, I_{AS} = 6 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 14.5 A.
Q2: E_{AS} of 97 mJ is based on starting T_J = 25 ^oC; N-ch: L = 0.6 mH, I_{AS} = 18 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 32.9 A.

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

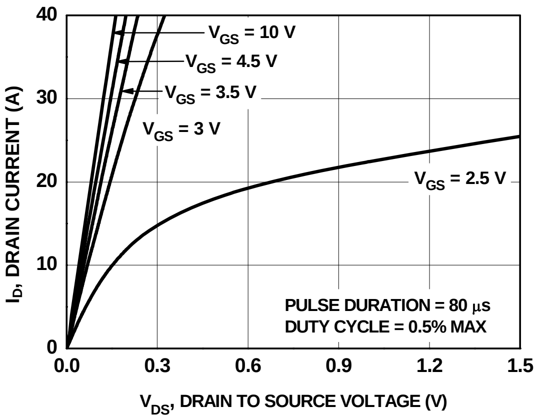


Figure 1. On Region Characteristics

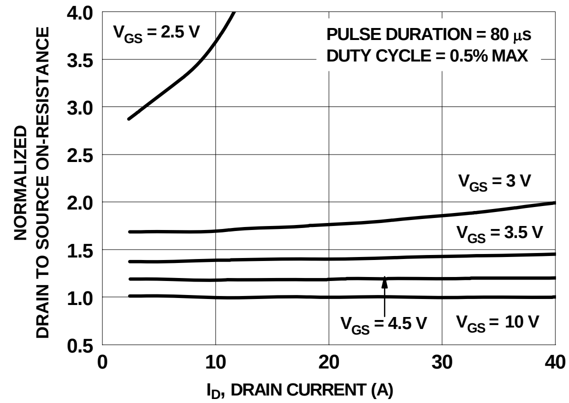


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

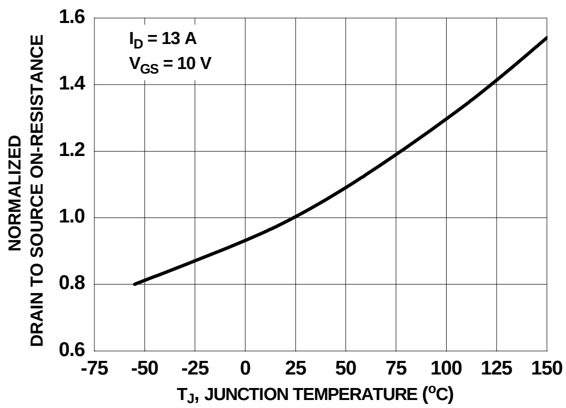


Figure 3. Normalized On Resistance vs Junction Temperature

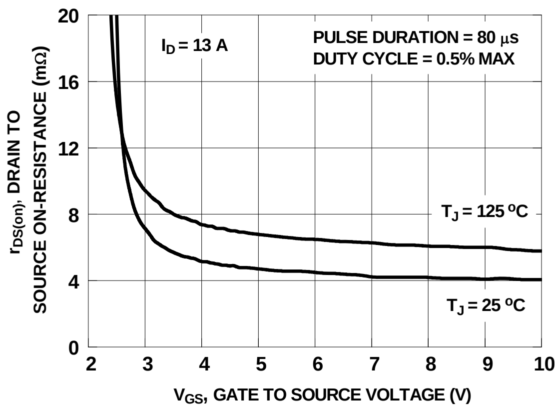


Figure 4. On-Resistance vs Gate to Source Voltage

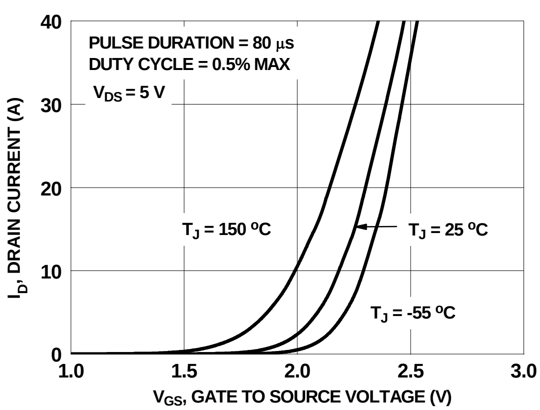


Figure 5. Transfer Characteristics

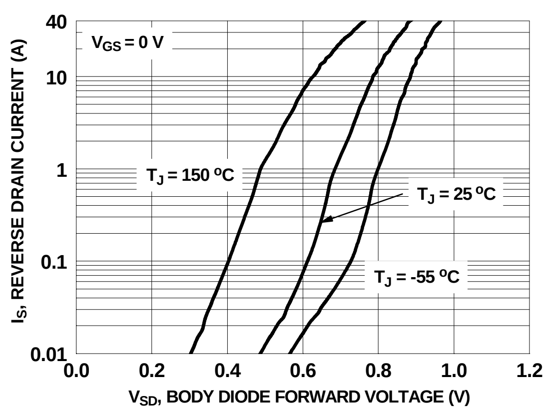


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

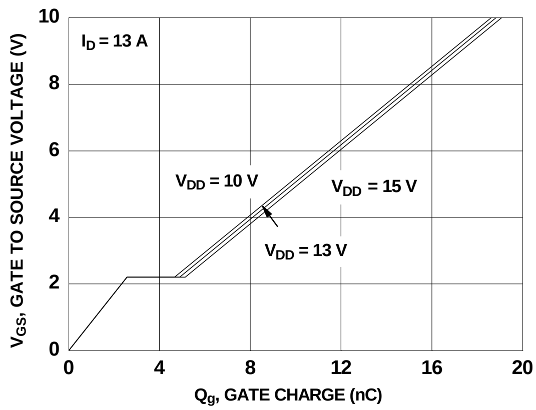


Figure 7. Gate Charge Characteristics

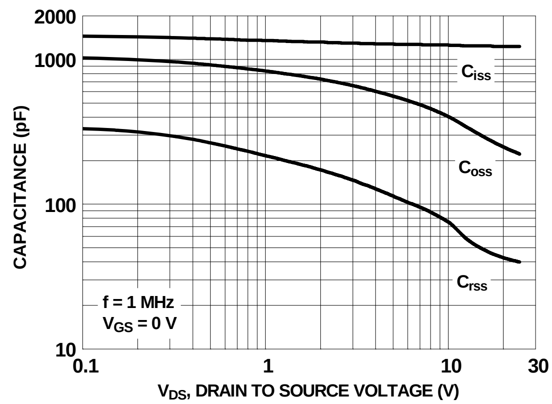


Figure 8. Capacitance vs Drain to Source Voltage

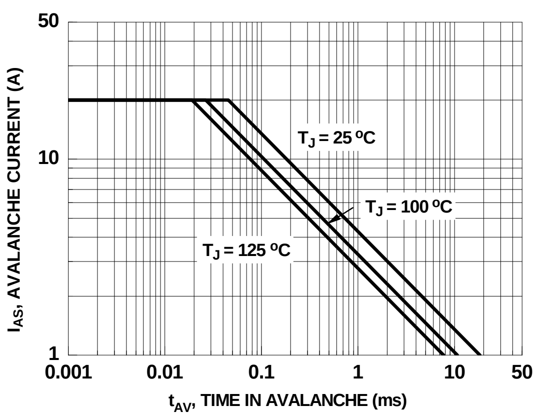


Figure 9. Unclamped Inductive Switching Capability

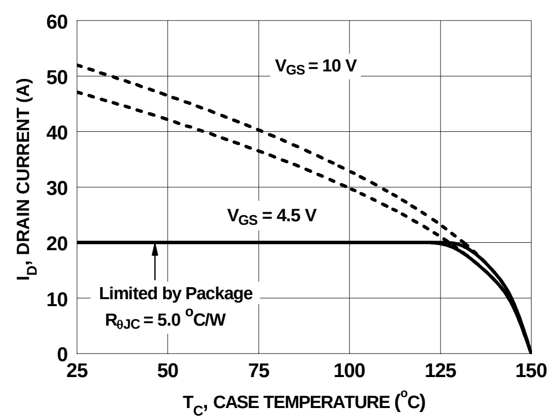


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

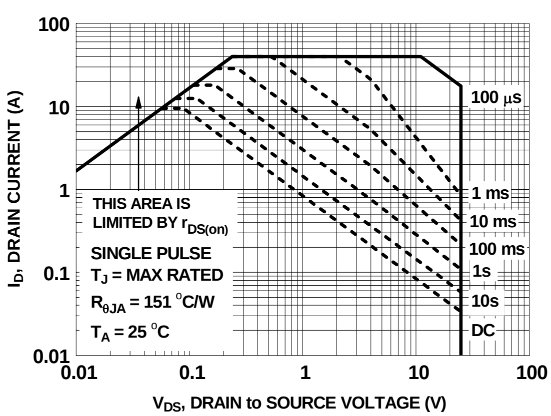


Figure 11. Forward Bias Safe Operating Area

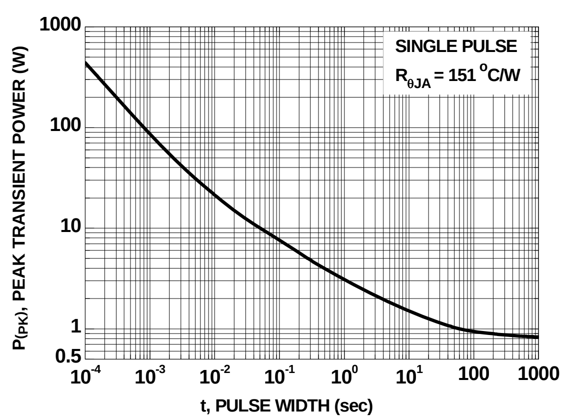


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

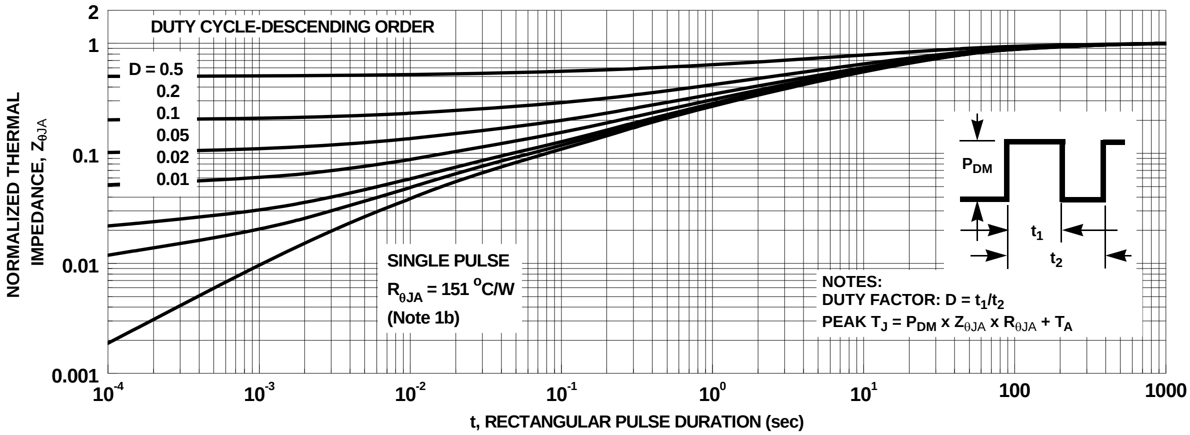


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 ^oC unlenss otherwise noted

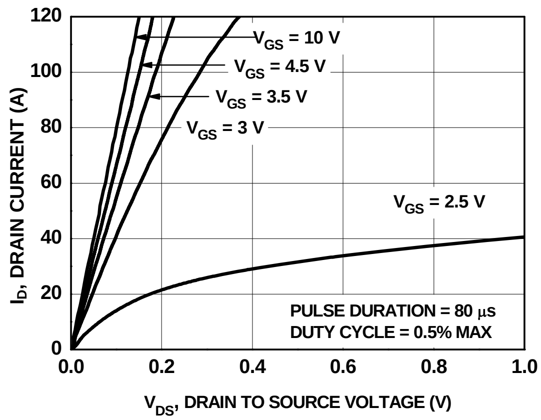


Figure 14. On-Region Characteristics

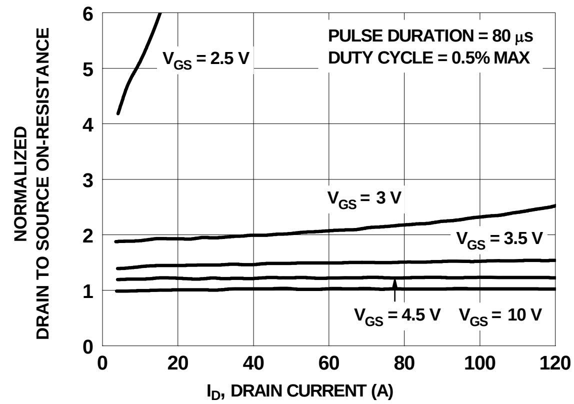


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

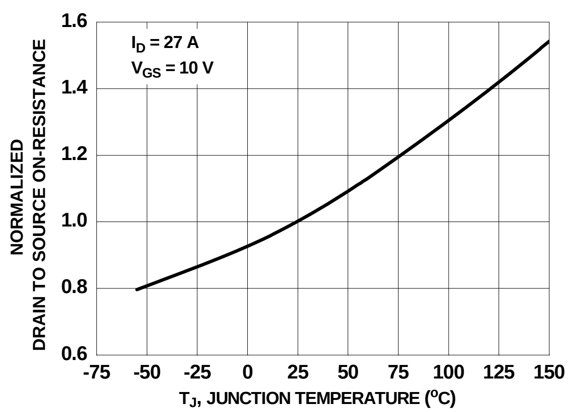


Figure 16. Normalized On-Resistance vs Junction Temperature

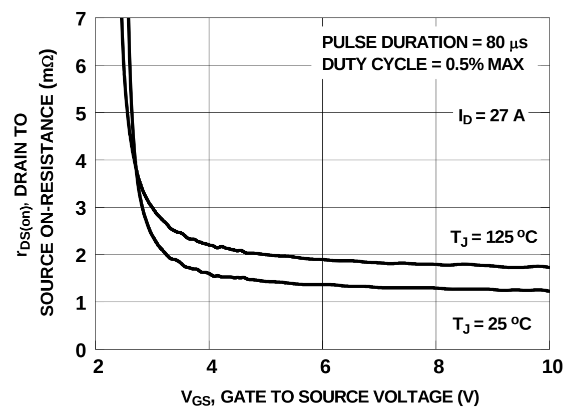


Figure 17. On-Resistance vs Gate to Source Voltage

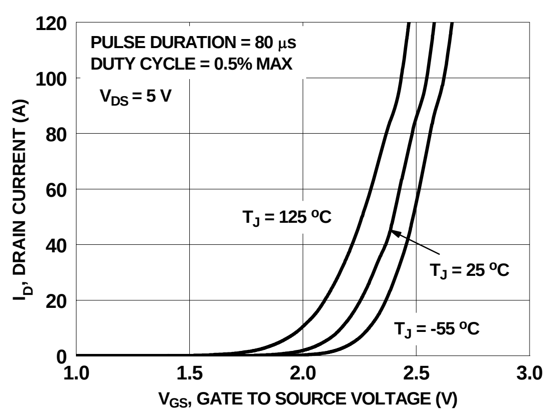


Figure 18. Transfer Characteristics

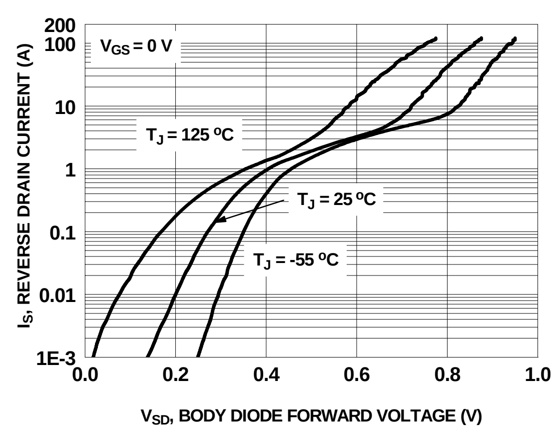


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted

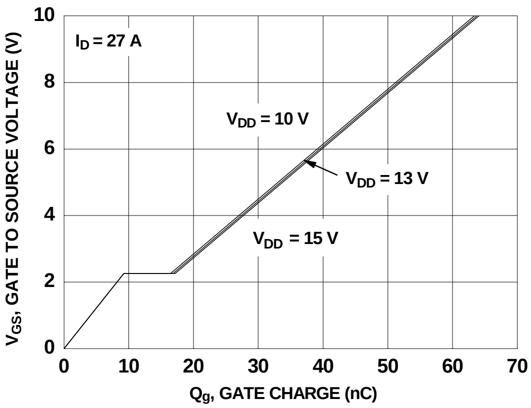


Figure 20. Gate Charge Characteristics

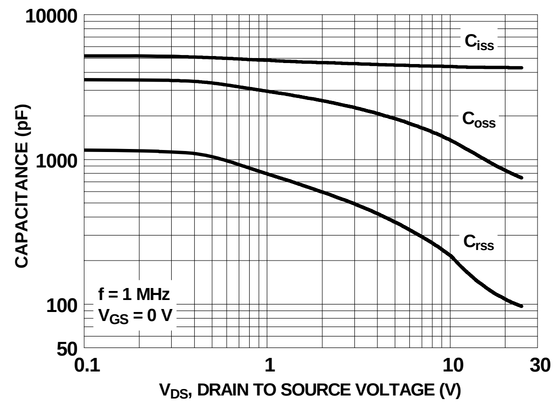


Figure 21. Capacitance vs Drain to Source Voltage

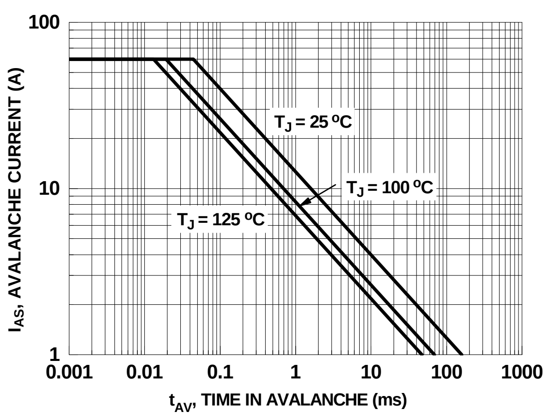


Figure 22. Unclamped Inductive Switching Capability

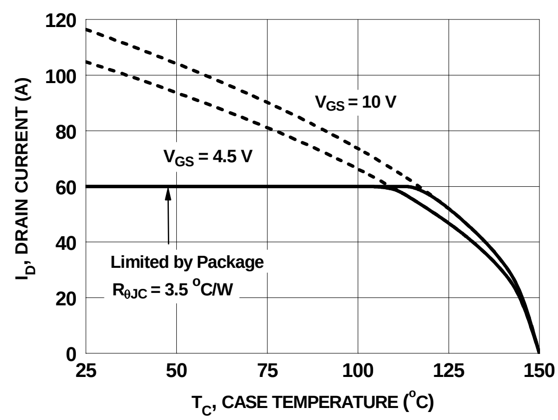


Figure 23. Maximum Continouns Drain Current vs Ambient Temperature

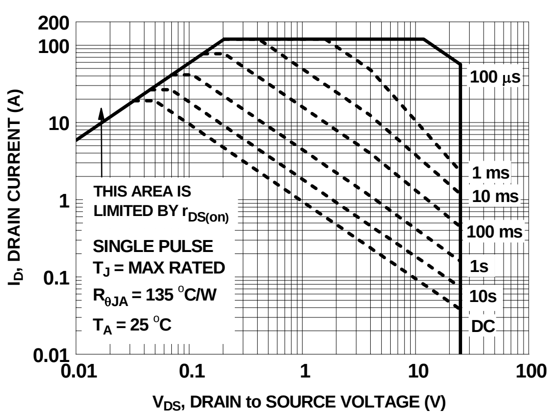


Figure 24. Forward Bias Safe Operating Area

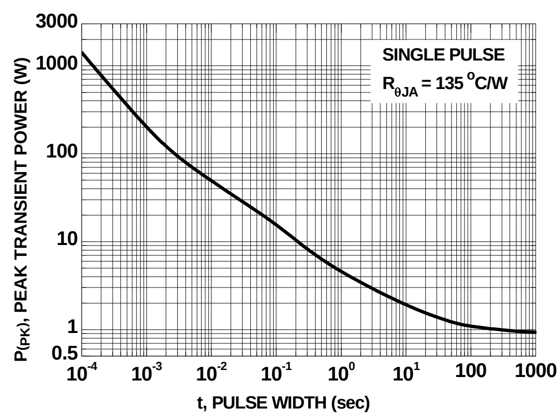


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted

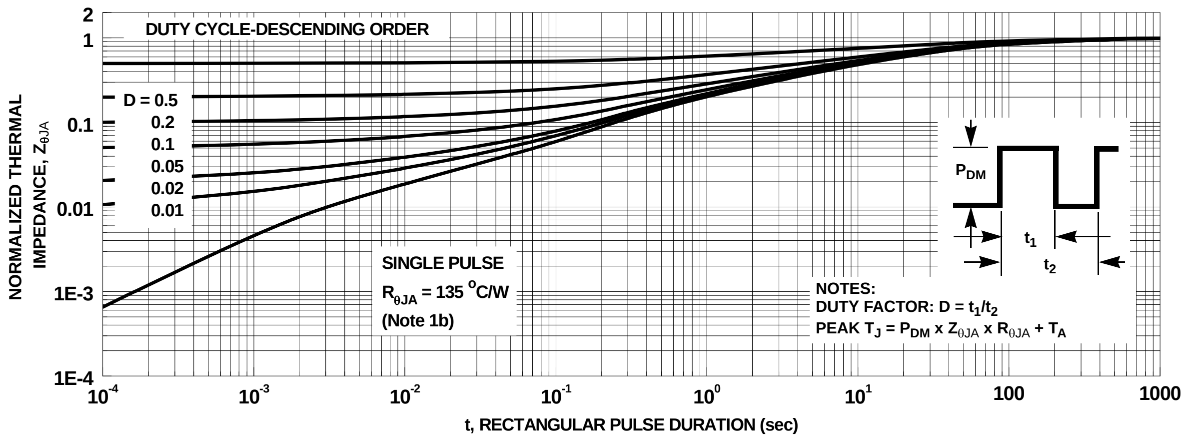


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET[TM] Schottky body diode Characteristics

Fairchild's SyncFET[TM] process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC1002S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

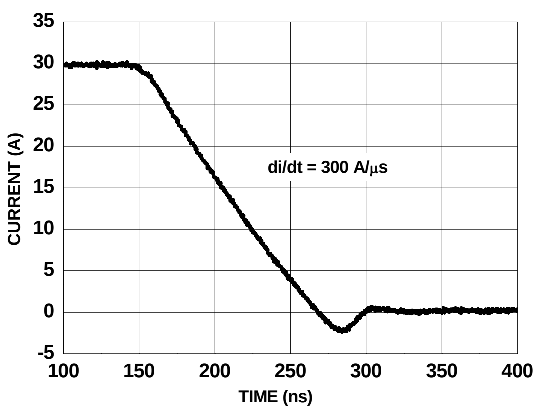


Figure 27. FDPC1002S SyncFET[TM] body diode reverse recovery characteristic

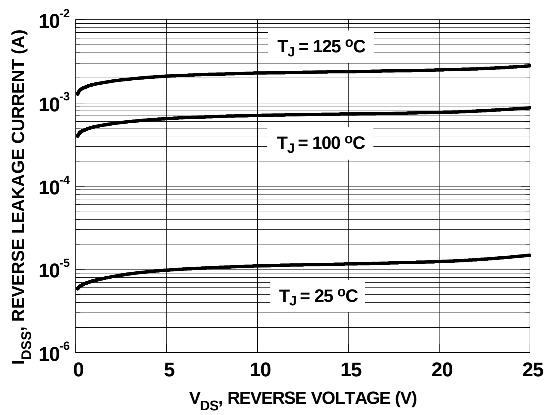


Figure 28. SyncFET[TM] body diode reverse leakage versus drain-source voltage

Application Information

Typical Application Diagram (Synchronous Rectifier Buck Converter)

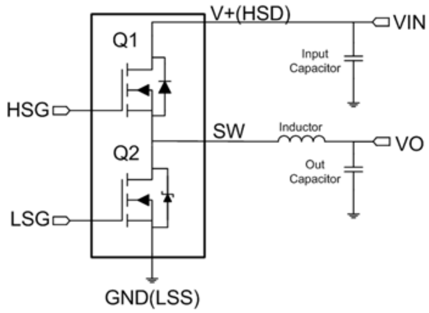


Figure 1.Power Clip in Buck Converter Topology

As shown in Figure 1, in the Power Clip package Q1 is the High Side MOSFET (Control MOSFET) and Q2 is the Low Side MOSFET (Synchronous MOSFET). Figure 2 below shows the package pin out. The blue overlay on the drawing indicates a typical PCB land pattern for the part.

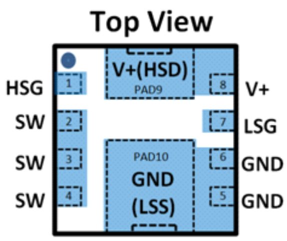


Figure 2.Top View of Power Clip

Table 1 Pin Information shows the name and description of each pin.

PIN		Description
Number	**Name**	
1	HSG	Gate signal input of Q1 Gate
2,3,4	SW	Switch or Phase node, Source of Q1 and Drain of Q2
5,6,PAD 10	GND,GND(LSS) PAD	Ground, Source of Q2
7	LSG	Gate signal input of Q2 Gate
8,PAD 9	V+, V+(HSD) PAD	Input voltage of SR Buck converter, Drain of Q1

Table 1. Pin Information

Recommended PCB Layout Guidelines

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Clip is a high power density solution and all high current flow paths, such as V+(HSD), SW and GND(LSS) should be short and wide for minimal resistance and inductance. V+(HSD) and GND(LSS) are the primary heat flow paths for the Power Clip. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.

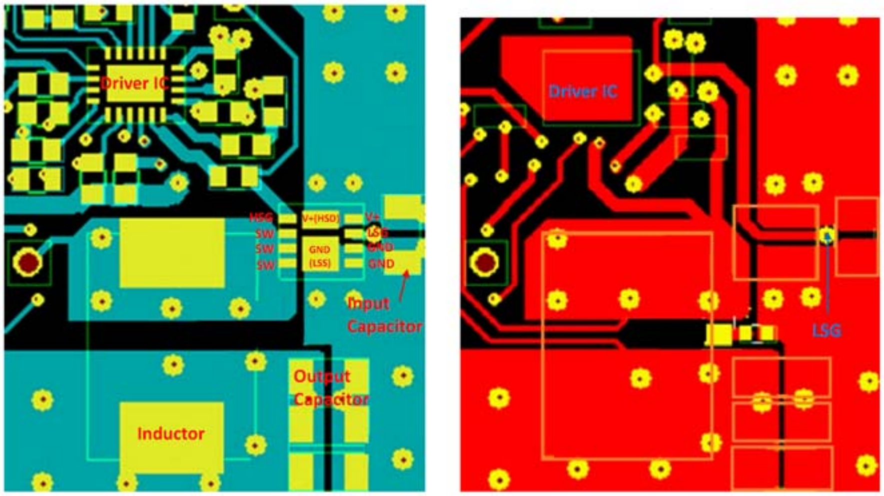


Figure 3.Top/Component (green) View and Bottom (red) PCB View

Following is a guideline, not a requirement which the PCB designer should consider.

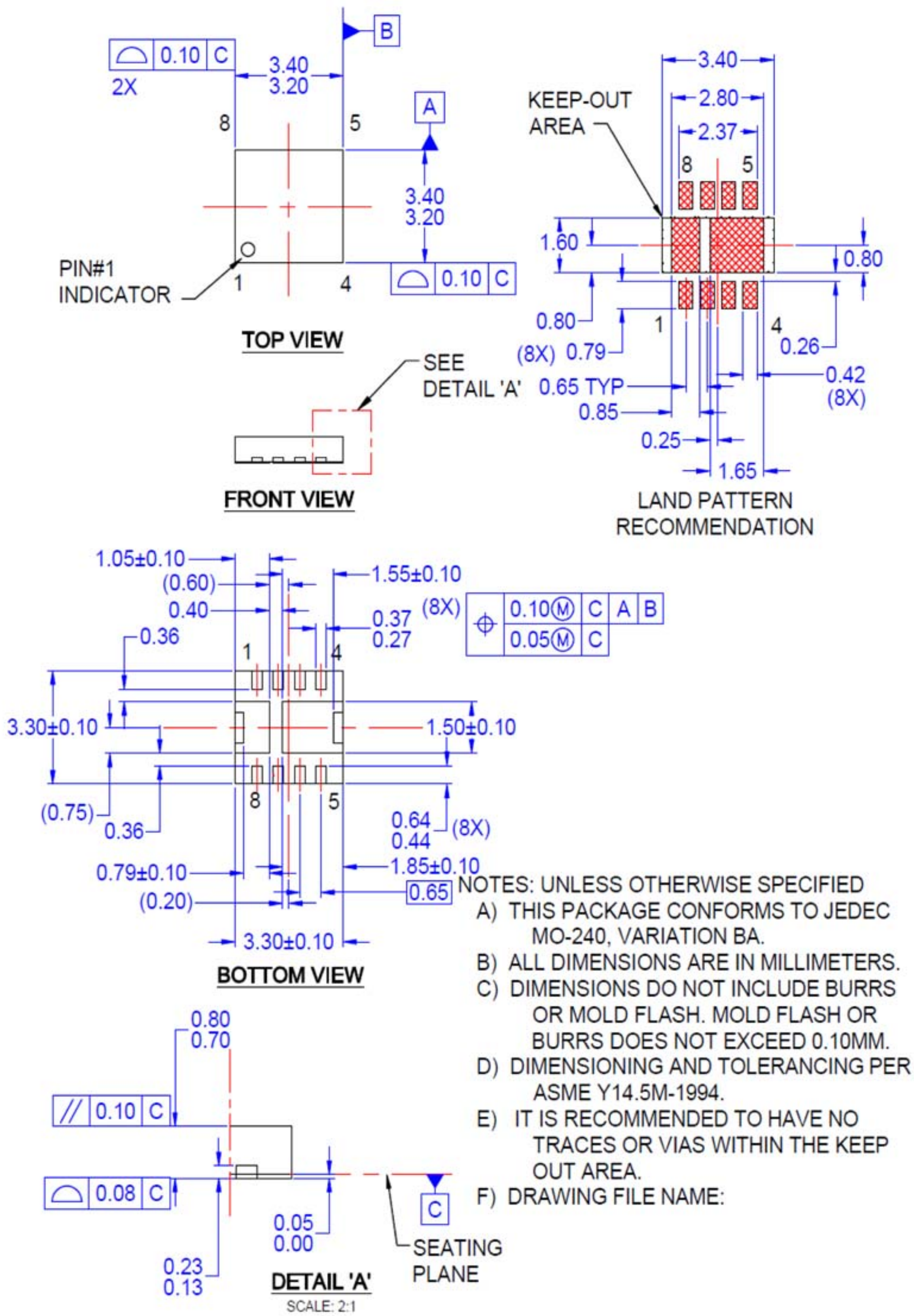
Figure 3 shows an example of a well designed layout. The discussion that follows summarizes the key features of this layout.

- "The input ceramic bypass capacitor between VIN and GND should be placed as close as possible to the pins V+ / V+(HSD) PAD and GND / GND(LSS) PAD to help reduce parasitic inductance and high frequency ringing. Several capacitors may be placed in parallel, and capacitors may be placed on both the top and bottom side of the board. The capacitor located immediately adjacent to the Power Clip will be the most effective at reducing HF parasitic. Caps located farther away, or on the opposite side of the board will also assist, but will be less effective due to increased trace inductance.
- "The Power Clip package design, with very short distance between pins V+ and GND, allows for a short connect distance to the input cap. This is a factor that enables the Power Clip switch loop to have very low parasitic inductance.
- "Use large copper areas on the component side to connect the V+ pin and V+ (HSD) pad, and the GND and GND(LSS) PAD.
- "The SW to inductor copper trace is a high current path. It will also be a high noise region due to switching voltage transients. The trace should be short and wide to enable a low resistance path and to minimize the size of the noise region. Care should be taken to minimize coupling of this trace to adjacent traces. The layout in Figure 3 shows a good example of this short, wide path.
- "The Power Trench® Technology MOSFETs used in the Power Clip are effective at minimizing SW node ringing. They incorporate a proprietary design[1] that minimizes the peak overshoot ring voltage on the switch node (SW). They allow the part to operate well within the breakdown voltage limits. For most layouts, this eliminates the need to add an external snubber circuit. If the designer chooses to use an RC snubber, it should be placed close to the part between the SW pins and GND / GND (LSS) PAD to dampen the high frequency ringing.
- "The Driver IC should be placed relatively closed to HSG pin and LSG pin to minimize G drive trace inductance. Excessive G trace length may slow the switching speed of the HS drive. And it may lead to excessive ringing on the LS G. If the designer must place the driver a significant distance away from the Power Clip, it would be a good practice to include a 0 Ohm resistor in the LS G path as a place holder. In the final design, if the LS G exhibits excessive LF ringing, efficiency can often be improved by changing this resistor to a few Ohms to dampen the LS G LF ringing.
- "The Power Clip has very good Junction-PCB heat transfer from all power pins. It has much better heat transfer Junction-GND (LSS) than traditional dual FET packages. In most cases, board ground will be the most effective heat transfer path on the PCB. Use a large copper area between GND / GND(LSS)PAD pins and board ground. To ensure the best thermal and electrical connection to ground, we recommend using multiple vias to interconnect ground plane layers as shown in Figure 3.

1.Patent Pending

- "Use multiple vias in parallel on each copper region to interconnect top, inner and bottom layers. This will reduce resistance and inductance of the vias and will improve thermal conductivity. Vias should be relatively large, around 8 mils to 10 mils.
- "Avoid using narrow thermal relief traces on the V+ / V+(HSD) PAD and GND / GND(LSS)PAD pins. These will increase HF switch loop inductance. And these will increase ringing of the HF power loop and the SW node.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MO-240, VARIATION BA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME:

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Rev. I61