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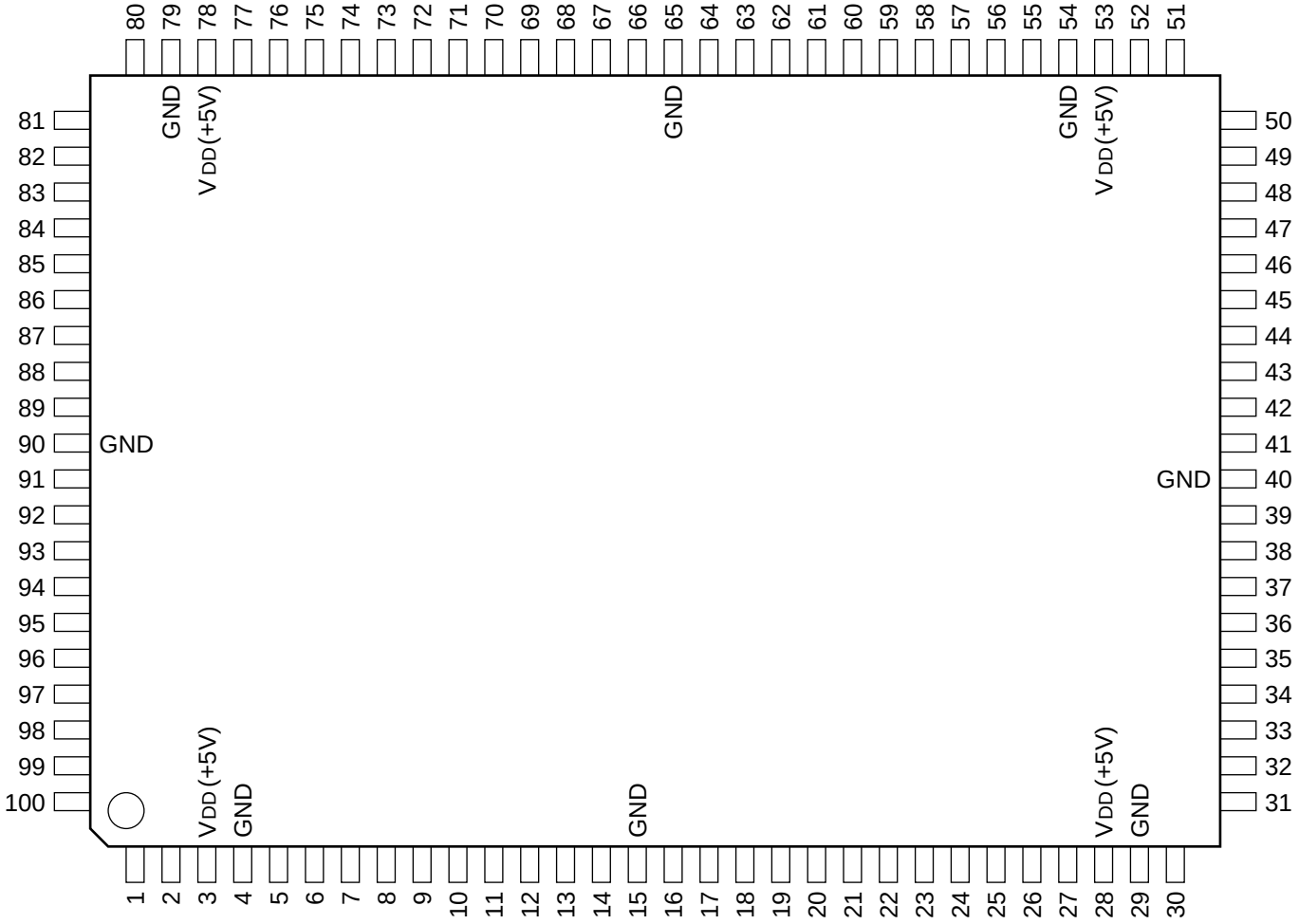
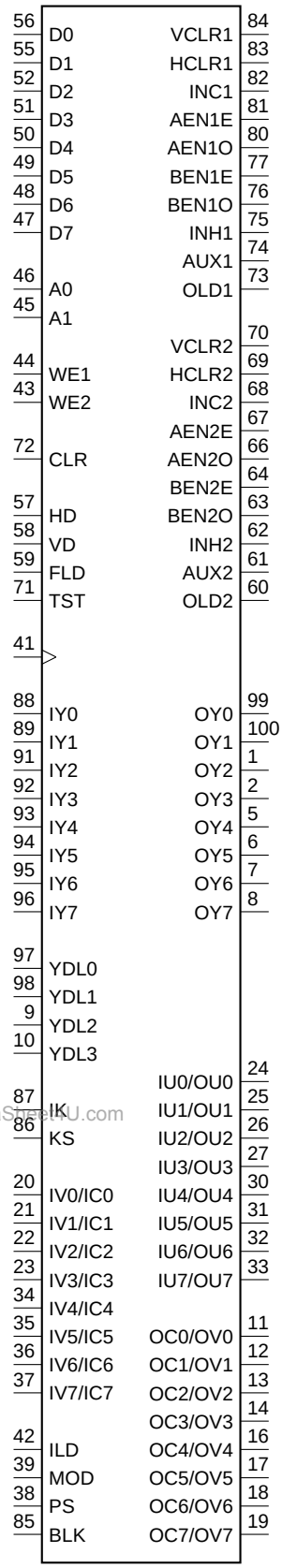
C-MOS MEMORY CONTROLLER FOR FRAME SYNCHRONIZER

- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	OY2	26	I/O	IU2/OU2	51	I	D3	76	O	BEN1O
2	O	OY3	27	I/O	IU3/OU3	52	I	D2	77	O	BEN1E
3	–	V_{DD}	28	–	V_{DD}	53	–	V_{DD}	78	–	V_{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	O	OY4	30	I/O	IU4/OU4	55	I	D1	80	O	AEN1O
6	O	OY5	31	I/O	IU5/OU5	56	I	D0	81	O	AEN1E
7	O	OY6	32	I/O	IU6/OU6	57	I	HD	82	O	INC1
8	O	OY7	33	I/O	IU7/OU7	58	I	VD	83	O	HCLR1
9	I	YDL2	34	I	IV4/IC4	59	I	FLD	84	O	VCLR1
10	I	YDL3	35	I	IV5/IC5	60	O	OLD2	85	I	BLK
11	O	OC0/OV0	36	I	IV6/IC6	61	O	AUX2	86	I	KS
12	O	OC1/OV1	37	I	IV7/IC7	62	O	INH2	87	I	IK
13	O	OC2/OV2	38	I	PS	63	O	BEN2O	88	I	IY0
14	O	OC3/OV3	39	I	MOD	64	O	BEN2E	89	I	IY1
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	OC4/OV4	41	I	CK	66	O	AEN2O	91	I	IY2
17	O	OC5/OV5	42	I	ILD	67	O	AEN2E	92	I	IY3
18	O	OC6/OV6	43	I	WE2	68	O	INC2	93	I	IY4
19	O	OC7/OV7	44	I	WE1	69	O	HCLR2	94	I	IY5
20	I	IV0/IC0	45	I	A1	70	O	VCLR2	95	I	IY6
21	I	IV1/IC1	46	I	A0	71	I	TST	96	I	IY7
22	I	IV2/IC2	47	I	D7	72	I	CLR	97	I	YDL0
23	I	IV3/IC3	48	I	D6	73	O	OLD1	98	I	YDL1
24	I/O	IU0/OU0	49	I	D5	74	O	AUX1	99	O	OY0
25	I/O	IU1/OU1	50	I	D4	75	O	INH1	100	O	OY1



INPUT

A0, A1 ; ADDRESS BUS
BLK ; BLANKING
CK ; CLOCK
CLR ; CLEAR
D0-D7 ; DATA BUS
FLD ; FIELD (L ; EVEN, H ; ODD)
HD ; HOLIZONTAL SYNCHRONIZED
IK ; 1 BIT KEY
ILD ; LOAD
IV0/IC0-IV7/IC7 ; PARALLEL DATA INPUT OF V DATA AT PARALLEL-SERIAL MODE,
SERIAL DATA INPUT OF UV DATA AT SERIAL-PARALLEL MODE.
IY0-IY7 ; Y DATA BUS
KS ; KEY SELECT
MOD ; MODE SELECT (L ; 4:1:1 MODE, H : 4:2:2 MODE)
PS ; PARALLEL-SERIAL / SERIAL-PARALLEL SELECT (L ; S → P, H ; P → S)
TST ; TEST
VD ; VERTICAL SYNCHRONIZED
WE1, WE2 ; WRITE ENABLE
YDL0-YDL3 ; Y DATA DELAY

OUTPUT

AEN1E, AEN2E ; A CH EVEN FIELD ENABLE
BEN1E, BEN2E ; B CH EVEN FIELD ENABLE
AEN1O, AEN2O ; A CH ODD FIELD ENABLE
BEN1O, BEN2O ; B CH ODD FIELD ENABLE
AUX1, AUX2 ; MODE 0,1 ; MSB (AUX BIT) OUTPUT OF MD 1·2 REGISTER.
MODE 2 ; HIGH BIT OUTPUT OF LOAD COUNTER.
MODE 3 ; H LEVEL OUTPUT OF LINE NUMBER SET AT VC1·2 REGISTER EVERY V RESET.
H LEVEL OUTPUT AT ALL TIMES WHEN VC1·2=0.
HCLR1, HCLR2 ; HOLIZONTAL CLEAR
INC1, INC2 ; LINE INCREMENT
INH1, INH2 ; INHIBIT
OC0/OV0-OC7/OV7 ; SERIAL DATA OUTPUT OF UV DATA AT PARALLEL-SERIAL MODE,
PARALLEL DATA OUTPUT OF V DATA AT SERIAL-PARALLEL MODE.
OLD1, OLD2 ; MODE 0 ; L LEVEL WHEN LOAD COUNTER OUTPUT IS 0 AT LOAD SIGNAL FOR 4:1:1 MODE OF UV DATA CONVERTER.
MODE 1,2 ; LOW BIT OUTPUT OF LOAD COUNTER AT LOAD SIGNAL FOR 4:2:2 MODE OF UV DATA CONVERTER.
MODE 3 ; H LEVEL OUTPUT OF CLOCK NUMBER SET AT LD1·2 REGISTER EVERY H RESET.
H LEVEL OUTPUT AT ALL TIMES WHEN LD1·2=0.
H LEVEL OUTPUT WHEN AUX1·2 (MODE 3) IS H LEVEL.
OY0-OY7 ; Y DATA BUS
VCLR1, VCLR2 ; VERTICAL CLEAR

INPUT/OUTPUT

IU0/OU0-IU7/OU7 ; SERIAL DATA OUTPUT OF U DATA AT PARALLEL-SERIAL MODE,
PARALLEL DATA OUTPUT OF U DATA AT SERIAL-PARALLEL MODE.