
4AM12

Silicon N-Channel/P-Channel Power MOS FET Array

HITACHI

ADE-208-1210 (Z)

1st. Edition

Mar. 2001

Application

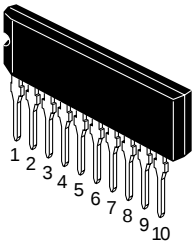
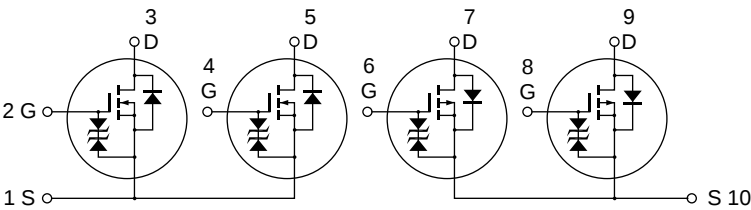
High speed power switching

Features

- Low on-resistance
N-channel: $R_{DS(on)} \leq 0.075$, $V_{GS} = 10$ V, $I_D = 4$ A
P-channel: $R_{DS(on)} \leq 0.12$, $V_{GS} = -10$ V, $I_D = -4$ A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline

SP-10



1, 10. Source
2, 4, 6, 8. Gate
3, 5, 7, 9. Drain

Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

Item	Symbol	Rating		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	-60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	8	-8	A
Drain peak current	$I_{D(pulse)}^{*1}$	32	-32	A
Body to drain diode reverse drain current	I_{DR}	8	-8	A
Channel dissipation	$Pch (Tc = 25^{\circ}C)^{*2}$	28		W
Channel dissipation	Pch^{*2}	4		W
Channel temperature	Tch	150		°C
Storage temperature	$Tstg$	-55 to +150		°C

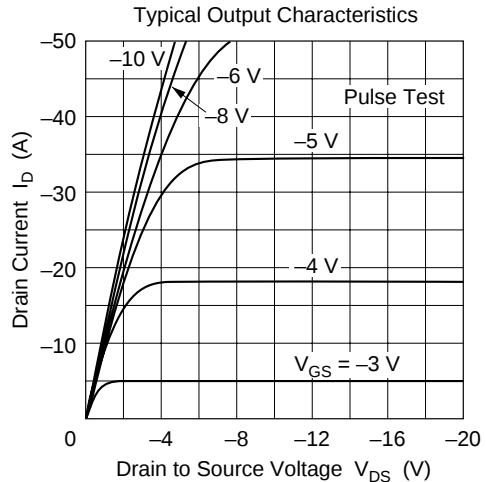
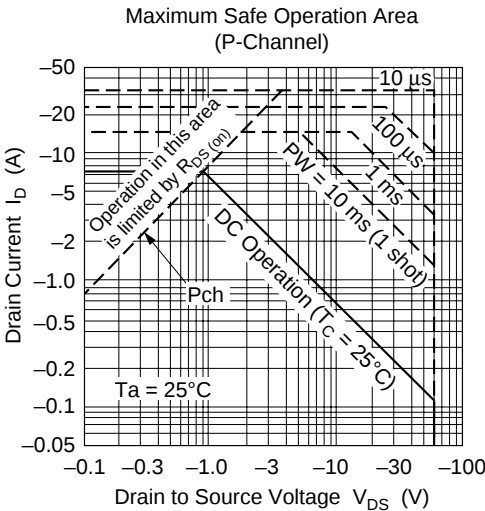
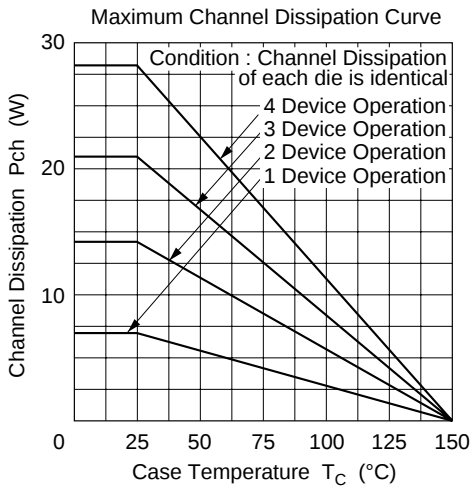
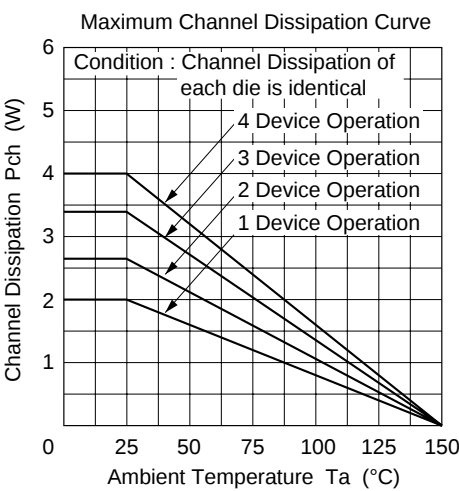
Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. 4 Devices operation

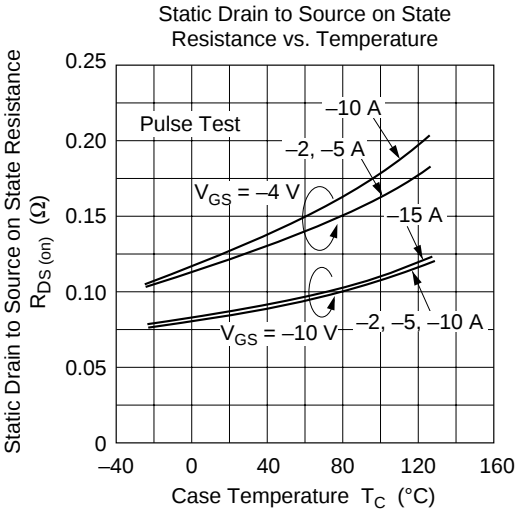
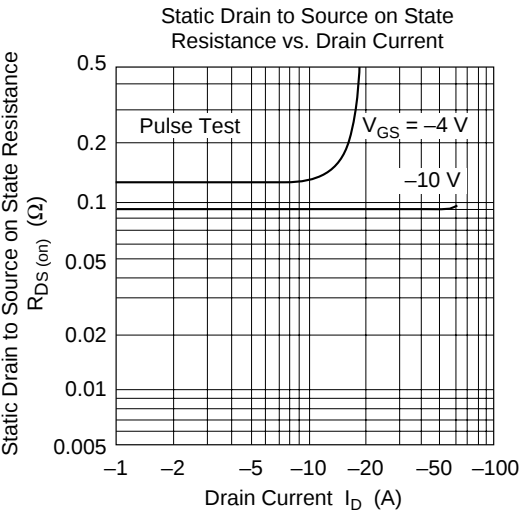
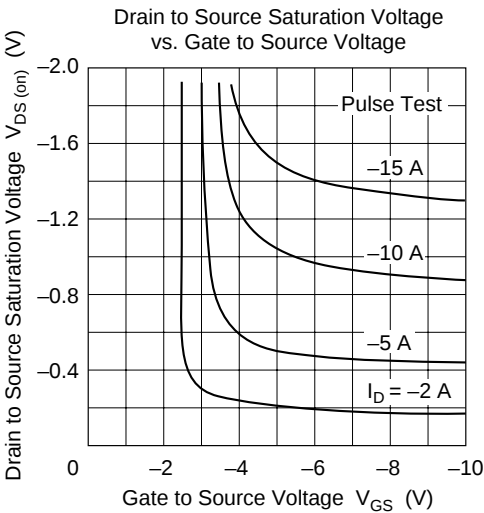
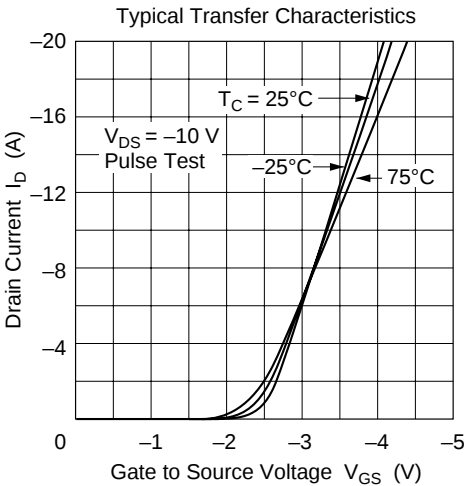
Electrical Characteristics (Ta = 25°C) (1 Unit)

Item	Symbol	N channel			P channel			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	−60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	μA	$I_G = \pm 100 \text{ μA}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	−250	V	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	−1.0	—	−2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.075	—	0.09	0.12	Ω	$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
		—	0.08	0.11	—	0.12	0.18	Ω	$I_D = 4 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	5.5	9.0	—	5.5	7.5	—	S	$I_D = 4 \text{ A}, V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	860	—	—	1400	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	450	—	—	720	—	pF	
Reverse transfer capacitance	C_{rss}	—	140	—	—	220	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	—	15	—	ns	$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V},$ $R_L = 7.5 \text{ Ω}$
Rise time	t_r	—	45	—	—	90	—	ns	
Turn-off delay time	$t_{d(off)}$	—	200	—	—	250	—	ns	
Fall time	t_f	—	100	—	—	150	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.05	—	—	−1.05	—	V	$I_F = 8 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	110	—	—	180	—	ns	$I_F = 8 \text{ A}, V_{GS} = 0,$ $dI_F/dt = 50 \text{ A/μs}$

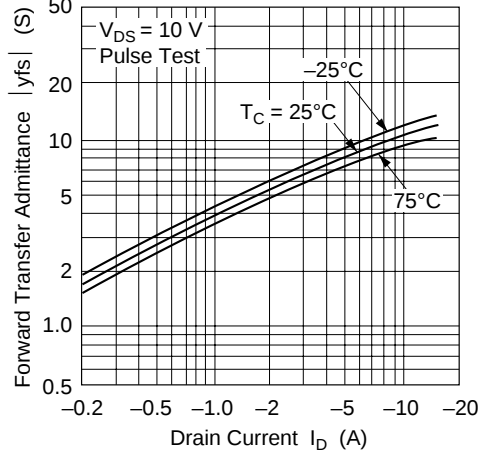
Note: 1. Pulse Test

Polarity of test conditions for P channel device is reversed.

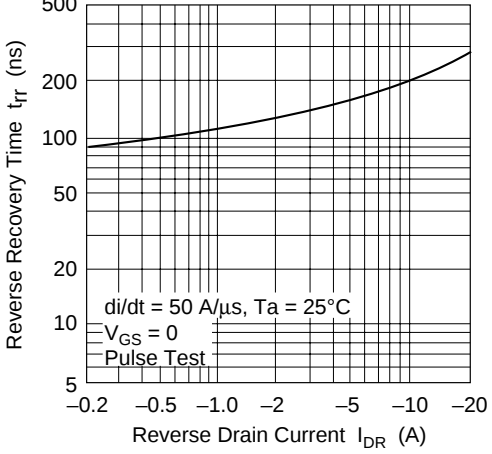




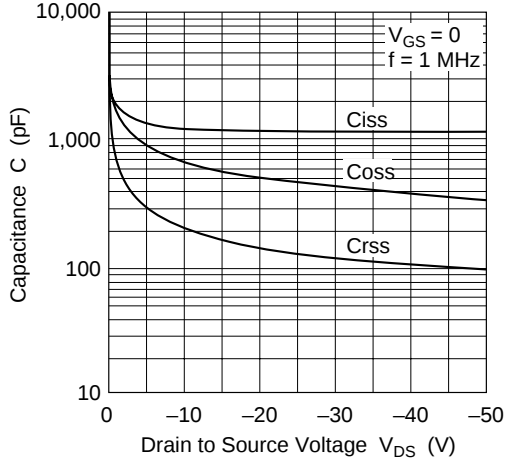
Forward Transfer Admittance
vs. Drain Current



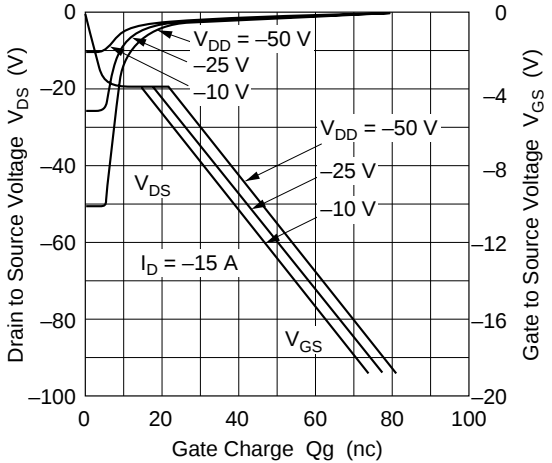
Body to Drain Diode Reverse
Recovery Time



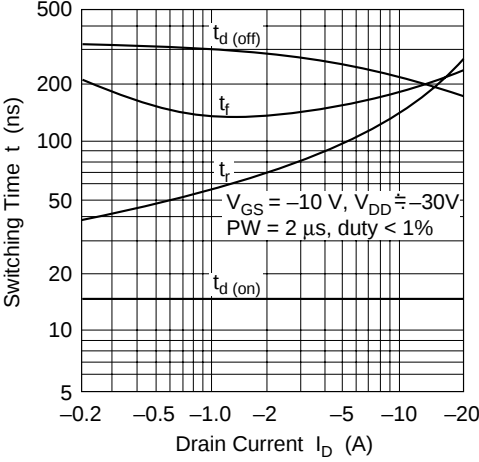
Typical Capacitance vs.
Drain to Source Voltage



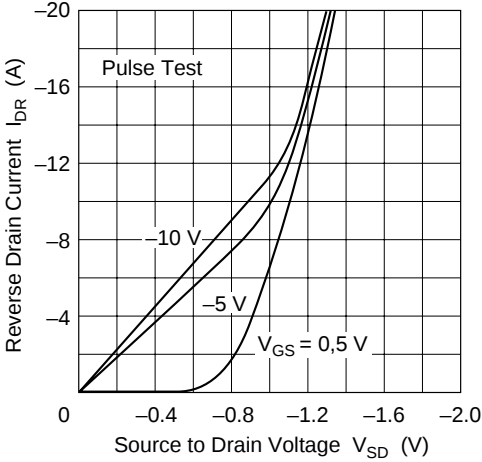
Dynamic Input Characteristics

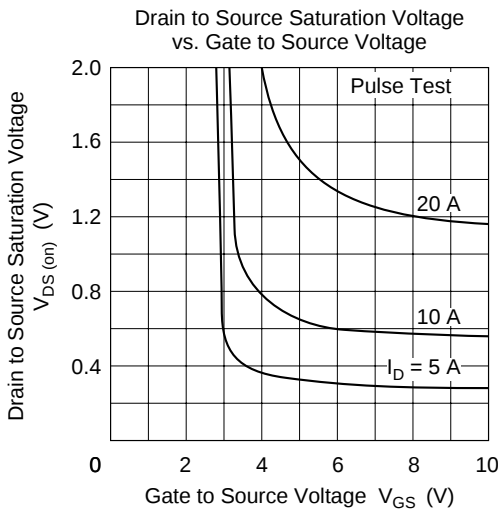
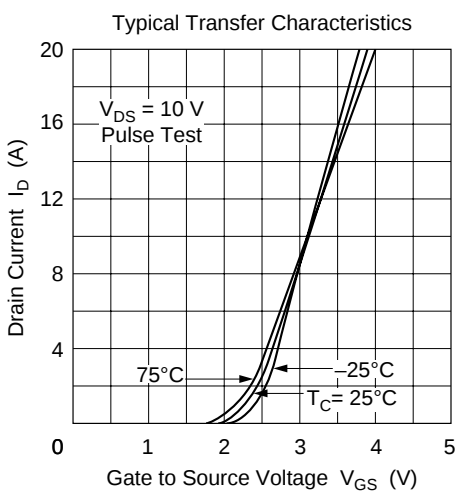
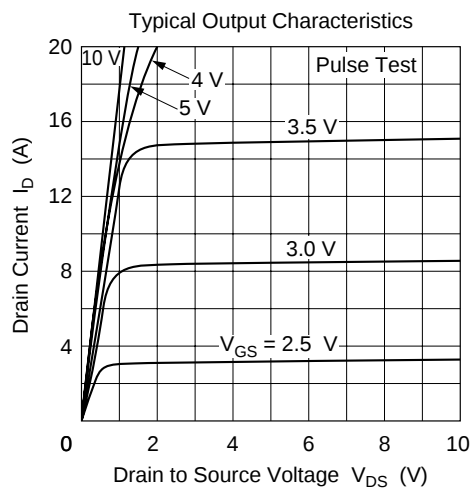
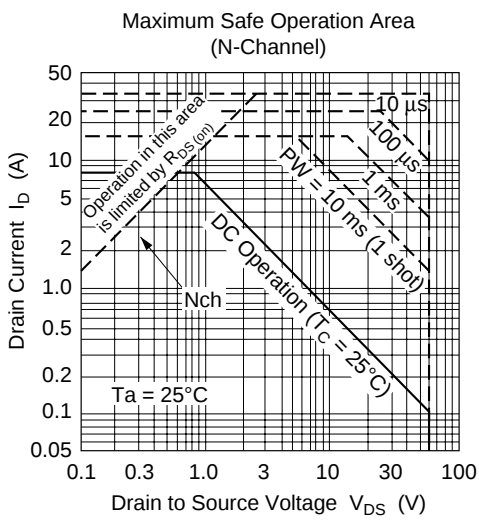


Switching Characteristics

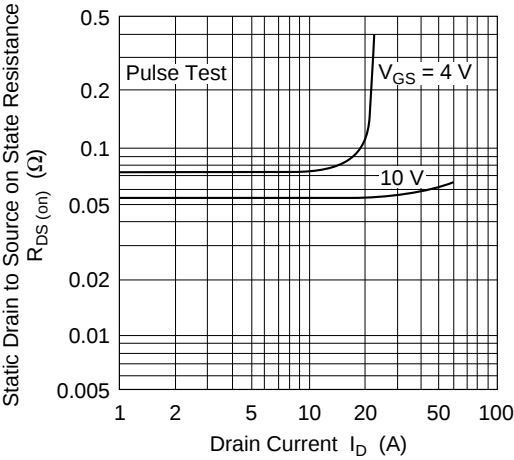


Reverse Drain Current vs. Source to Drain Voltage

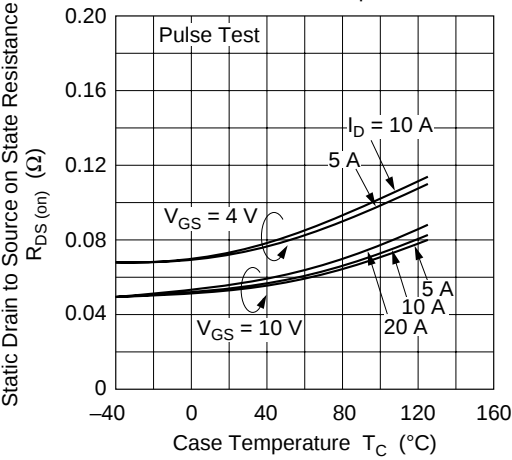




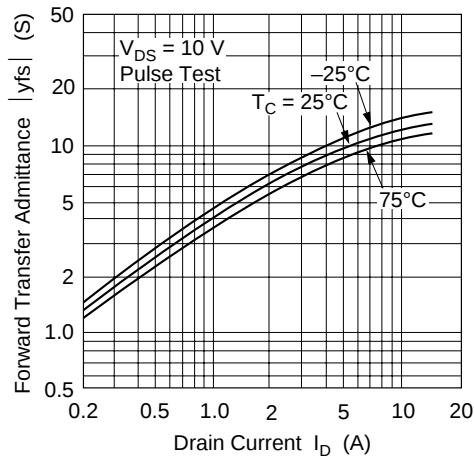
Static Drain to Source on State Resistance vs. Drain Current



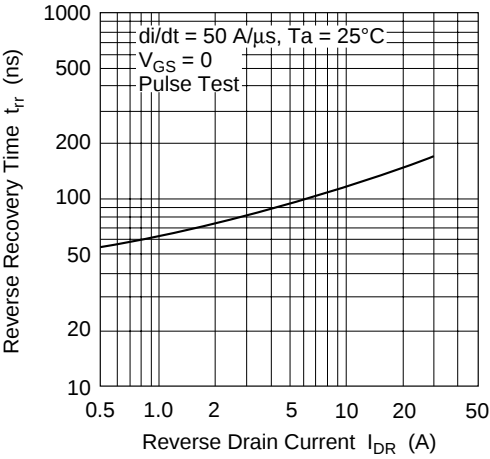
Static Drain to Source on State Resistance vs. Temperature



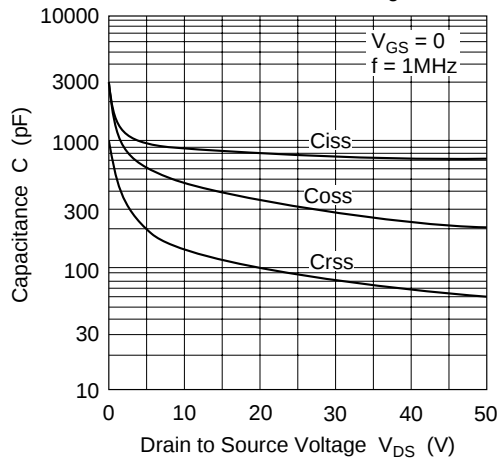
Forward Transfer Admittance vs. Drain Current



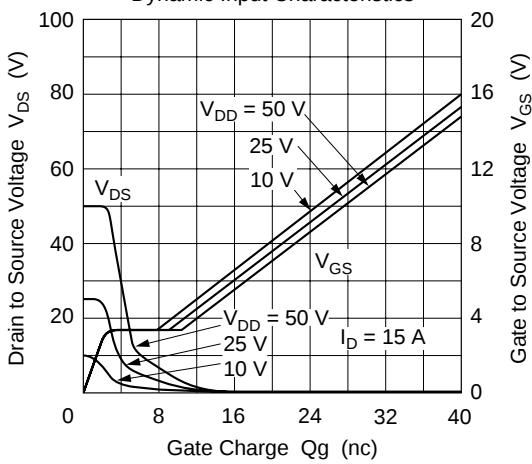
Body to Drain Diode Reverse Recovery Time



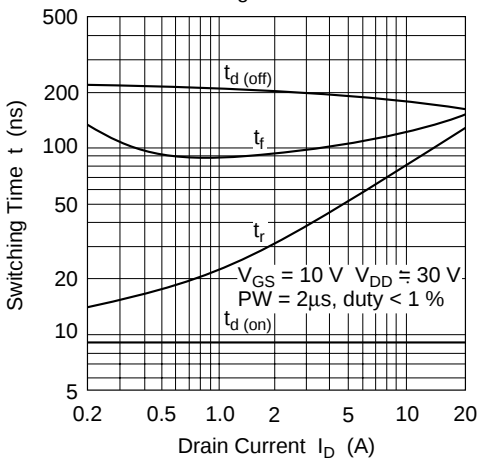
Typical Capacitance vs.
Drain to Source Voltage



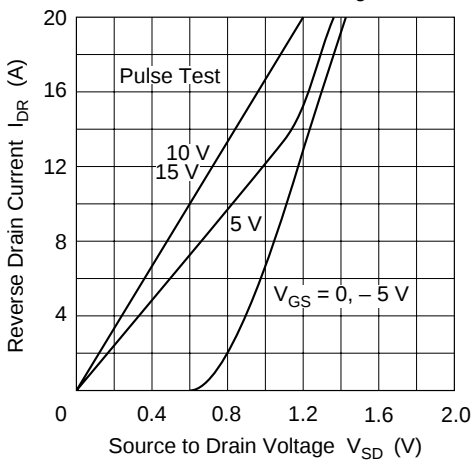
Dynamic Input Characteristics



Switching Characteristics

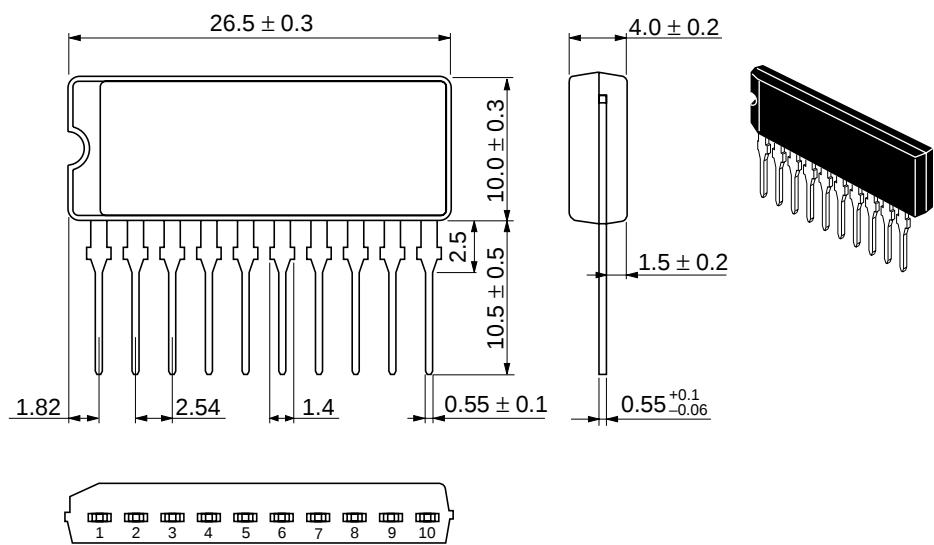


Reverse Drain Current vs.
Source to Drain Voltage



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	SP-10
JEDEC	—
EIAJ	—
Mass (reference value)	2.9 g

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