

### Features

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion...0.003% Typ
- Low Noise  $V_n = 18nV/\sqrt{Hz}$  Typ at  $f = 1kHz$
- High Input Impedance...JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate...13V/ $\mu s$  Typ
- Common-Mode Input Voltage Range Includes  $V_{CC+}$
- SOP-8L: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

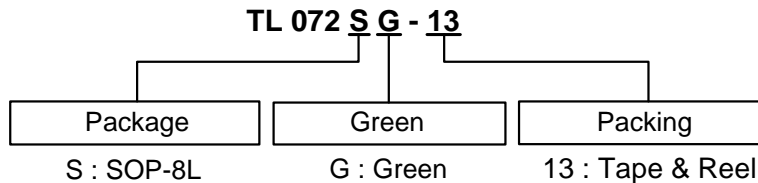
### General Description

The JFET-input operational amplifiers in the TL072 are similar to the TL082, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL072 ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

### Applications

- Active filters
- Audio pre-amps

### Ordering Information



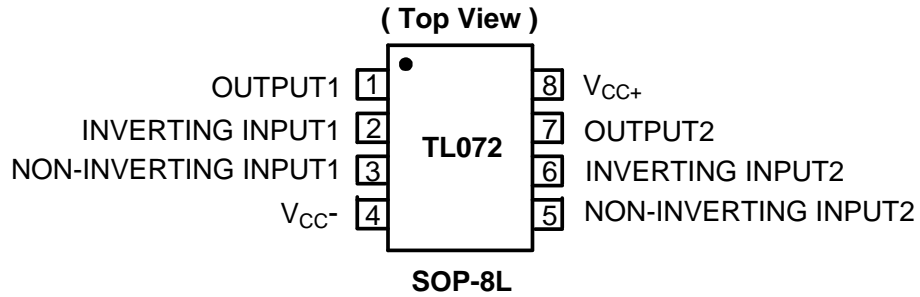
Device	Package Code	Packaging (Note 2)	13" Tape and Reel	
			Quantity	Part Number Suffix
TL072SG-13	S	SOP-8L	2500/Tape & Reel	-13



Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html)  
 2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

**Pin Assignments**

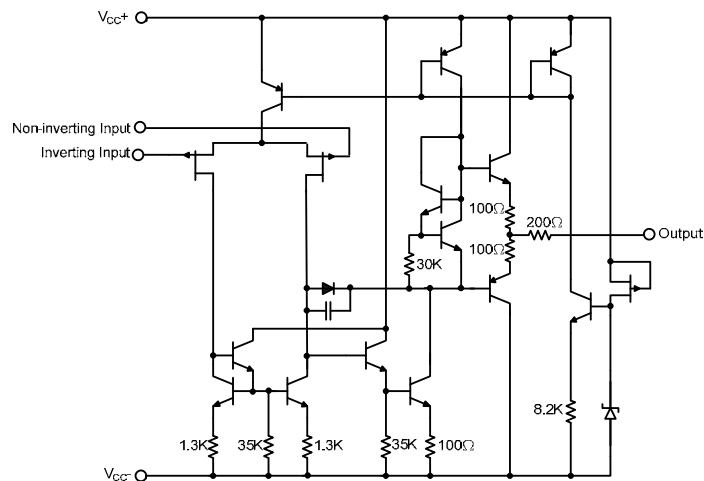
(1) Dual channel SOP-8L



**Pin Descriptions**

Pin Name	Pin No.	Description
OUTPUT1	1	Channel 1 Output
INVERTING INPUT1	2	Channel 1 Inverting Input
NON-INVERTING INPUT1	3	Channel 1 Non-inverting Input
$V_{CC-}$	4	Supply Voltage
NON-INVERTING INPUT2	5	Channel 2 Non-inverting Input
INVERTING INPUT2	6	Channel 2 Inverting Input
OUTPUT2	7	Channel 2 Ouput
$V_{CC+}$	8	Supply Voltage

**Block Diagram**



**Absolute Maximum Ratings (Note 8)**

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
$V_{CC+}$	Supply Voltage + (Note 3)	+18	V
$V_{CC-}$	Supply Voltage - (Note 3)	-18	V
$V_I$	Input voltage (Notes 3 and 5)	$\pm 15$	V
$V_{ID}$	Differential input Voltage, $V_{ID}$ (Note 4)	$\pm 30$	V
	Duration of output short circuit (Note 6)	Unlimited	
$P_D$	Power Dissipation (Note 7)	860	mW
$T_J$	Operating Junction Temperature Range	150	$^{\circ}\text{C}$
$T_{ST}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$

- Notes:
3. ALL voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  4. Differential voltage are at the non-inverting input terminal with respect to the inverting input terminal.
  5. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less.
  6. The output may be shorted to ground or either supply. Temperature and/or supply voltage must be limited to ensure that the dissipation rating is not exceeded.
  7. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A) / \theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150 $^{\circ}\text{C}$  can affect reliability

**Recommended Operating Conditions (Note 8)**

Symbol	Description	Rating	Unit
$V_{CC\pm}$	Supply Voltage	$\pm 15$	V
$T_A$	Operating Ambient Temperature Range	-40 to +85	$^{\circ}\text{C}$

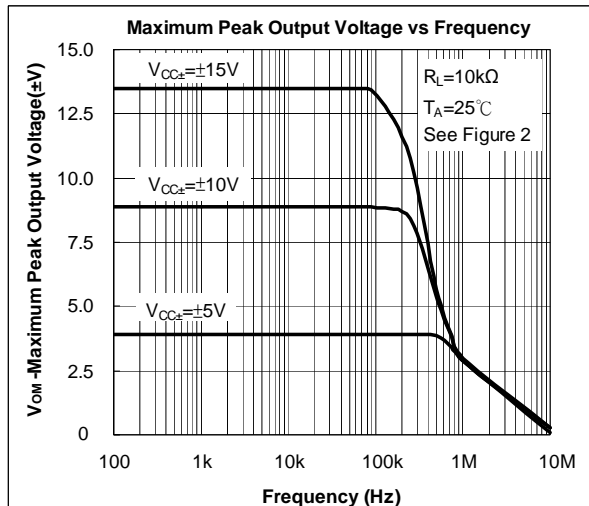
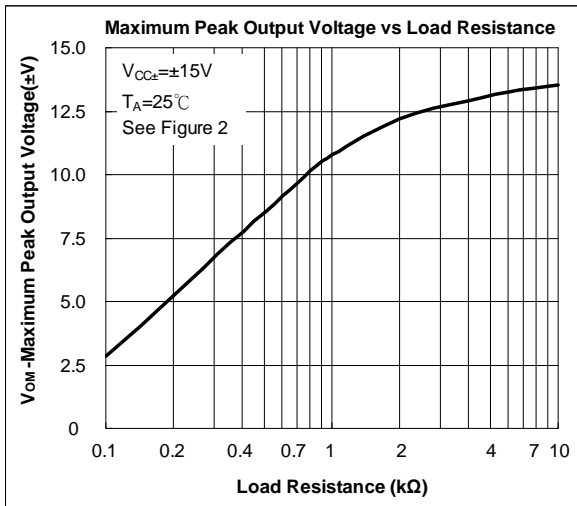
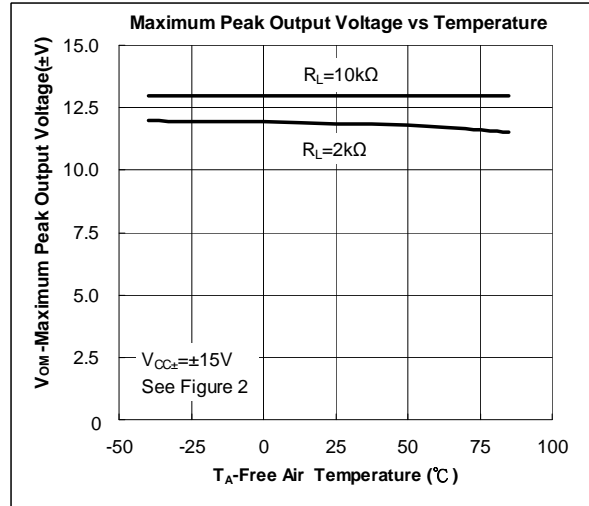
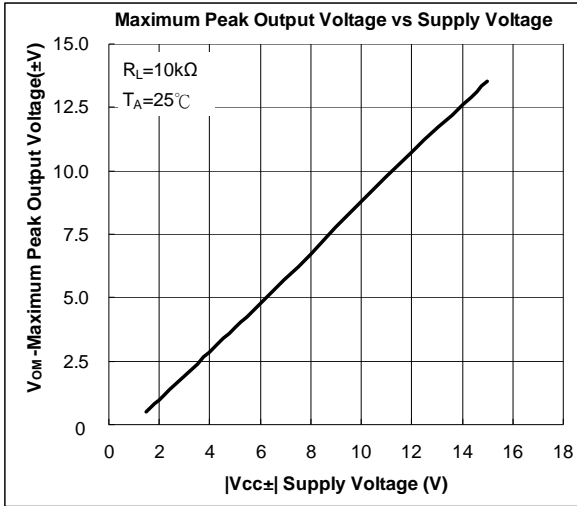
- Notes:
8. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Electrical Characteristics** ( $V_{CC\pm} = \pm 15V$ ,  $T_A = 25^\circ C$ ; unless otherwise noted)

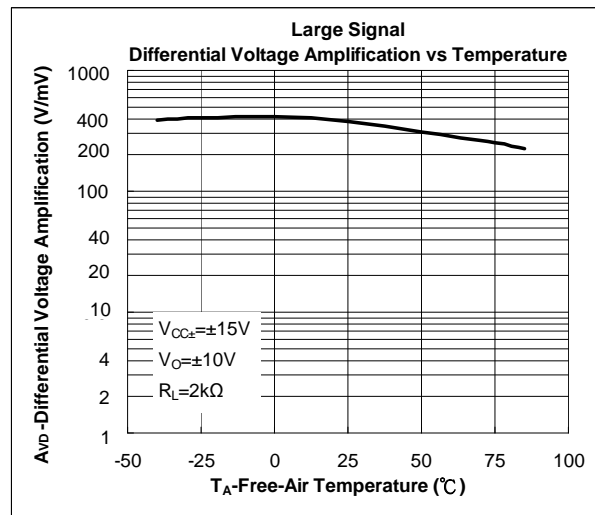
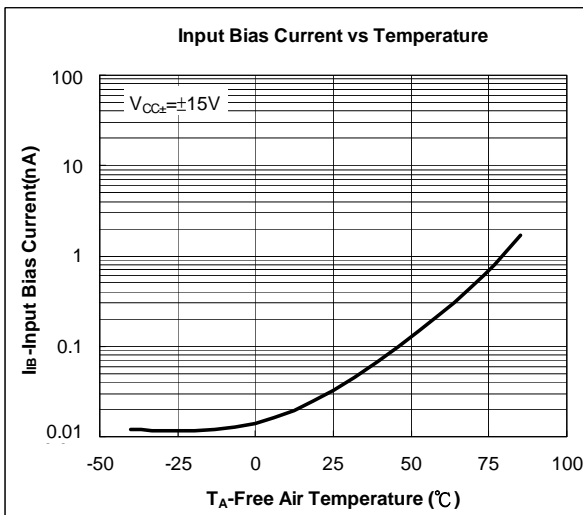
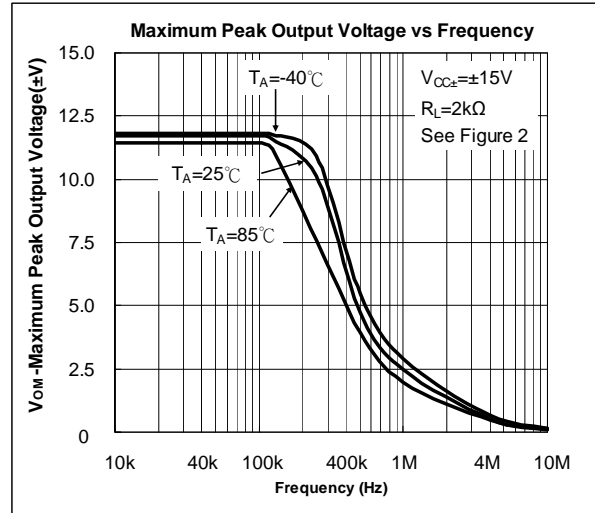
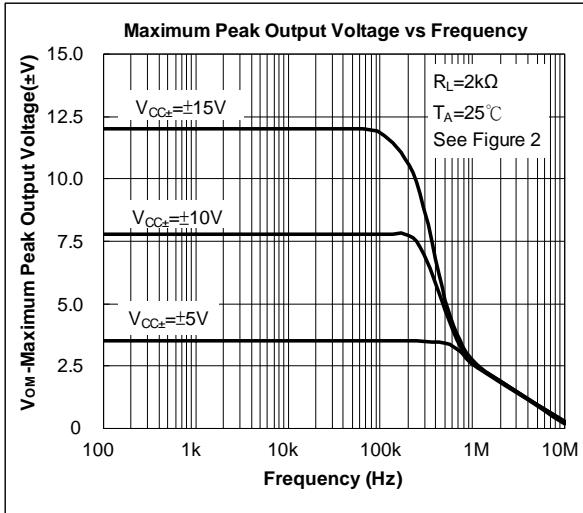
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit		
$V_{IO}$	Input Offset Voltage	$V_O=0$ , $R_S=50\Omega$	$T_A=25^\circ C$		3	6	mV	
			$T_A=$ full range			8		
$\alpha_{V_{IO}}$	Temperature Coefficient of Input Offset Voltage	$V_O=0$ , $R_S=50\Omega$ , $T_A=$ full range		18		$\mu V/^\circ C$		
$I_{IO}$	Input Offset Current	$V_O=0$	$T_A=25^\circ C$		5	100	pA	
			$T_A=$ full range			2	nA	
$I_{IB}$	Input Bias Current	$V_O=0$	$T_A=25^\circ C$		65	200	pA	
			$T_A=$ full range			20	nA	
$V_{ICR}$	Common Mode Input Voltage Range		$\pm 11$	-12~+15		V		
$V_{OM}$	Maximum Peak Output Voltage Swing	$R_L=10k\Omega$ , $T_A=25^\circ C$		$\pm 12$	$\pm 13.5$		V	
			$R_L \geq 10k\Omega$ ,	$T_A=$ full range	$\pm 12$			
			$R_L \geq 2k\Omega$		$\pm 10$			
$A_{VD}$	Large Signal Differential Voltage Amplification	$V_O=\pm 10V$ , $R_L \geq 2k\Omega$	$T_A=25^\circ C$	50	200		V/mV	
			$T_A=$ full range	25				
$B_1$	Unity Gain Bandwidth			3		MHz		
$r_i$	Input Resistance	$T_A=25^\circ C$		$10^{12}$		$\Omega$		
CMRR	Common Mode Rejection Ratio	$V_{IC}=V_{ICRmin}$ , $V_O=0$ $R_S=50\Omega$ , $T_A=25^\circ C$	75	100		dB		
$k_{SVR}$	Supply Voltage Rejection Ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC}=\pm 9$ to $\pm 15V$ $V_O=0$ $R_S=50\Omega$ , $T_A=25^\circ C$	80	100		dB		
$I_{CC}$	Supply Current (each amplifier)	$V_O=0$ , $T_A=25^\circ C$ No load		1.4	2.5	mA		
$V_{O1}/V_{O2}$	Crosstalk Attenuation	$A_{VD}=100$ , $T_A=25^\circ C$		120		dB		
SR	Slew Rate at Unity Gain	$V_I=10V$ , $C_L=100pF$ , $R_L=2k\Omega$ (See Figure 1)	8	13		V/ $\mu s$		
tr	Rise Time	$V_I=20mV$ , $R_L=2k\Omega$ , $C_L=100pF$ (See Figure 1)		0.1		$\mu s$		
	Overshoot Factor			20		%		
$V_n$	Equivalent Input Noise Voltage	$R_S=20\Omega$	f=1kHz		18	$nV/\sqrt{Hz}$		
			f=10 Hz to 10kHz		4	$\mu V$		
$I_n$	Equivalent Input Noise Current	$R_S=20\Omega$ , f=1kHz		0.01		$pA/\sqrt{Hz}$		
THD	Total Harmonic Distortion	$V_{I rms}=6V$ , $A_{VD}=1$ , $R_L \geq 2k\Omega$ , $R_S \leq 1k\Omega$ , f=1kHz		0.003		%		
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SOP-8L (Note 9)		145		$^\circ C/W$		
$\theta_{JC}$	Thermal Resistance Junction-to-Case	SOP-8L (Note 9)		35		$^\circ C/W$		

Notes: 9. Test condition for SOP-8L: Devices mounted on FR-4 substrate PC board, with minimum recommended pad layout.

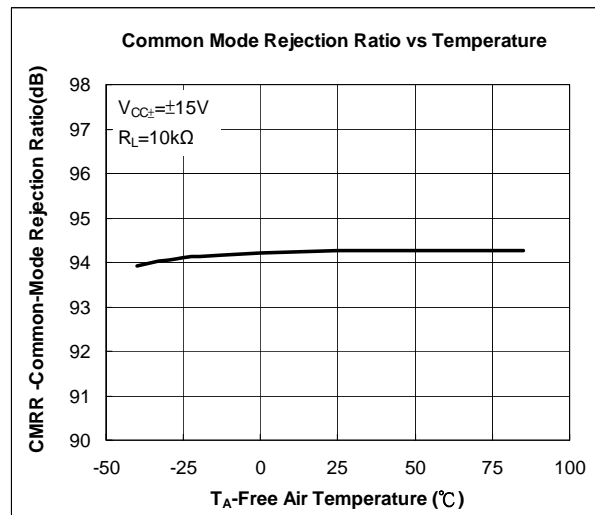
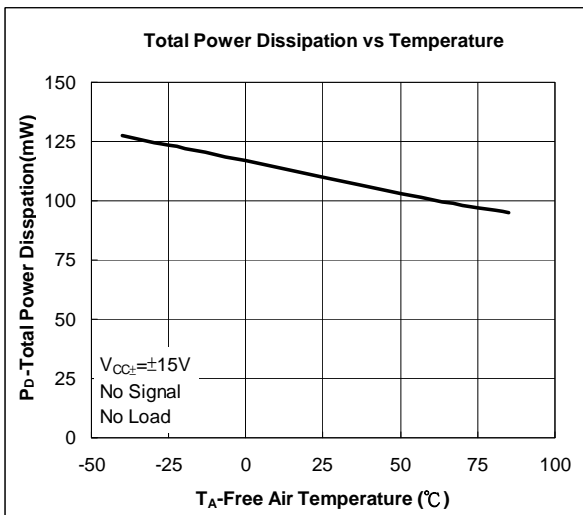
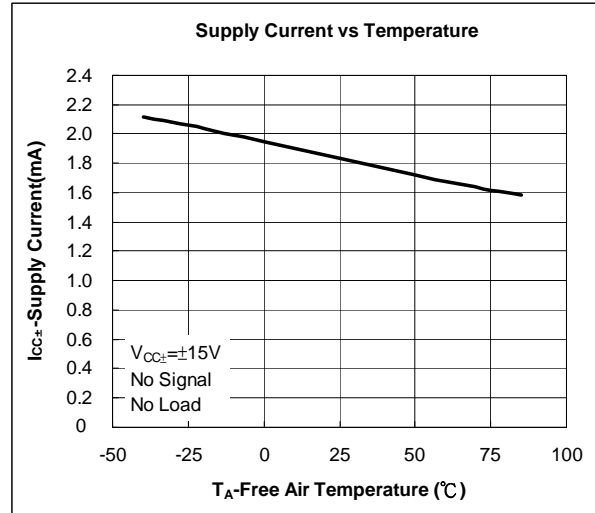
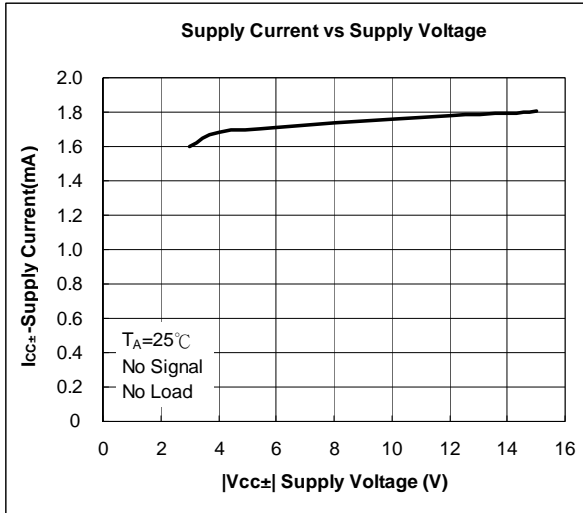
**Typical Performance Characteristics**



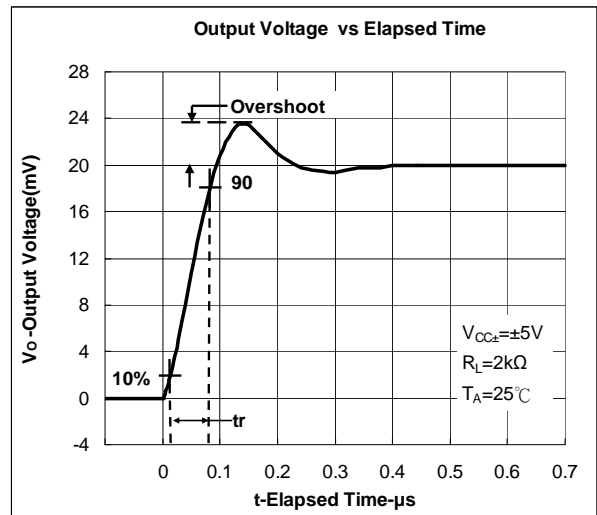
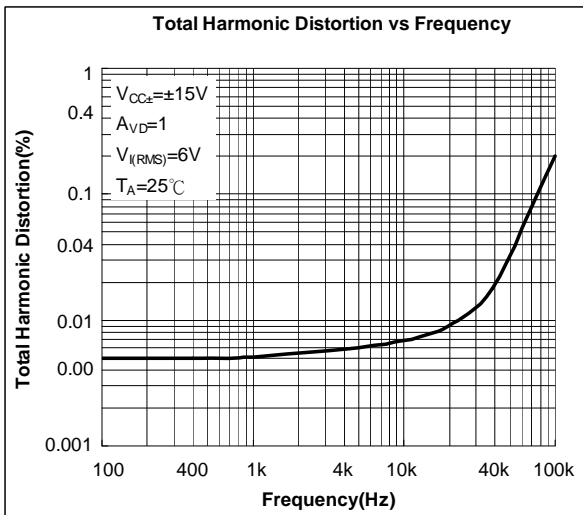
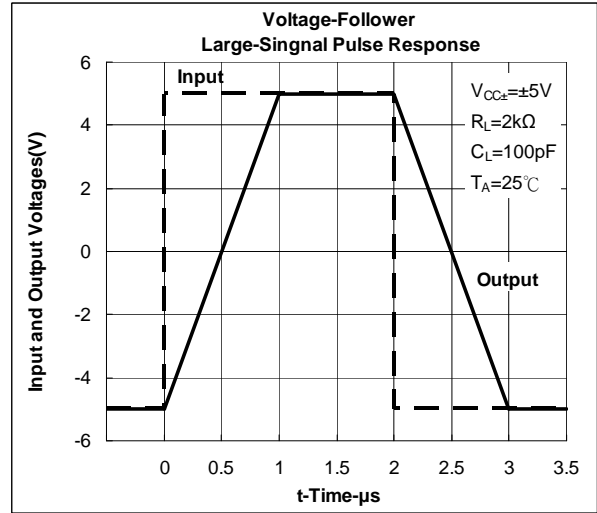
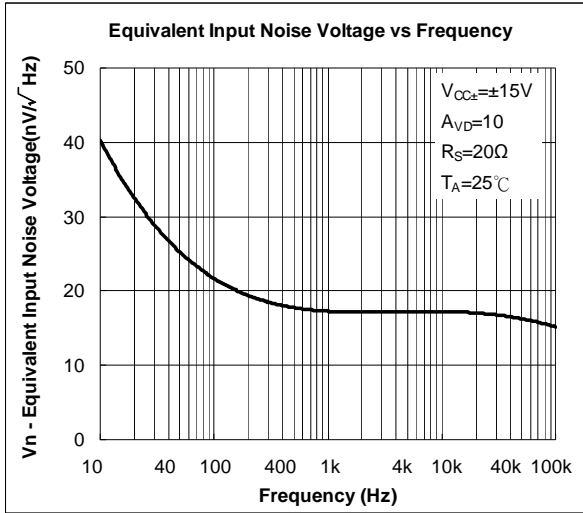
**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**





**Test Circuit**

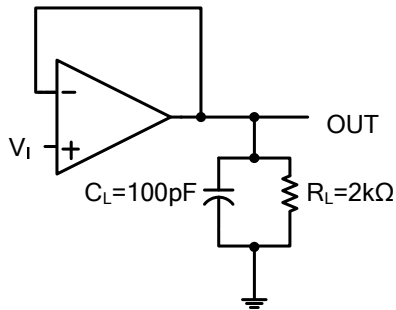


Figure 1. Unity-Gain Amplifier

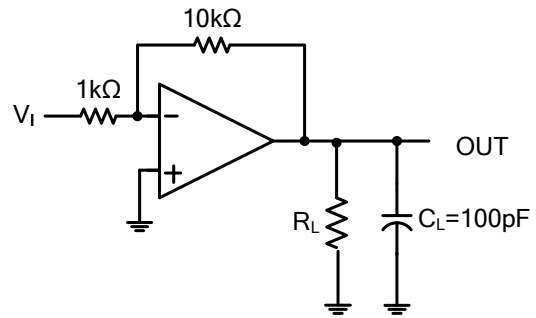
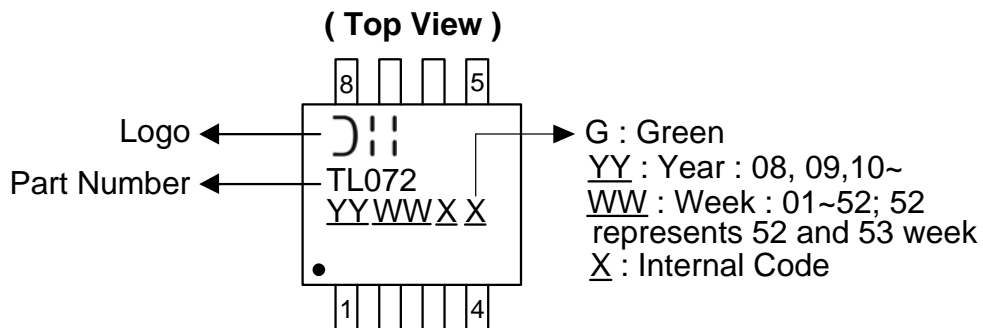


Figure 2. Gain-of-10 Inverting Amplifier

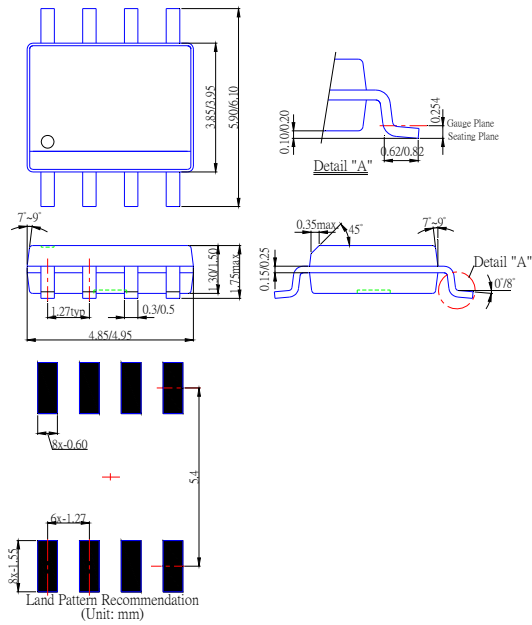
**Marking Information**

(1) SOP-8L



**Package Information ( All Dimensions in mm )**

**(1) Package type: SOP-8L**



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