LCD MODULE

(DEPARTMENT)

SPECIFICATION

T4880C03WP01 – REV. A

(480 x 800 RGB TFT 7.0”)

CUSTOMER APPROVAL

……
STAMP AND SIGNATURE

DATE: _____

IMPORTANT NOTE: This document must be approved by customer and send back to CCT by mail, email or fax.
If the approved document is not returned, CCT will assume it has been approved if any Mass Production Order is issued subsequently.

	Designation	Name	Signature/Date
Originator	**Electronic Engineer**	**Christopher Choong**	**27.02.07**
Checked by	**Electronic Engineer**	**Zuriana Zulkifli**	**27.02.07**
Approved by	**Project Manager**	**Azhar Rosdi**	**27.02.07**

LCD Module Specification

1.0 Table of Contents

2.0 Record of revision

Rev	Date	Item	Page	Comment
A	27/02/07			Initial release

3.0 General specification

Display format	: 800 (W) x RGB x 480 (H) dots
Color	: 262k colors
Screen size	: 7.0 inch
Surface treatment	: Anti-glare
Active area	: 152.40mm x 91.44mm
General dimensions	: 165.00mm x 104.00mm x 5.50mm
Pixel pitch	: 0.1905mm x 0.1905mm
Controller	: None

LCD type : ☐ CSTN ☒ TFT ☐ OLED

Polarizer mode : ☐ Reflective ☐ Transflective

☒ Transmissive

View angle : ☒ 6 O' clock ☐ 12 O'clock

☐ 9 O'clock ☐ 3 O'clock

Backlight : ☐ NONE ☒ LED ☐ CCFL

Backlight color : ☐ Yellow Green ☐ Amber ☒ White

☐ Blue Green ☐ Others

Temperature range : ☐ Normal temperature ☒ Wide temperature

Operating 0 to 50 C Operating –30 to 85 C

Storage –20 to 70 C Storage –40 to 95 C

4.0 Absolute maximum rating (Ta = 25 °C)

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	V_{CC}	+2.5	+3.6	V	
	AV_{DD}	-0.3	+3.9	V	
	V_{GH}	-0.3	+20.0	V	
	V_{GL}	-13.0	+0.3	V	
	$V_{GH} - V_{GL}$	-	33	V	

Notes:

1. The absolute maximum rating values of this product must not be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently damaged.

5.0 Electrical characteristics (At Ta = 25 °C, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (logic)	V_{CC}	3.0	3.3	3.6	V
Supply voltage (analog)	AV_{DD}	-	(10.0)	-	V
Gate ON voltage	V_{GH}	-	(16.0)	-	V
Gate OFF voltage	V_{GL}	-	(-7.0)	-	V
Common electrode voltage	V_{COM}	-	3.6	-	V
Input logic high voltage	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V
Input logic low voltage	V_{IL}	0	-	$0.3V_{CC}$	V
Supply current (driver)	I_{DD}	-	(25.0)	50.0	mA
	I_{CC}	-	(4.0)	10.0	mA
	I_{GH}	-	(0.2)	0.5	mA
	I_{GL}	-	(0.2)	1.0	mA
LED voltage	V_{LED}	-	9.6	12.0	V
LED current	I_{LED}	-	20	-	mA
LED lifetime		20,000	-	-	Hr

Notes:

1. The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.
2. LED voltage and current is defined for each LED branch (3 LED serial).

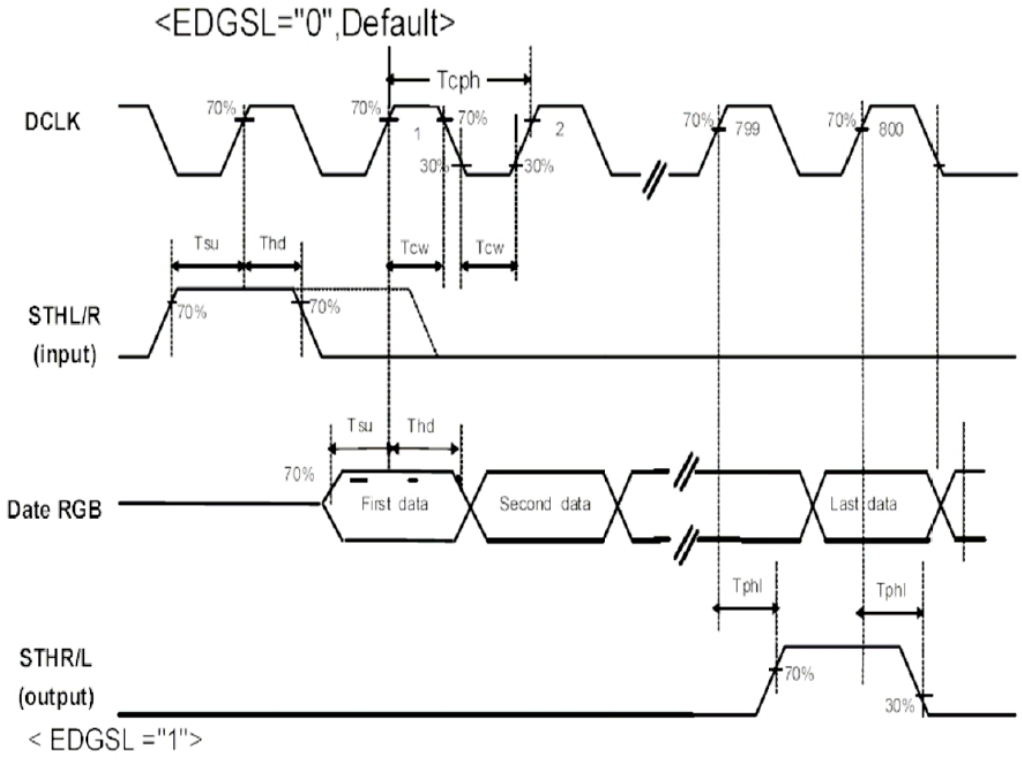
5.1 Timing characteristics

5.1.1 Timing conditions

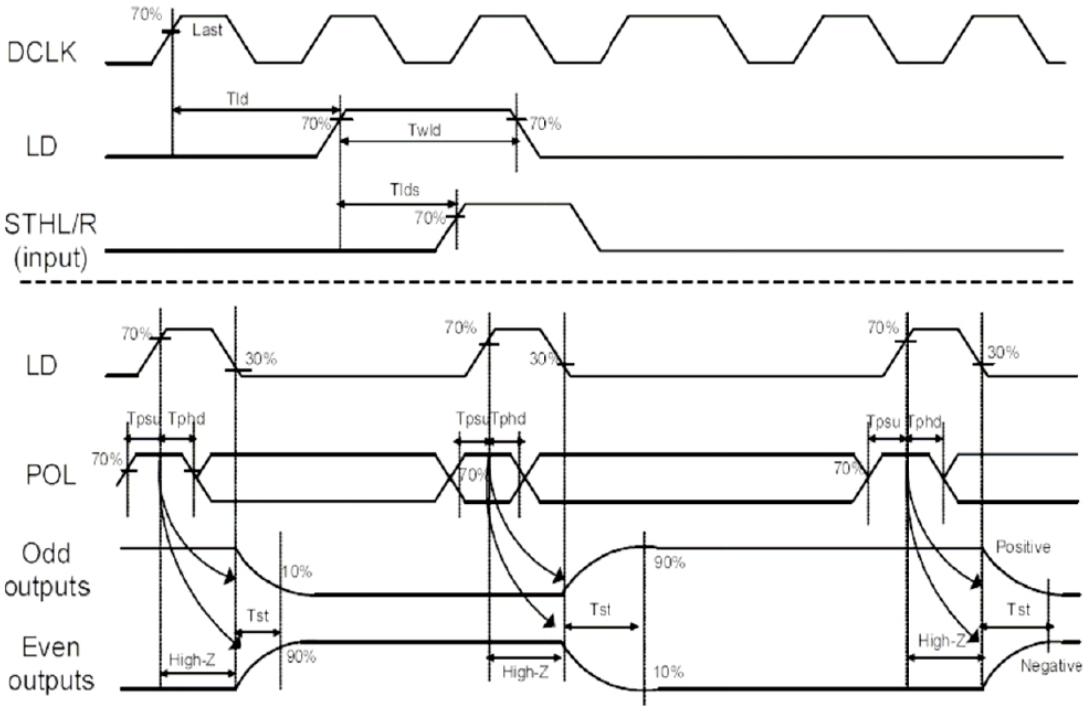
Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fdclk	-	40	45	MHz
DCLK cycle	Tcph	22	25	-	ns
DCLK pulse width	Tcw	8	-	-	ns
Data setup time	Tsu	4	-	-	ns
Data hold time	Thd	2	-	-	ns
Time that the last data to LD	Tld	1	-	-	Tcph
Pulse width of LD	Twld	2	-	-	Tcph
Time that LD to STHL/R	Tlds	5	-	-	Tcph
POL setup time	Tpsu	6	-	-	ns
POL hold time	Tphd	6	-	-	ns
CKV frequency	Fvclk	-	-	200	kHz
CKV rise time	Trck	-	-	100	ns
CKV falling time	Tfck	-	-	100	ns
CKV pulse width	Pwclk	500	-	-	ns
Horizontal display period	Tdh	-	800	-	Tcph
Horizontal period timing range	Th	-	1056	-	Tcph
STVU/D setup time	Tsuv	200	-	-	ns
STVU/D hold time	Thdv	300	-	-	ns
STVU/D delay time	Tdt	-	-	500	ns
Driver output delay time	Tdo	-	-	900	ns
Output rise time	Ttlh	-	500	1000	ns
Output falling time	Tthl	-	400	800	ns
OEV pulse width	Twcl	1	-	-	us
OEV to Driver output delay time	Toe	-	-	900	ns
Horizontal lines per field	Tv	512	525	610	Tdh
Vertical display timing range	Tvd	-	480	-	Tdh

5.1.2 Timing diagram

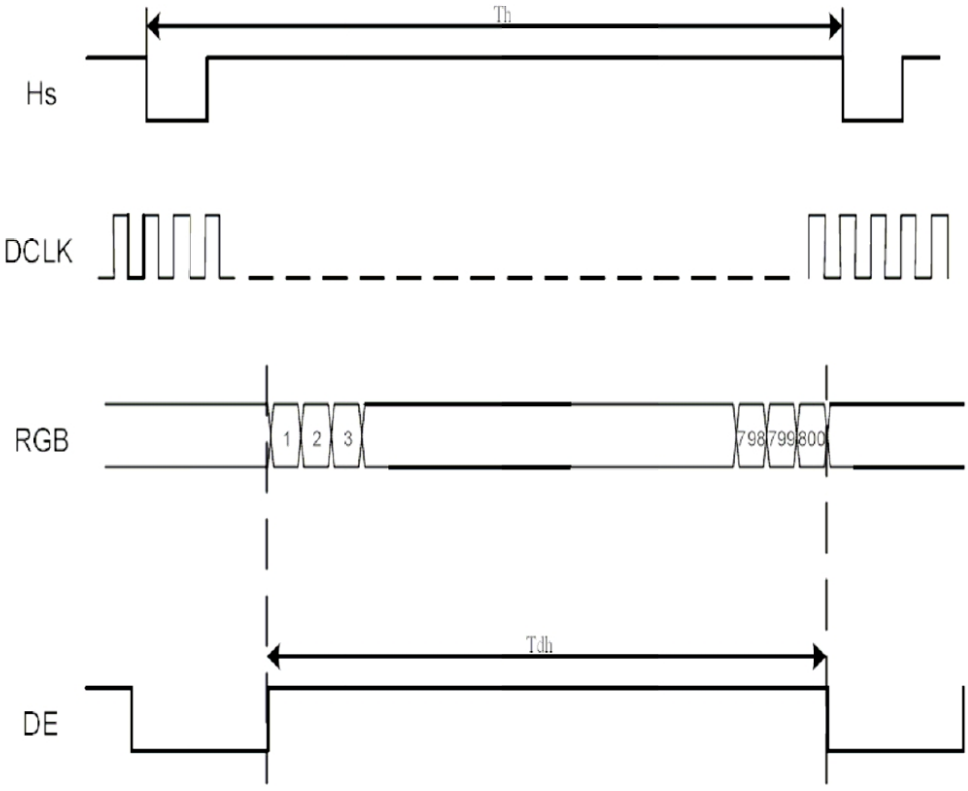
Timing Diagram1 (CHNSL="1" , Default)



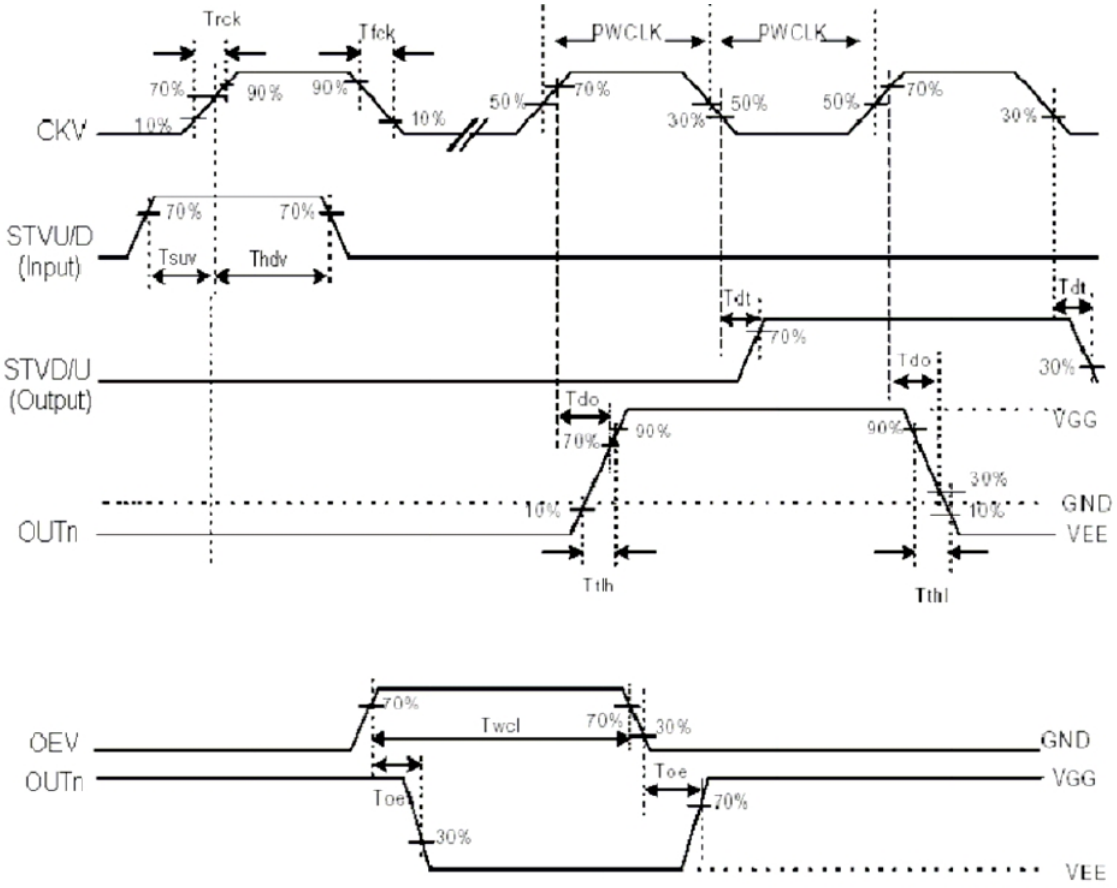
Timing Diagram 2



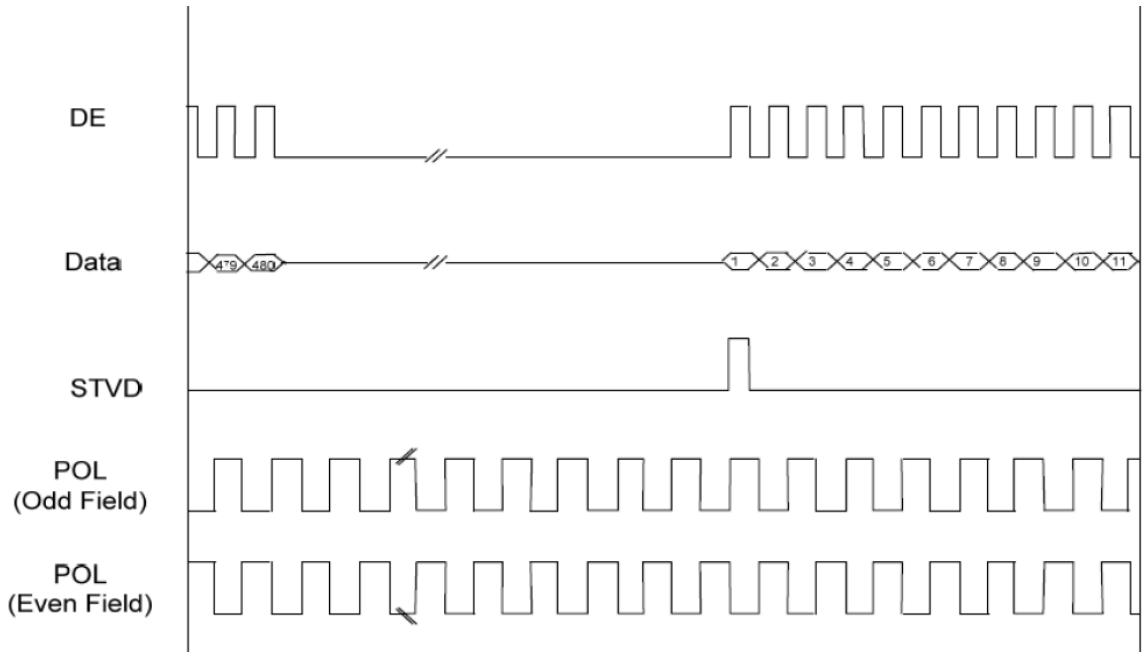
Horizontal Timing 1



Horizontal Timing 2

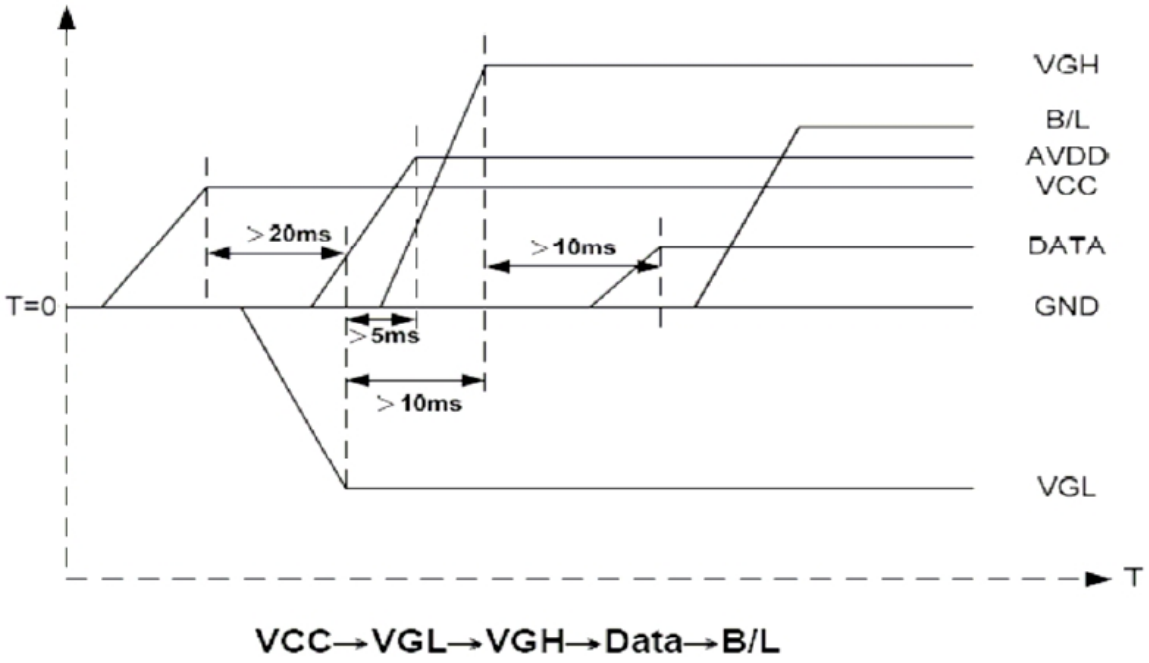


Vertical Shift Clock Timing



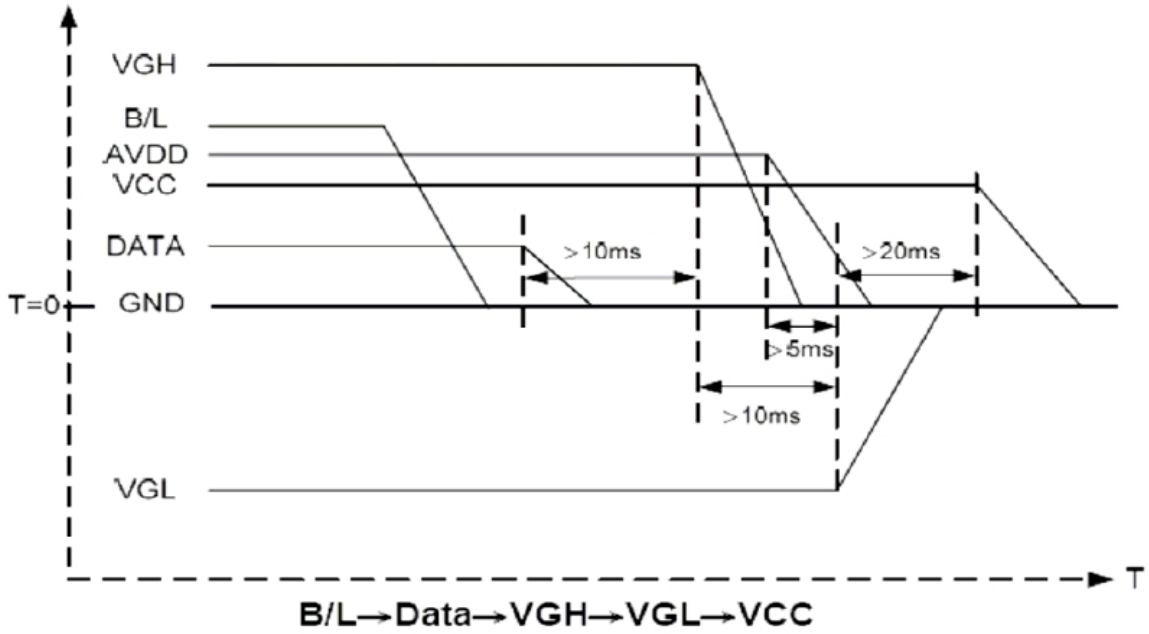
Vertical Timing

5.2 Power ON / OFF sequence



VCC→VGL→VGH→Data→B/L

Power On



B/L→Data→VGH→VGL→VCC

Power Off

6.0 Environmental requirements

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature (Ta)	-30°C	+85°C	-40°C	+95°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 1.5 mm Duration: 2 Hours in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note: Product cannot sustain at extreme storage conditions for long time.

7.0 LCD specification

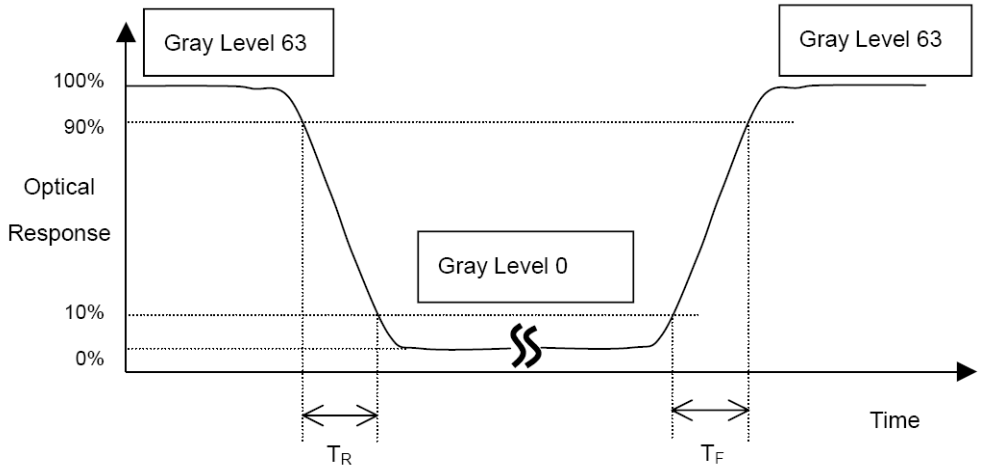
7.1 Electro-optical characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle (CR ≥ 10)	θ_L	ϕ=270°	60	70	-	Degree	Note 3
	θ_R	ϕ=90°	60	70	-		
	θ_T	ϕ=0°	40	50	-		
	θ_B	ϕ=180°	60	70	-		
Response time	T_{ON}	θ=ϕ=0°	-	10	20	ms	Note 2
	T_{OFF}		-	15	30	ms	
Contrast ratio	CR		400	500	-		Note 1
Color chromaticity	W_X		0.26	0.31	0.36		Note 4, 5
	W_Y		0.28	0.33	0.38		
Luminance	L		250	300	-	cd/m^2	Note 5
Luminance uniformity	Y_U		70	75	-	%	

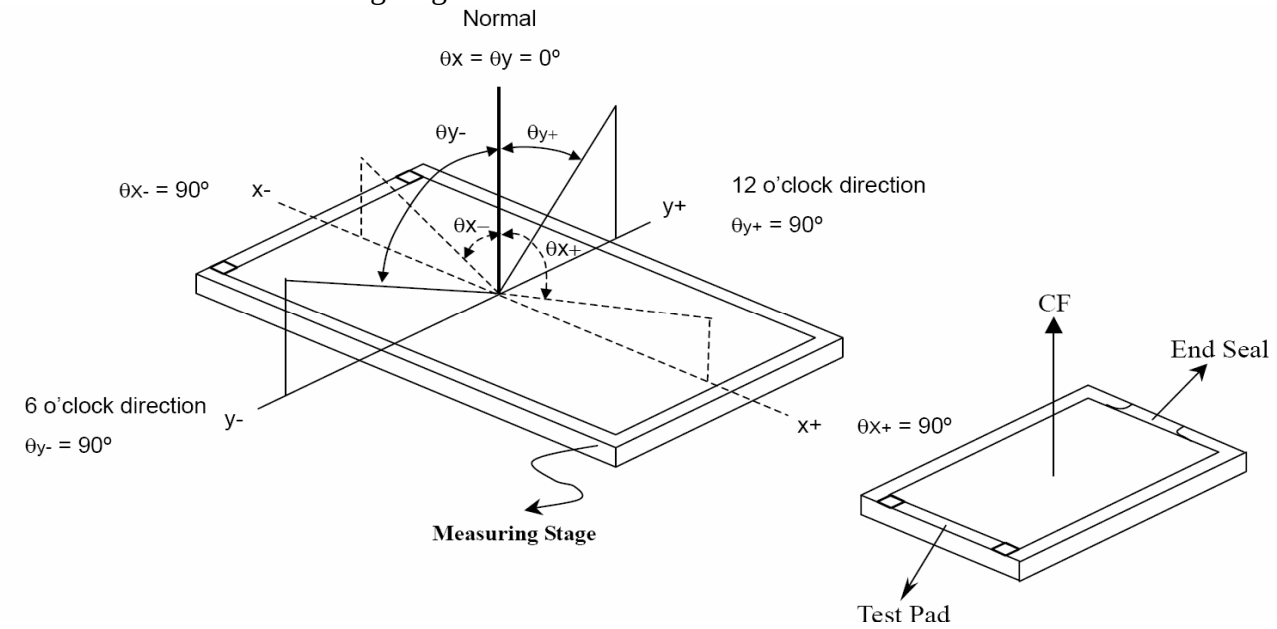
Note 1: Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.
Contrast Ratio (CR) = L63 / L0
L63: Luminance of gray level 63
L0: Luminance of gray level 0
CR = CR (10)
CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note 5.

Note 2: Definition of Response Time (TR, TF):

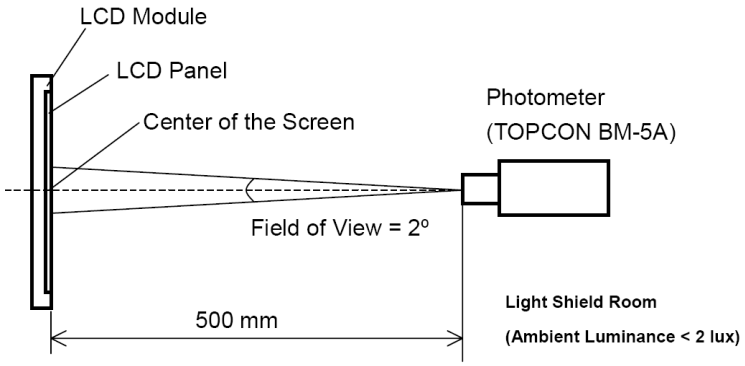


Note 3: Definition of Viewing Angle:

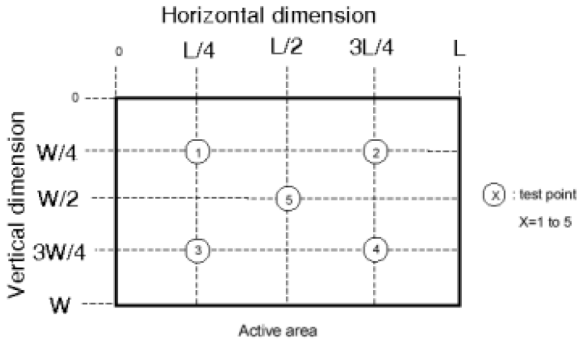


Note 4: Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note 5:



8.0 Interface

Pin No.	Symbol	I/O	Function	Remark
1	POL	I	Polarity selection	
2	STVD	I/O	Vertical start pulse input when U/D= H	Note 1
3	OEV	I	Output enable	
4	CKV	I	Vertical clock	
5	STVU	I/O	Vertical start pulse input when U/D= L	Note 1
6	GND	P	Power ground	
7	EDGSL	I	Select rising edge or falling edge	
8	V_{CC}	P	Power supply for digital circuit	
9	V9	I	Gamma voltage level 9	
10	V_{GL}	P	Gate OFF voltage	
11	V2	I	Gamma voltage level 2	
12	V_{GH}	P	Gate ON voltage	
13	V6	I	Gamma voltage level 6	
14	U/D	I	Up/down selection	Note 1,2
15	V_{COM}	I	Common voltage	
16	GND	P	Power ground	
17	AV_{DD}	P	Power supply for analog circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	
20	V8	I	Gamma voltage level 8	

21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power ground	
24	R5	I	Red data(MSB)	
25	R4	I	Red data	
26	R3	I	Red data	
27	R2	I	Red data	
28	R1	I	Red data	
29	R0	I	Red data(LSB)	
30	GND	P	Power ground	
31	GND	P	Power ground	
32	G5	I	Green data(MSB)	
33	G4	I	Green data	
34	G3	I	Green data	
35	G2	I	Green data	
36	G1	I	Green data	
37	G0	I	Green data(LSB)	
38	STHL	I/O	Horizontal start pulse input when R/L = H	Note 1
39	REV	I	Control signal are inverted or not	Note3
40	GND	I	Power ground	
41	DCLK	I	Sample clock	
42	V_{CC}	P	Power supply for digital circuit	
43	STHR	I/O	Horizontal start pulse input when R/L = L	Note 1
44	LD	I	Latches the polarity of outputs and switches the new data to outputs	
45	B5	I	Blue data (MSB)	

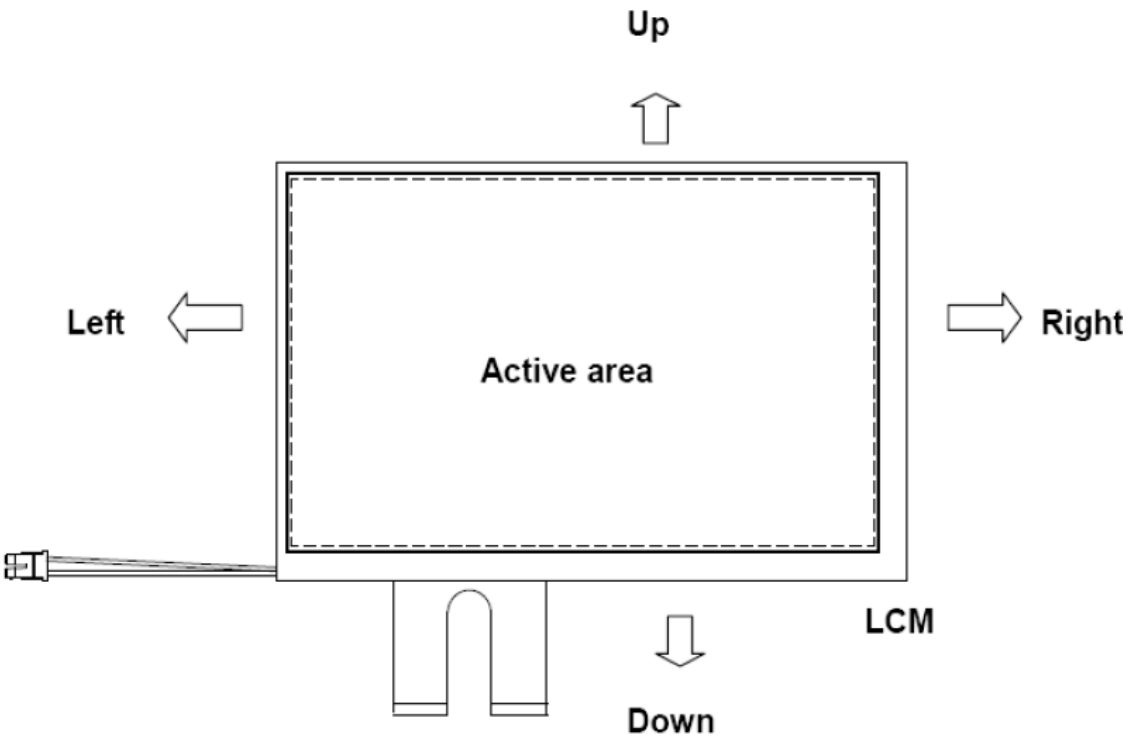
46	B4	I	Blue data	
47	B3	I	Blue data	
48	B2	I	Blue data	
49	B1	I	Blue data	
50	B0	I	Blue data (LSB)	
51	R/L	I	Right/ left selection	Note 1,2
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AV_{DD}	P	Power supply for analog circuit	
59	GND	P	Power ground	
60	V_{COM}	I	Common voltage	

I: input, O: output, P: Power

Note 1: Selection of scanning mode

Setting of scan control input		IN/OUT state for start pulse				Scanning direction
U/D	R/L	STVD	STVU	STHR	STHL	
GND	V_{CC}	O	I	O	I	Up to down, left to right
V_{CC}	GND	I	O	I	O	Down to up, right to left
GND	GND	O	I	I	O	Up to down, right to left
V_{CC}	V_{CC}	I	O	O	I	Down to up, left to right

Note 2: Definition of scanning direction.
Refer to the figure as below:

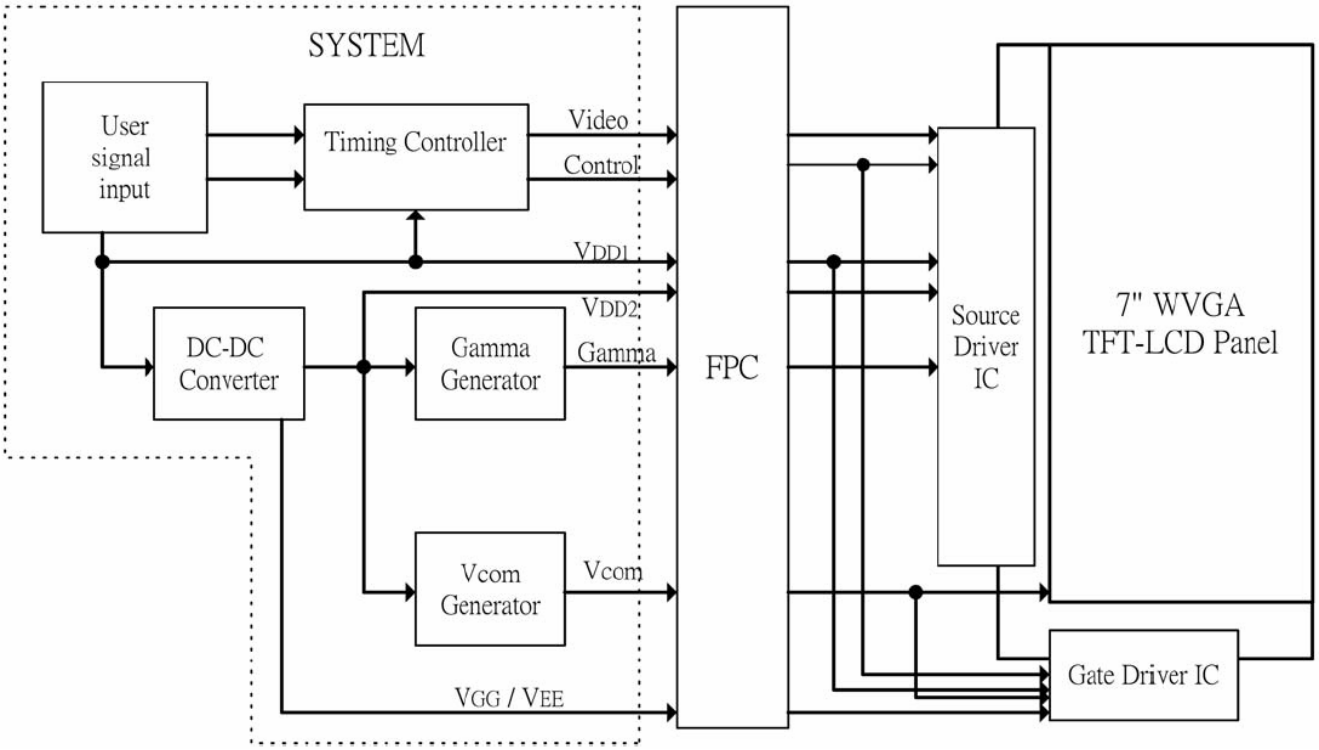


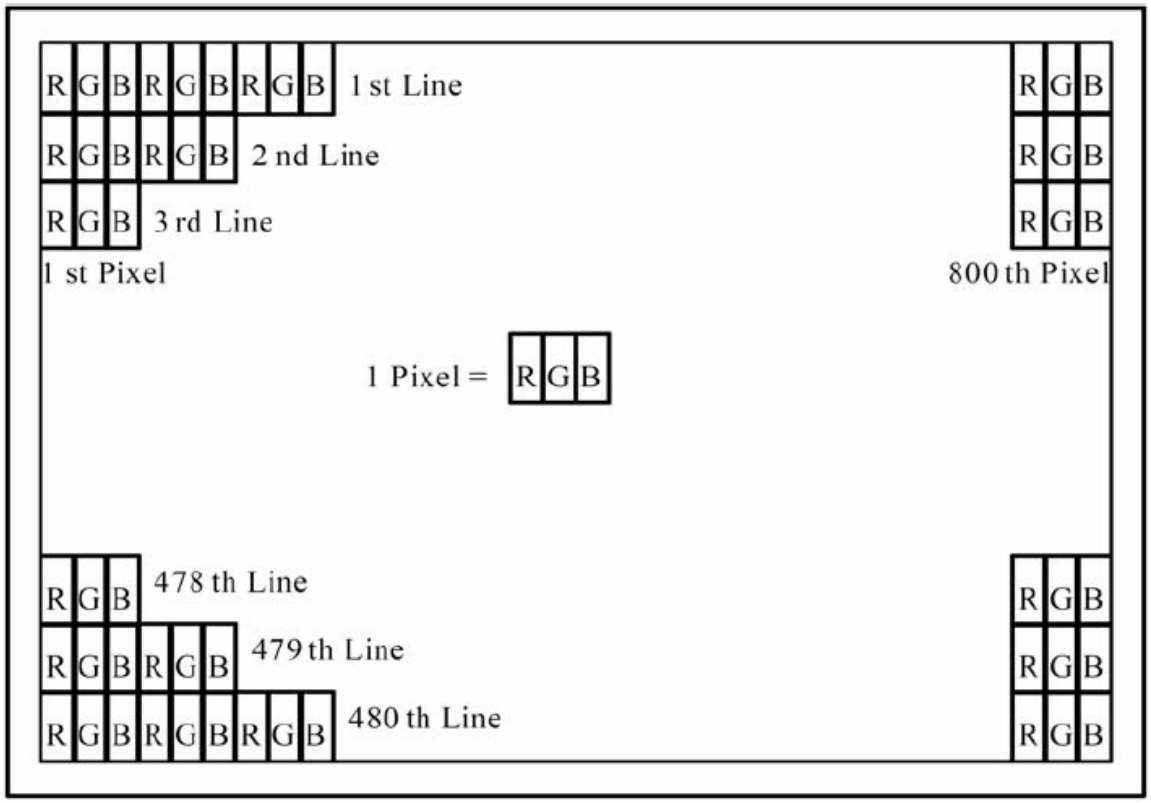
Note 3: When REV="L" , normally
REV="H", these data will be inverted.

Backlight connection

Pin No.	Symbol	I/O	Function	Remark
1	HI	P	Power supply for backlight unit(High voltage)	Pink
2	GND	P	Ground for backlight unit	White

9.0 Block diagram & pixel arrangement



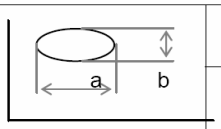


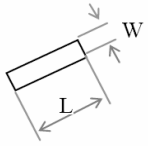
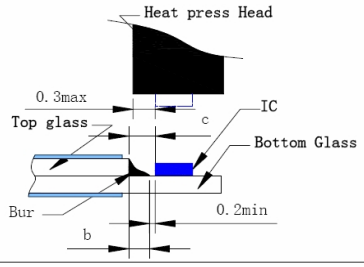
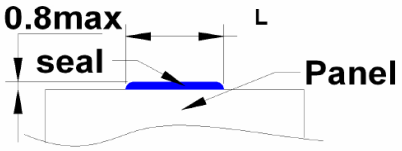
10.0 Display color and gray scale reference

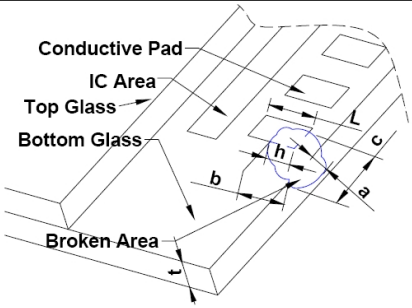
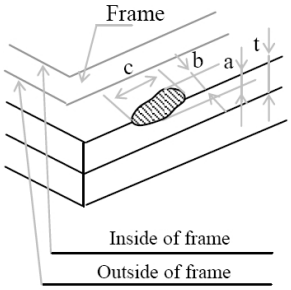
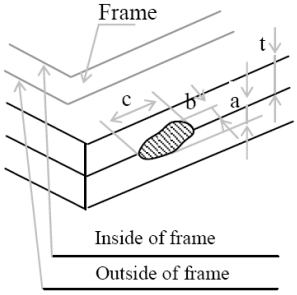
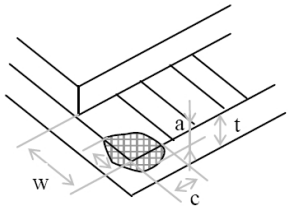
Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

11.0 TFT panel inspection specification

Note: Customer must 100% examine received TFT panels according to this inspection specifications.

<table>
<tr><td rowspan="6">1. Dot Defects (including particles and TFT dot defects)</td><td rowspan="6"> 

Φ=(a+b)/2</td><td colspan="2">Classifications</td><td colspan="2">Acceptable counts</td></tr>
<tr><td></td><td></td><td>Visible area</td><td>Non-visible area</td></tr>
<tr><td rowspan="3">A grade</td><td>Φ≦0.10</td><td>Don't care</td><td rowspan="4">Don't care</td></tr>
<tr><td>0.10<Φ≦0.20</td><td>1</td></tr>
<tr><td>0.20<Φ</td><td>0</td></tr>
<tr><td>B grade (for reference)</td><td>0.1<Φ≦0.15</td><td>5</td></tr>
<tr><td></td><td></td><td>0.15<Φ≦0.2</td><td>3</td></tr>
<tr><td rowspan="5">2. Line Defects</td><td rowspan="5"> 
</td><td colspan="2">Classifications</td><td colspan="2">Acceptable counts</td></tr>
<tr><td></td><td></td><td>Visible area</td><td>Non-visible area</td></tr>
<tr><td rowspan="3">A grade</td><td>W≦0.03,L≦3.0</td><td>Don't care</td><td rowspan="4">Don't care</td></tr>
<tr><td>0.03<W≦0.05,L≦2.0</td><td>1</td></tr>
<tr><td>0.05<W</td><td>According to dot defects.</td></tr>
<tr><td>B grade (for reference)</td><td>0.03<W≦0.05,L≦3.0</td><td>3</td></tr>
<tr><td rowspan="2">3.Glass bur</td><td> 
</td><td colspan="3">1). b ≦ 1.0, and not affect outline dimension and assemble
2). Around bonding area, b must fulfill b ≦ (c-0.2) max,
Any burs should not affect the assemble as a rule.</td></tr>
<tr><td>  </td><td colspan="3">Not affect outline dimension and assemble</td></tr>
<tr><td>4. End seal dimension</td><td> 
</td><td colspan="3">1).Depth =< 0.2 mm, and not enter to the visible area.
2). Height =< 0.8 mm.
3). L=The cell chip width+(2~6)mm.</td></tr>
<tr><td rowspan="3">5. Glass edges breakage</td><td rowspan="3"></td><td colspan="3">Categories</td></tr>
<tr><td>A</td><td colspan="2">If a ≦ t and b ≦3, c has no limit.</td></tr>
<tr><td>B</td><td colspan="2">a ≦ t, b≦3, c≦3</td></tr>
</table>

	 Breakage on step glass	C	If damage FPC contacts and /or alignment mark, then b ≦ 0.5, and the FPC contacts h ≦ L x 25% max
		D	Side breakage should not damage alignment mark.
	Edge breakage 	b should not arrive inside of frame	
	Breakage between upper and lower glass 	b should not arrive outside of frame	
	Corner breakage 	a ≦ t, b ≦ 3.0, c ≦ 3.0	
		Corner breakage should not damage track and /or alignment mark.	

Items	Position	Inspection Criteria
6.Crack	Whole area	Not allowed
7.Surface cleanness	Step surface	The impurity which is easy to clean is allowed, glass particle is not allowed.
Remark: a: breakage thickness; b: breakage depth; c: breakage length; t: glass thickness; h: damaged FPC contact length; L: total length of FPC contacts (Unit: mm)		

12.0 Mechanical drawing