54AC164245

Rad-hard 16-bit transceiver 3.3 V to 5 V bidirectional level shifter

Datasheet - production data

Ceramic Flat-48

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Features

- Fully compatible with 54ACS164245
- Dual supply bidirectional level shifter
- Extended voltage range from 2.3 V to 5.5 V
- Separated enable pin for 3-state output
- Schmidt-triggered I/Os: 100 mV hysteresis
- Internal 26 Ω limiting resistor on each I/O
- High speed: Tpd = 8 ns maximum
- Fail safe
- Cold spare
- Hermetic package
- 100 krad (Si) at any Mil1019 dose rate
- SEL immune to 110MeV.cm^2/mg LET ions
- RHA QML-V qualified

Description

The 54AC164245 is a rad-hard advanced high-speed CMOS, Schmitt trigger 16-bit bidirectional multi-purpose transceiver with 3-state outputs and cold sparing.

Designed for use as an interface between a 5 V bus and a 3.3 V bus in mixed 5 V/3.3 V supply systems, it achieves high-speed operation while maintaining the CMOS low-power dissipation.

All pins have cold spare buffers to change them to high impedance when V_{DD} is tied to ground.

This IC is intended for two-way asynchronous communication between the data buses. The direction of the data transmission is determined by the nDIR inputs.

The A port interfaces with the 3.3 V bus but can also operate at 2.3 V. The B port operates with the 5 V bus.

Table 1. Device summary

Order codes	SMD pin	Quality level	Package	Lead finish	Mass	EPPL	Temp. range
RHFAC164245K1	-	Engineering model	Flat-48	Gold	1.50 g	-	-55 °C to 125 °C
RHRAC164245K01V	5962R9858008VYC	QML-V flight				Yes	

Contents

1 Functional description

Figure 1. Logic diagram

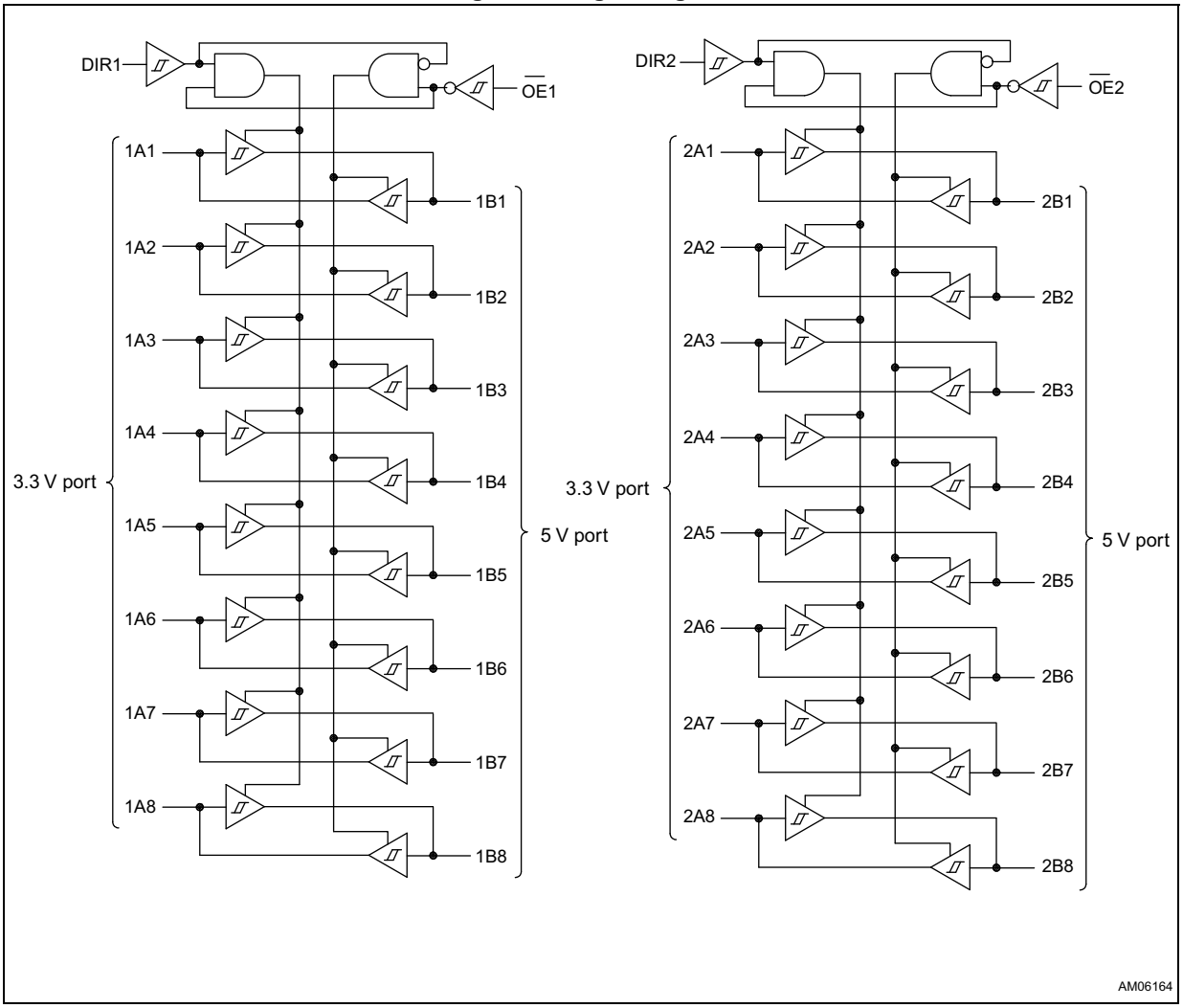


Table 2. Function table

Enable, $\overline{OEx}$	Direction, DIRx	Operation
L	L	B data to A bus
	H	A data to B bus
H	X	Isolation

1.1 Cold spare

The 54AC164245 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{DD} = V_{SS}, V_{DD} - V_{SS} = 0 V) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept unpowered so that they can be switched on only when required. Power consumption is therefore reduced by switching off the redundant circuit. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between I/Os and V_{DD}. The ESD protection is ensured through a non-conventional dedicated structure.

1.2 Power-up

During power-up, all outputs are forced to high impedance. The high-impedance state is maintained approximately until V_{DD} is high, thus avoiding any transient and erroneous signals during power-up.

1.3 Pin connections

Figure 2. Pin connections

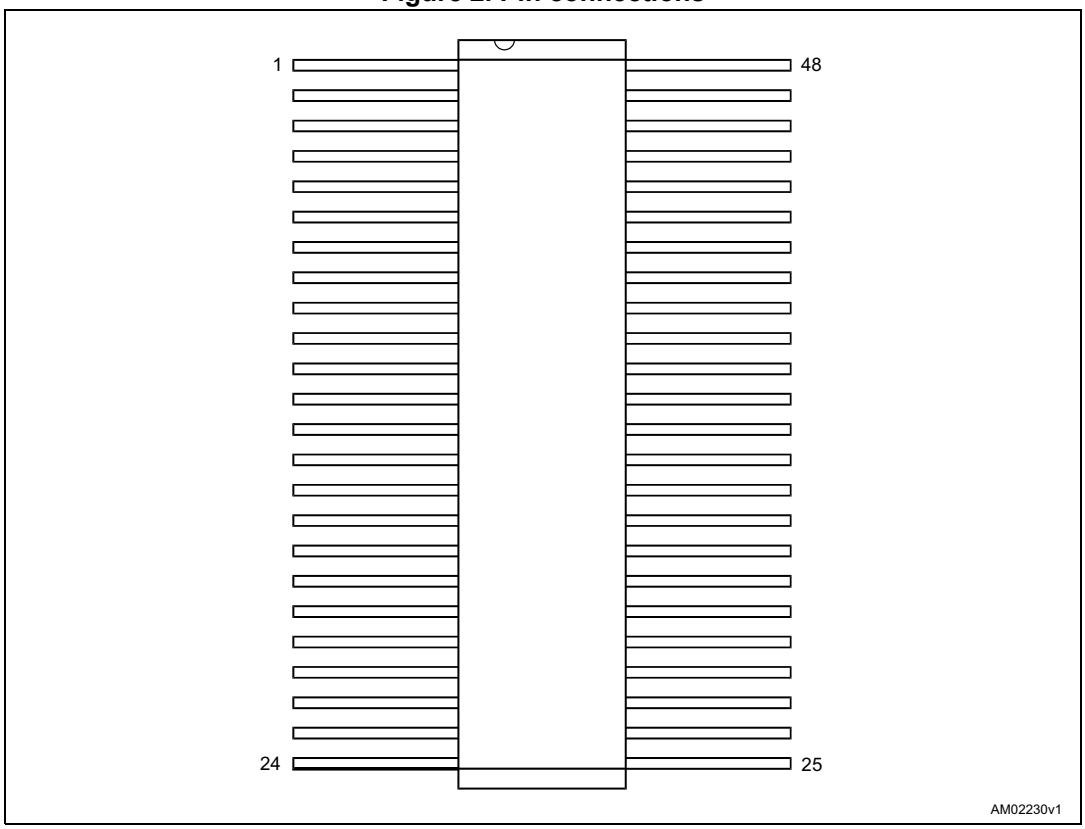


Table 3. Pin descriptions

Pin number	Symbol	Name and function
1	DIR1	Direction control inputs
2, 3, 5, 6, 8, 9, 11, 12	1B1 to 1B8	Side B inputs or 3-state outputs (5 V port)
4,10, 15, 21, 28, 34, 39, 45	V_{SS}	Reference voltage to ground
7, 18	V_{DD1}	Supply voltage (5 V)
13, 14, 16, 17, 19, 20, 22, 23	2B1 to 2B8	Side B inputs or 3-state outputs (5 V port)
24	DIR2	Direction control inputs
25	nG2	Output enable inputs (active low)
31, 42	V_{DD2}	Supply voltage (3.3 V)
47, 46, 44, 43, 41, 40, 38, 37	1A1 to 1A8	Side A inputs or 3-state outputs (3.3 V port)
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Side A inputs or 3-state outputs (3.3 V port)
48	nG1	Output enable inputs (active low)

2 Absolute maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Unless otherwise noted, all voltages are referenced to V_{SS}.

The limits for the parameters specified in *Table 4* apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD1}	5 V supply voltage(1)	-0.3 to +6.0	V
V_{DD2}	3 V supply voltage		
V_{IA}	DC input voltage range port A	-0.3 to V_{DD1}+0.3 V	
V_{IB}	DC input voltage range port B		
V_{OA}	DC output voltage range port A		
V_{OB}	DC output voltage range port B		
I_{IA}	DC input currents port A, anyone input	± 10	mA
I_{IB}	DC input currents port B, anyone input		
T_{stg}	Storage temperature range	-65 to +150	°C
T_L	Lead temperature (10 s)	300	
T_J	Junction temperature range	175	
R_{thja}	Thermal resistance junction to ambient(2) Flat package, 48 pins	TBD	°C/W
R_{thjc}	Thermal resistance junction to case(2) Flat package, 48 pins		
ESD	HBM: human body model(3)	2	kV

1. V_{DD1} (5 V) may remain disconnected.
2. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
3. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

In *Table 5*, unless otherwise noted, all voltages are referenced to V_{SS}.

Table 5. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD1}	Supply voltage	4.5 to 5.5 or 2.3 to 3.6	V
V_{DD2}		2.3 to 3.6 or 4.5 to 5.5	
V_I	Input voltage	0 to V_{DD1}	
V_O	Output voltage		
T_{op}	Operating temperature	-55 to +125	°C
d_t / d_v	Input rise and fall time V_{CC} = 3.0, 4.5 or 5.5(1)	0 to 8	ns / V

1. Derates system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.

3 Electrical characteristics

In *Table 6*, T_{op} = -55 °C to 125°C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 2.7 V to 3.6 V, unless otherwise specified. Each input/output, as applicable, is tested at the specified temperature, for the specified limits, to the tests specified in TABLE IA from the SMD 5962-98580 DLA Agency Spec. Non-designated output terminals are high level logic, low level logic or open, except for all I_{DD} tests, where the output terminals are open. When performing these tests, the current meter must be placed in the circuit such that all current flows through the meter.

Table 6. DC specifications

Symbol	Parameter	Port voltage	Test condition (V_{DD}) (1)	Limits		Unit
				Min.	Max.	
V_{T+}	Schmitt trigger positive going threshold port A	3.3 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 2.7 and 3.6 V		0.7 V_{DD2}	V
		5.0 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 4.5 and 5.5 V			
	Schmitt trigger positive going threshold port B	3.3 V	V_{DD2} = 2.7 and 3.6 V V_{DD1} = 2.7 and 3.6 V		0.7 V_{DD1}	
		5.0 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 2.7 and 3.6 V			
V_{T-}	Schmitt trigger positive going threshold port A	3.3 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 2.7 and 3.6 V		0.3 V_{DD2}	
		5.0 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 4.5 and 5.5 V			
	Schmitt trigger positive going threshold port B	3.3 V	V_{DD1} = 2.7 and 3.6 V V_{DD2} = 2.7 and 3.6 V		0.3 V_{DD1}	
		5.0 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 2.7 and 3.6 V			
V_H	Schmitt trigger range of hysteresis port A	3.3 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 2.7 and 3.6 V	0.4		
		5.0 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 4.5 and 5.5 V	0.6		
	Schmitt trigger range of hysteresis port B	3.3 V	V_{DD1} = 2.7 and 3.6 V V_{DD2} = 2.7 and 3.6 V	0.4		
		5.0 V	V_{DD1} = 4.5 and 5.5 V V_{DD2} = 2.7 and 3.6 V	0.6		

Table 6. DC specifications (continued)

Symbol	Parameter	Port voltage	Test condition (V_{DD}) [1]	Limits		Unit
				Min.	Max.	
I_{IH}	Input current high port A (for input under test $V_I = V_{DD2}$ other inputs, $V_I = V_{DD2}$ or V_{SS})	3.3 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V		3	µA
		5.0 V	V_{DD1} = 5.5 V V_{DD2} = 5.5 V			
	Input current high port B (for input under test $V_I = V_{DD1}$ other inputs, $V_I = V_{DD1}$ or V_{SS})	3.3 V	V_{DD1} = 3.6 V V_{DD2} = 3.6 V			
		5.0 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V			
I_{IL}	Input current low port A (for input under test $V_I = V_{SS}$ other inputs, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V	-1		
		5 V	V_{DD1} = 5.5 V V_{DD2} = 5.5 V			
	Input current low port B (for input under test $V_I = V_{SS}$ other inputs, $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 3.6 V V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V			
I_{CS}	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 5.5 V, $\overline{OEn}$ = 5.5 V		V_{DD1} = 0 V	-1	5	
	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 0V, $\overline{OEn}$ = 5.5 V		V_{DD1} = 0 V			
	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 5.5 V, $\overline{OEn}$ = 0 V		V_{DD1} = 0 V			
	Input current cold spare mode port A = port B = 5.5 V = V_I DIRn = 0 V, $\overline{OEn}$ = 0 V		V_{DD1} = 0 V			
V_{OL1}	Low level output voltage port A, I_{OL} = 8 mA for all inputs affecting output under test, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V		0.5	V
		5 V	V_{DD1} = 4.5 V V_{DD2} = 4.5 V		0.4	
	Low level output voltage port B, I_{OL} = 8 mA for all inputs affecting output under test, $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 V V_{DD2} = 2.7 V		0.5	
		5 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V		0.4	

Table 6. DC specifications (continued)

Symbol	Parameter	Port voltage	Test condition (V_{DD}) (1)	Limits		Unit
				Min.	Max.	
V_{OL2}	Low level output voltage	3.3 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V		0.2	V
	Port A, I_{OL} = 100 µA for all inputs affecting output under test, $V_I = V_{DD2}$ or V_{SS}	5 V	V_{DD1} = 4.5 V V_{DD2} = 4.5 V			
	Low level output voltage	3.3 V	V_{DD1} = 2.7 V V_{DD2} = 2.7 V			
	Port B, I_{OL} = 100 µA For all inputs affecting output under test, $V_I = V_{DD1}$ or V_{SS}	5 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V			
V_{OH1}	High level output voltage port A, I_{OH} = -8 mA for all inputs affecting output under test, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V	V_{DD2}-0.9		
		5 V	V_{DD1} = 4.5 V V_{DD2} = 4.5 V	V_{DD2}-0.7		
	High level output voltage port B, I_{OH} = -8 mA for all inputs affecting output under test, $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 V V_{DD2} = 2.7 V	V_{DD1}-0.9		
		5 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V	V_{DD1}-0.7		
V_{OH2}	High level output voltage port A, I_{OH} = - 100 µA for all inputs affecting output under test, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V	V_{DD2}-0.2		
		5 V	V_{DD1} = 4.5 V V_{DD2} = 4.5 V			
	High level output voltage port B, I_{OH} = - 100 µA for all inputs affecting output under test, $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 V V_{DD2} = 2.7 V	V_{DD1}-0.2		
		5 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V			
I_{OL} (2)	Output current (sink) port A, $V_I = V_{SS}$	3.3 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V V_{OL} = 0.5 V	8.0		mA
		5 V	V_{DD1} = 4.5 V V_{DD2} = 4.5 V V_{OL} = 0.4 V			
	Output current (sink) port B, $V_I = V_{SS}$	3.3 V	V_{DD1} = 2.7 V V_{DD2} = 2.7 V V_{OL} = 0.5 V			
		5 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V V_{OL} = 0.4 V			

Table 6. DC specifications (continued)

Symbol	Parameter	Port voltage	Test condition (V_{DD}) (1)	Limits		Unit
				Min.	Max.	
I_{OH} (4)	Output current (source) port A, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V $V_{OH} = V_{DD2}$ -0.9 V	-8.0		mA
		5 V	V_{DD1} = 4.5 V V_{DD2} = 4.5 V $V_{OH} = V_{DD2}$ -0.7 V			
	Output current (source) port B, $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 V V_{DD2} = 2.7 V $V_{OH} = V_{DD2}$ -0.9 V			
		5 V	V_{DD1} = 4.5 V V_{DD2} = 2.7 V $V_{OH} = V_{DD2}$ -0.7 V			
I_{OZH}	Three-state output leakage current high port A, for input under test, $V_I = V_{DD2}$ other inputs, $V_O = V_{DD2}$ $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V		3.0	µA
			V_{DD1} = 5.5 V V_{DD2} = 5.5 V			
	Three-state output leakage current high port B, for input under test, $V_I = V_{DD1}$ other inputs, $V_O = V_{DD1}$ $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 3.6 V V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V			
I_{OZL}	Three-state output leakage current low port A, for input under test, $V_I = V_{SS}$ other inputs, $V_O = V_{SS}$ $V_I = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V	-1.0		
		5 V	V_{DD1} = 5.5 V V_{DD2} = 5.5 V			
	Three-state output leakage current low port B, for input under test, $V_I = V_{SS}$ other inputs, $V_O = V_{SS}$ $V_I = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 3.6 V V_{DD2} = 3.6 V			
		5 V	V_{DD1} = 5.5 V V_{DD2} = 3.6 V			
I_{OS} (3) (3)	Short circuit output current port A, $V_O = V_{DD2}$ or V_{SS}	3.3 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V	-100	100	mA
		5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V	-200	200	
	Short circuit output current port B, $V_O = V_{DD1}$ or V_{SS}	3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.6 V	-100	100	
		5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V	-200	200	

Table 6. DC specifications (continued)

Symbol	Parameter	Port voltage	Test condition (V_{DD}) (1)	Limits		Unit
				Min.	Max.	
P_D (3) (4) (5)	Power dissipation, port A, C_L = 50 pF per switching output	3.3 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V		1.5	mW/ MHz
		5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		2.0	
	Power dissipation, port B, C_L = 50 pF per switching output	3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.6 V		1.5	
		5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V		2.0	
I_{DDQ}	Quiescent supply current port A, V_I = V_{DD2} or V_{SS}	5 V	V_{DD1} = 5.5 V V_{DD2} = 5.5 V at 25°C		10	µA
			V_{DD1} = 5.5 V V_{DD2} = 5.5 V at -55 to 125 °C		100	
	Quiescent supply current port B, V_I = V_{DD1} or V_{SS}	5 V	V_{DD1} = 5.5 V V_{DD2} = 5.5 V at 25 °C		10	
			V_{DD1} = 5.5 V V_{DD2} = 5.5 V at -55 to 125 °C		100	
C_I	Input capacitance		f = 1 MHz V_{DD1} = V_{DD2} = 0 V		15	pF
C_O	Output capacitance		f = 1 MHz V_{DD1} = V_{DD2} = 0 V			
(6)	Functional test V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V	L	H	

1. This device requires both VDD1 and VDD2 power supplies for operation. The power supply is indicated and followed by the voltage to which the power supply is set to the given test.
2. This parameter is supplied as a design limit but not guaranteed or tested.
3. No more than one output should be shorted at a time for a maximum duration of one second.
4. Power does not include power contribution of any CMOS output sink current.
5. Power dissipation specified per switching output.
6. Tests must be performed in sequence and include attribute data only. Functional tests should include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table must, at minimum, test all the functions of each input and output. All possible input to output logic patterns per function should be guaranteed, if not tested, to the function table, *Table 2*. Functional tests are performed in sequence as approved by the qualifying activity on qualified devices. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: VIH = V_{IH}(min + 20%, -0%); V_{IL} = V_{IL}(max + 0%, -50%), as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.

In *Table 7*, data are guaranteed by design but not tested.

Table 7. AC electrical characteristics

Symbol	Parameter	Port voltage	Test condition (V_{DD})	Limits		Unit
				Min.	Max.	
t_{PLH}	Propagation delay time, data to bus (active low) C_L = 50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} =2.7 to 3.6 V	1.0	20	ns
	Propagation delay time, data to bus (active low) C_L = 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1}=4.5 to 5.5 V V_{DD2}=4.5 to 5.5 V		15	
t_{PHL}	Propagation delay time, data to bus (active high) C_L = 50 pF	Port A = 3.3V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V		20	
	Propagation delay time, data to bus (active high) C_L = 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		15	
t_{PZL}	Propagation delay time, output enable, $\overline{OEn}$ to bus (active low), C_L = 50 pF	Port A = 3.3 V Port B = 5V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V		18	
	Propagation delay time, output enable, $\overline{OEn}$ to bus (active low), C_L = 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V V_{DD2} = 2.7 to 3.6 V		18	
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		12	
t_{PZH}	Propagation delay time, output enable, $\overline{OEn}$ to bus (active high), C_L = 50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V		18	
	Propagation delay time, output enable, $\overline{OEn}$ to bus (active high), C_L = 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5V V_{DD2} = 4.5 to 5.5V		12	
t_{PLZ}	Propagation delay time, output disable, $\overline{OEn}$ to bus (low impedance), C_L = 50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.6 V		20	
	Propagation delay time, output disable, $\overline{OEn}$ to bus (low impedance), C_L= 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.6 V V_{DD2} = 2.7 to 3.6 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		15	
t_{PHZ}	Propagation delay time, output disable, $\overline{OEn}$ to bus (high impedance), C_L = 50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.3 V		18	
	Propagation delay time, output disable, $\overline{OEn}$ to bus (high impedance), C_L= 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		12	

Table 7. AC electrical characteristics (continued)

Symbol	Parameter	Port voltage	Test condition (V_{DD})	Limits		Unit
				Min.	Max.	
t_{PZL} (1)	Propagation delay time, output enable, DIRn to bus (active low), C_L = 50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.3 V	1.0	18	ns
	Propagation delay time, output enable, DIRn to bus (active low), C_L= 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		12	
t_{PZH} (1)	Propagation delay time, output enable, DIRn to bus (active high), C_L = 50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.3 V		18	
	Propagation delay time, output enable, DIRn to bus (active high), C_L= 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		12	
t_{PLZ} (1)	Propagation delay time, output disable, DIRn to bus (low impedance), C_L =50 pF	Port A = 3.3 V Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.3 V		20	
	Propagation delay time, output disable, DIRn to bus (low impedance), C_L= 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		15	
t_{PHZ} (1)	Propagation delay time, output disable, DIRn to bus (high impedance), C_L = 50 pF	Port A = 3.3 V Port B = 5.0 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 2.7 to 3.3 V		20	
	Propagation delay time, output disable, DIRn to bus (high impedance), C_L= 50 pF	Port A = Port B = 3.3 V	V_{DD1} = 2.7 to 3.3 V V_{DD2} = 2.7 to 3.3 V			
		Port A = Port B = 5 V	V_{DD1} = 4.5 to 5.5 V V_{DD2} = 4.5 to 5.5 V		15	

4 Radiations

Total dose (Mil1019 dose rate): all parameters are post-irradiation guaranteed by wafer-lot acceptance (after dose, all guaranteed electrical parameters are tested on a sample of units of each wafer lot).

All parameters provided in *Table 6* and *Table 7* apply to both pre- and post-irradiation. The 54AC164245 is a pure CMOS product. Irradiation is performed at high dose rates.

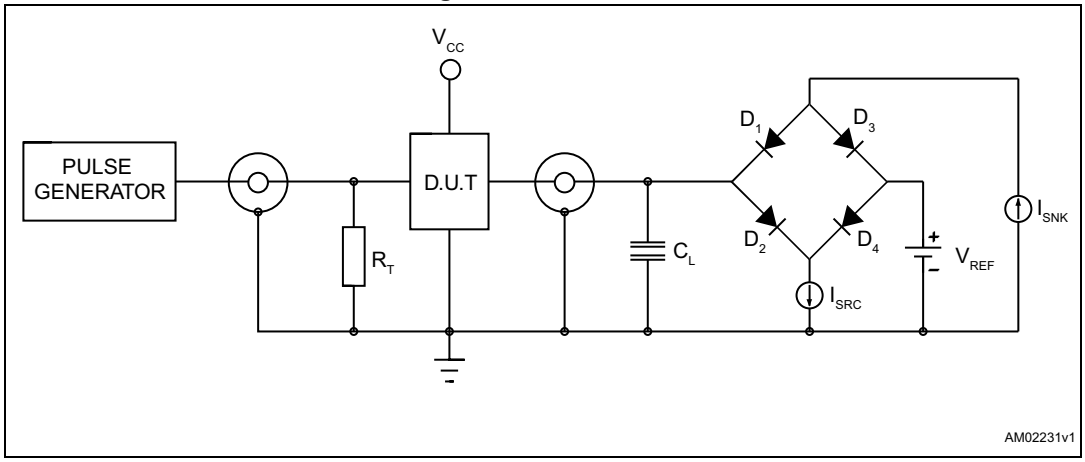
Heavy ions: the behavior of the product when submitted to heavy ions is guaranteed by qualification and is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 8. Radiations

Type	Features	Value	Unit
TID	Total Ionizing dose High dose rate (50 - 300 rad/sec) up to:	100	k rad
Heavy ions	SEL immune (at 125 °C) up to:	110	MeV.cm²/mg
	SEU immune up to:	64	

5 Test circuit

Figure 3. Test circuit



1. C_L = 50 pF or equivalent (includes jig and probe capacitance), $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω), V_{REF} = 0.5 V_{DD}. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements. Input signal from pulse generator: V_I = 0.0 V to V_{DD}; f = 10 MHz; t_r = 1.0 V/ns "0.3 V/ns; t_f = 1.0 V/ns "0.3 V/ns; tr and tf are measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD} respectively.

Figure 4. Waveform 1: propagation delay

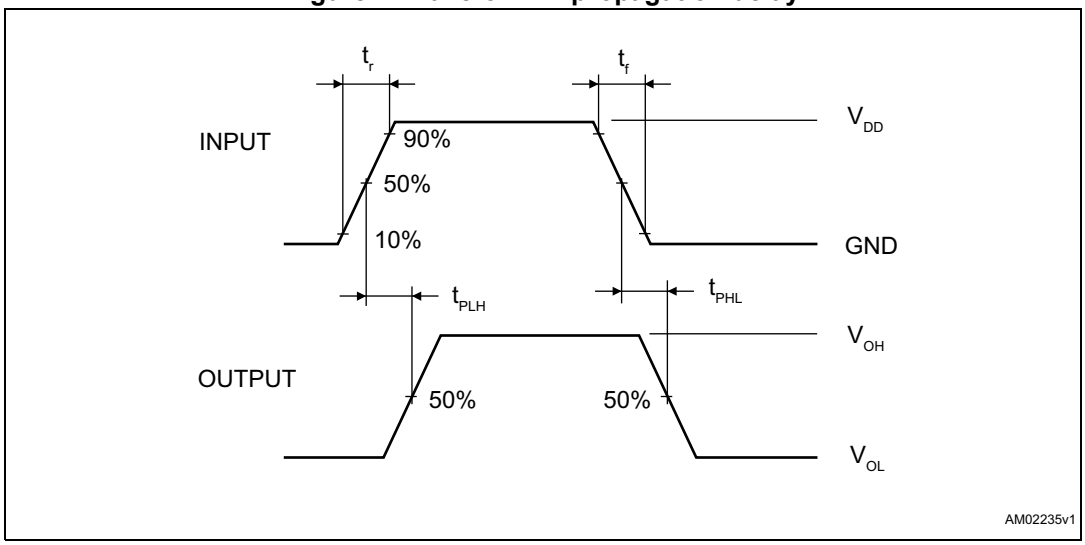


Figure 5. Waveform 2: enable and disable times (port A = port B, 5 V operation)

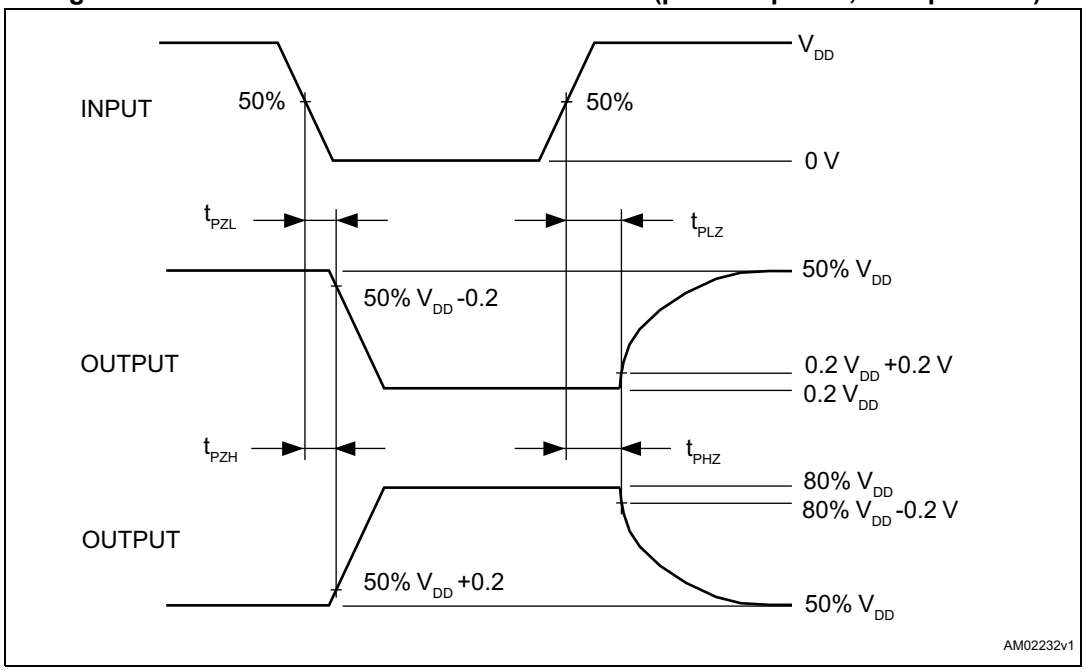


Figure 6. Waveform 3: enable and disable times (port A = port B, 3.3 V operation)

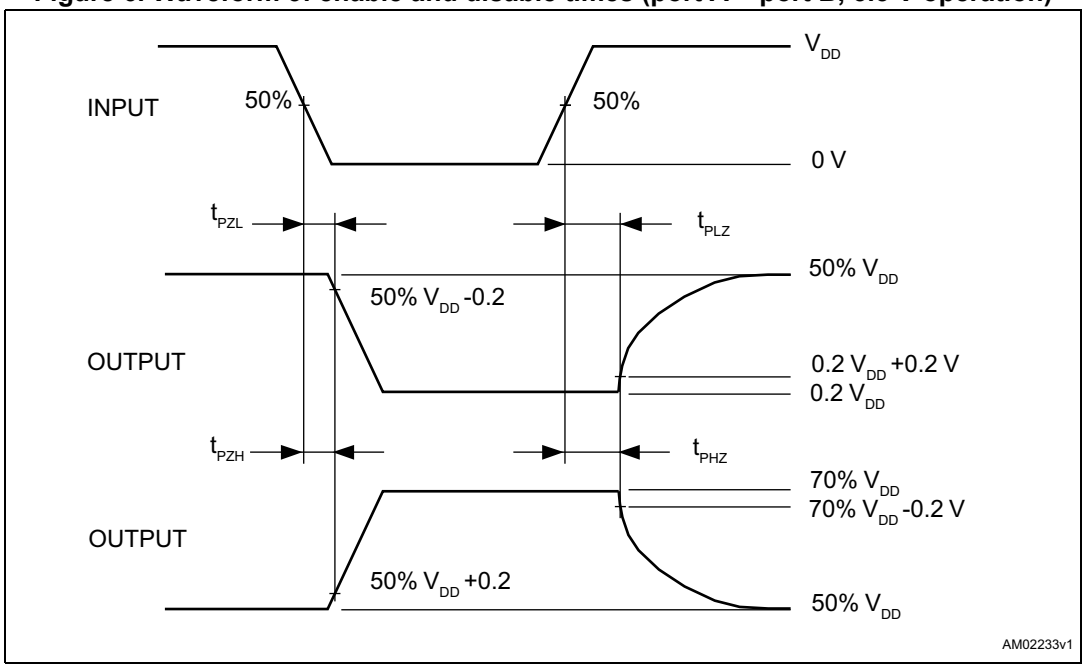
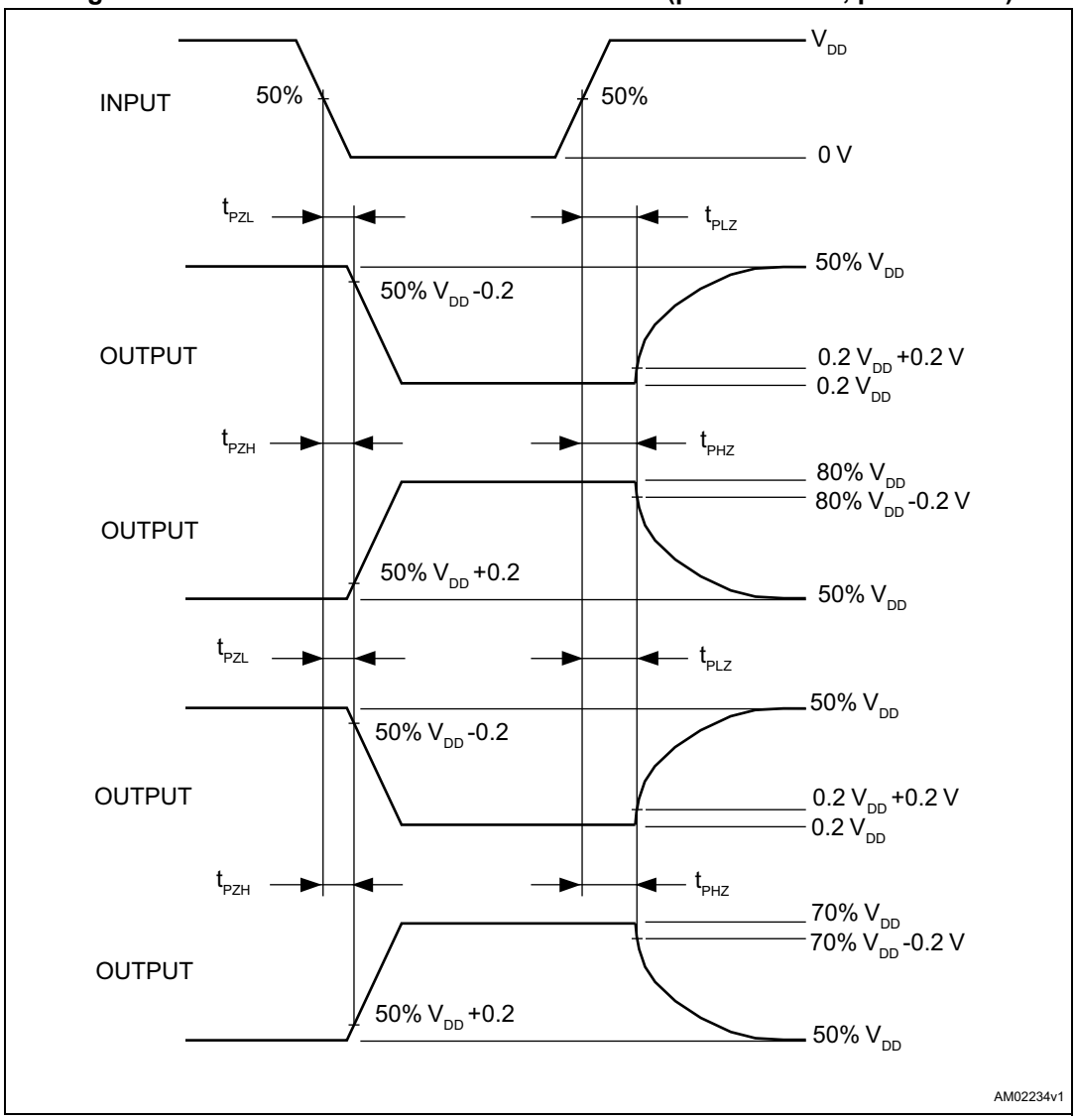


Figure 7. Waveform 4: enable and disable times (port A = 3.3 V, port B = 5 V)

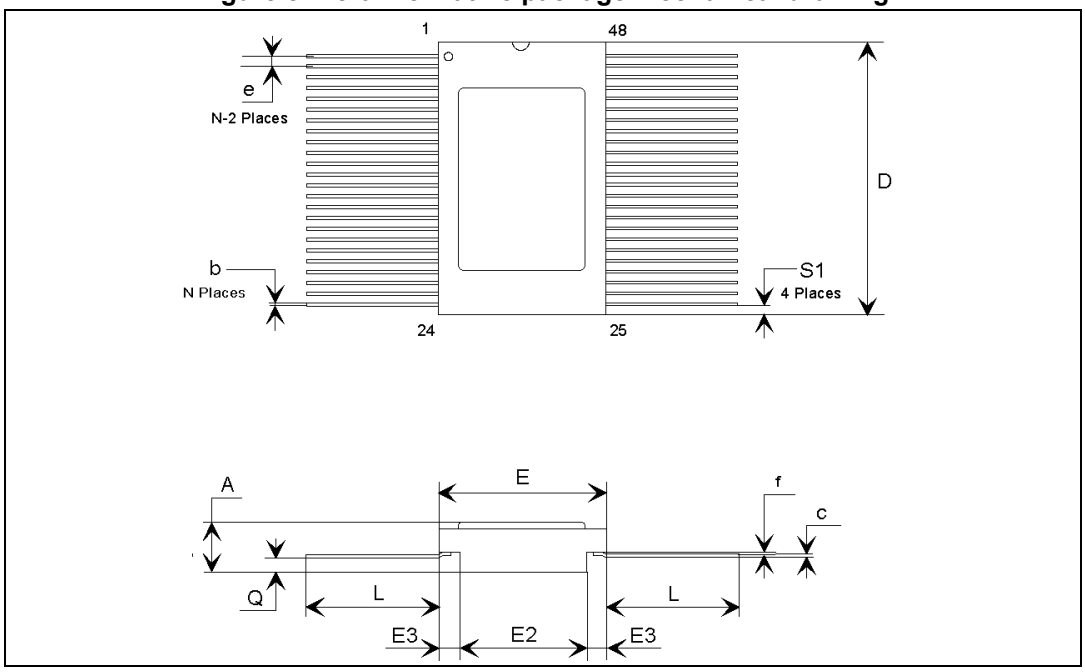


6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark.

6.1 Ceramic Flat-48 package information

Figure 8. Ceramic Flat-48 package mechanical drawing



1. The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting any unused pins or the metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 9. Ceramic Flat-48 package mechanical data

Dim	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	2.47	2.18	2.72	0.097	0.086	0.107
b	0.254	0.20	0.30	0.010	0.008	0.012
c	0.15	0.12	0.18	0.006	0.005	0.007
D	15.75	15.57	15.92	0.620	0.613	0.627
E	9.65	9.52	9.78	0.380	0.375	0.385
E2	6.35	6.22	6.48	0.250	0.245	0.255
E3	1.65	1.52	1.78	0.065	0.060	0.070
e	0.635			0.025		
f	0.20			0.008		
L	8.38	6.85	9.40	0.330	0.270	0.370
Q	0.79	0.66	0.92	0.031	0.026	0.036
S1	0.43	0.25	0.61	0.017	0.010	0.024

7 Ordering information

Table 10. Order codes

Order code	Description	Temperature range	Package	Marking	Packing
RHFAC164245K1	Engineering model	-55 °C to 125 °C	Flat-48	RHFAC164245K1	Conductive strip pack
RHRAC164245K01V	QML-V flight			5962R9858008VYC	

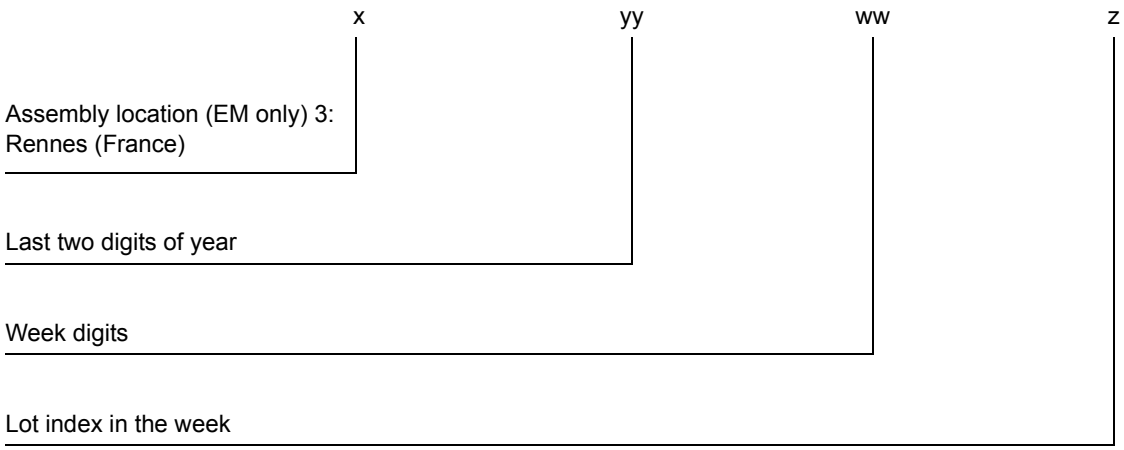
8 Other information

8.1 Data code

The date code is structured as shown below:

- EM xyywwz
- QML-V yywwz

where:



8.2 Documentation

Table 11. Documentation provided for ESCC flight

Quality level	Documentation
Engineering model	-
QML-V flight	Certificate of conformance QCI(1) (groups A, B, C, D, and E) Screening electrical data Precap report PIND(2) test SEM(3) inspection report X-Ray report

1. QCI = quality conformance inspection
2. PIND = particle impact noise detection
3. SEM = scanning electron microscope

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
23-Sep-2011	1	Initial release.
06-Apr-2012	2	Added Pin 4 description to *Table 3: Pin descriptions*.
29-Aug-2013	3	Minor changes to layout *Features*: Removed “Bus hold” *Table 1: Device summary*: updated order codes, quality level, and EPPL data. *Table 10: Order codes*: updated order codes and description data. Added *Section 8: Other information*
28-Apr-2014	4	*Table 11: Documentation provided for ESCC flight*: removed documentation for engineering model (there is none). Updated disclaimer

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