NEC

TFT COLOR LCD MODULE
NL128102AC31-02

51 cm (20.1 inches), 1280 1024 pixels, 8bit/color, Incorporated backlight and Inverter Ultra wide viewing angle

DESCRIPTION

NL128102AC31-02 is a TFT (Thin Film Transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight.
NL128102AC31-02 has a built-in backlight with the inverter.

The 51cm (20.1 Inches) diagonal display area contains 1280 x 1024 pixel and can display 16,777,216 colors simultaneously.

FEATURES

- Ultra-wide viewing angle
- High luminance (200 cd/m2 typ.)
- Low reflection and wide color gamut
- LVDS interface (THC63LVDF84A x 2 chips, THine Electronics, Inc.)
  8bit per color
- Incorporated direct type backlight (12 CCFLs with inverter)

APPLICATIONS

- Engineering work station, desk-top type of PC
- Display terminals for control system
- Monitors for process controller

The information in this document is subject to change without notice.

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NEC Electronics Inc.

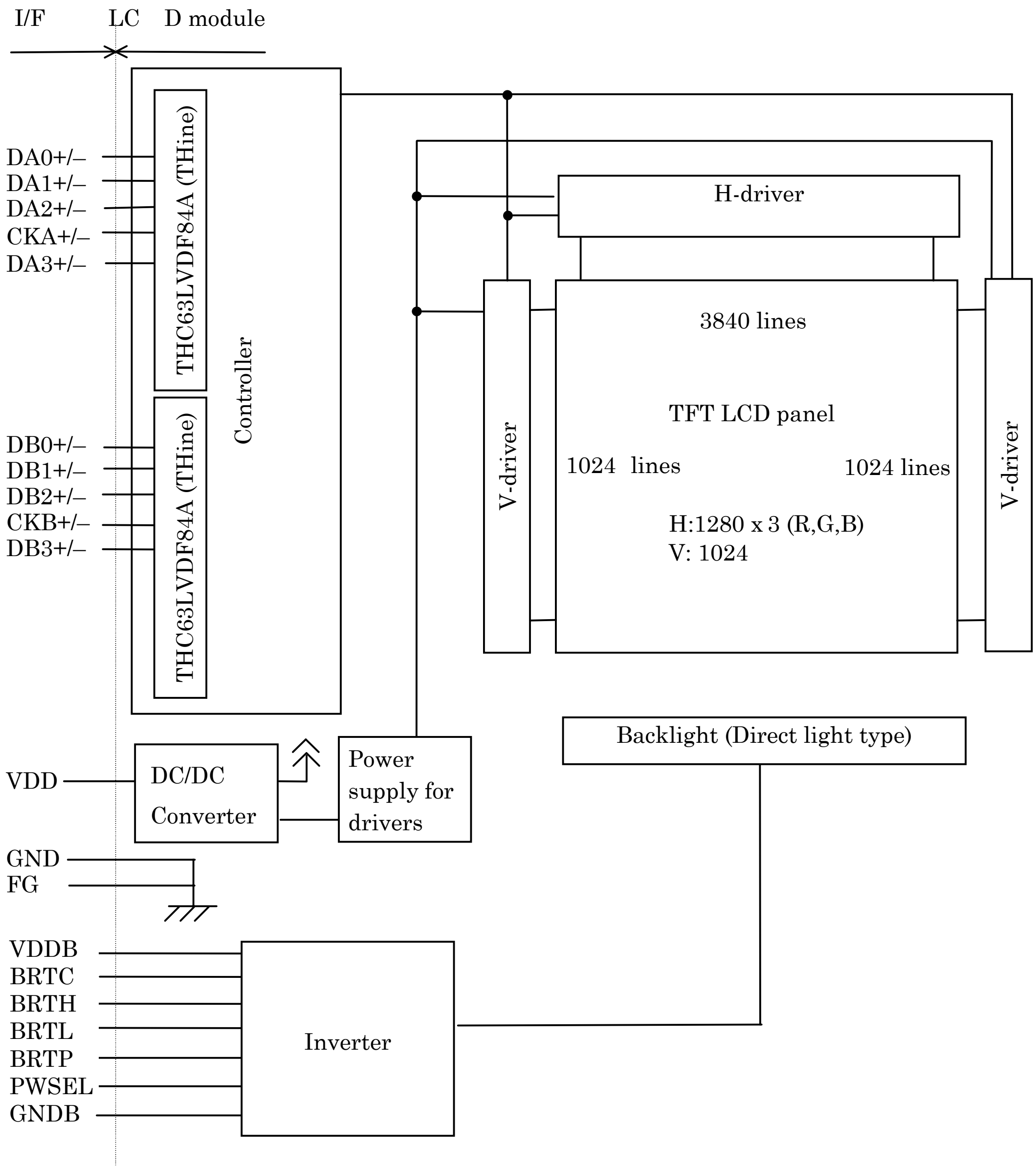
STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

BLOCK DIAGRAM



Remark GND (Signal Ground) is connected to FG (Frame Ground) in the LCD module. Neither GND nor FG is connected to GNDB (Backlight Ground). GND, FG and GNDB should be connected in the system ground.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	399.36 (H) x 319.49 (V)
Drive system	a-Si TFT active matrix
Display colors	16,777,216 colors
Number of pixels	1280 x 1024 pixels
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.312 (H) 0.312 (V) mm
Module size	470.0 (H) x 382.0 (V) x 42.5 (D) mm
Weight	2320 g (typ.)
Contrast ratio	250 : 1 (typ.)
Viewing angle (more than the contrast ratio of 10 : 1)	
	• Horizontal : 85° (typ., left side, right side)
	• Vertical : 85° (typ., up side, down side)
Designed viewing direction	• Optimum grayscale (r = 2.2): perpendicular
Polarizer pencil-hardness	3H (min., at JIS K5400)
Color gamut	60 % (typ., at center, to NTSC)
Response time	45 ms (typ.), "black" to "white"
Luminance	200 cd/m^2 (typ.)
Signal system	RGB 8-bit signals, Synchronous signals (Hsync, Vsync), Dot clock (CLK), DE LVDS interface (THC63LVDF84A, THine Electronics, Inc.)
Supply voltage	12 V (Logic, LCD driving), 12 V (Backlight)
Backlight	Direct light type: 12 CCFLs with inverter [Replaceable parts] • Lamp holder type No.: 201LHS02 • Inverter type No.: 201PW021
Power consumption	46.6 W (typ.)

GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	470.0 ± 1.0 (H) 382 ± 1.0 (V) 42.5 max. (D)	mm
Display area	399.36 (H) x 319.49 (V), Diagonal 51cm (20.1 inchies)	mm
Number of pixels	1280 (H) 1024 (V)	pixel
Dot pitch	0.104 (H) 0.312 (V)	mm
Pixel pitch	0.312 (H) 0.312 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	16,777,216 (8bit per color)	color
Weight	2430 (max.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +14.0	V	T_a = 25°C
	$V_{DD}B$	–0.3 to +14.0	V	
Logic input voltage (LCD)	Vi	- 0.3 to + 3.6	V	V_{DD}=12V, T_a = 25°C
Logic input voltage (backlight-BRTC signal)	ViBL1	–0.3 to +5.5	V	$V_{DD}B$=12V, T_a = 25°C
Logic input voltage (backlight-BRTL signal)	ViBL2	–0.3 to +1.5	V	
Storage temp.	T_{ST}	–20 to +60	°C	-
Operating temp.	T_{OP}	0 to +55	°C	Module surface
Humidity (No condensation)	–	95% relative humidity	–	T_a 40°C
	–	85% relative humidity	–	40 < T_a 50°C
	–	70% rel	–	50 < T 55°C
	–	Absolute humidity shall not exceed T_a = 55°C, 70% relative humidity level.	–	T_a > 55°C

Note: The temperature is measured at the surface of display.

ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving

T_a = 25°C

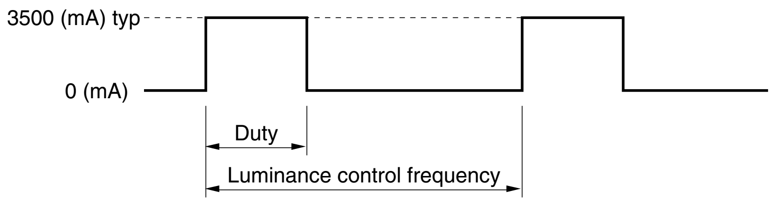
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply voltage	V_{DD}	11.4	12.0	12.6	V	–
Ripple voltage	V_{rp}	–	–	100	mV	for V_{DD}
LVDS signal input "L" voltage	V_{IL}	–100	–	–	mV	VCM = 1.2 V VCM: Common mode voltage in LVDS driver
LVDS signal input "H" voltage	V_{IH}	–	–	+100	mV	
Input voltage	V_i	0	–	2.4	V	–
Terminating resistor	R_t	–	100	–		–
Supply current	I_{DD}	–	380 **Note**	1000	mA	V_{DD} = 12.0V

Note Checkered flag pattern (in EIAJ ED-2522)

(2) Backlight

T_a = 25°C

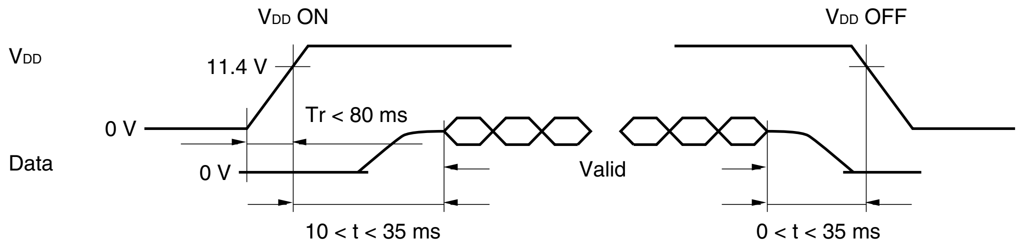
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply voltage	$V_{DD}B$	10.8	12.0	13.2	V	–
Logic input "L" current	IiBL1	-1.6	–	–	mA	for BRTC
Logic input "H" current	IiBL1	–	–	3.5	mA	
Logic input "L" current	IiBL2	-610	–	–	A	for BRTC, PWSEL
Logic input "H" current	IiBL2	–	–	440	A	
Supply current	$I_{DD}B$	–	3500	4200	mA	$V_{DD}B$ = 12 V (at max. luminance)

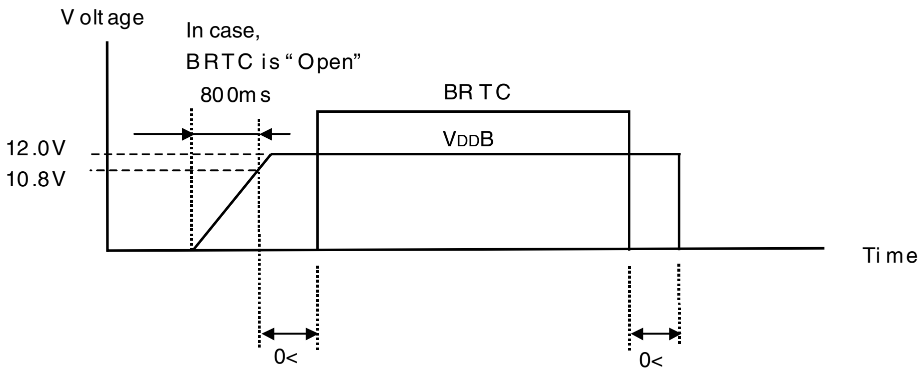


Maximum luminance control: 100 %
Minimum luminance control: 20 %
Luminance control frequency: 243 to 297 Hz, 270 Hz (typ.)

Note: The power supply line ($V_{DD}B$ and GNDB) has a large ripple noise while dimming. Certain consideration should be taken to reduce the noise.

SUPPLY VOLTAGE SEQUENCE





Notes 1. Data: pixel data and Pixel clock.

2. The supply voltage for input signals should be the same as V_{DD}.

3. Apply $V_{DD}B$ within the LCD operation period. When the backlight turns on before LCD operation or the LCD operation turns off before the backlight turns off, the display may momentarily become white. However, 12 V for backlight should be started up within 800ms, otherwise, the protection circuit makes the backlight turns off.

4. The backlight on/off signal (BRTC) should be controlled while logic signals are supplied.

5. Do not input "H" for PWSE, when $V_{DD}B$ is 0V or BRTC is "L".

6. When the power is off, please keep whole signals low level or high impedance.

INTERFACE PIN CONNECTION

(1) Interface connector for signal and power

Part No. : 53780-2010
Adaptable socket : 51146-2000
Supplier : Molex Incorporated

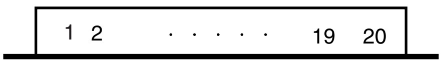
CN1

Pin No.	Symbol	Signal type	Function
1	NC	Non-connection	Keep the termainal open
2	NC		
3	GND	Ground	Connect to system ground
4	GND		
5	DA0-	Odd pixlel data input 0	Odd pixel data input 0 (LVDS level)
6	DA0+		
7	GND	Ground	Connect to system ground
8	DA1-	Odd pixlel data input 1	Odd pixel data input 1 (LVDS level)
9	DA1+		
10	GND	Ground	Connect to system ground
11	DA2-	Odd pixlel data input 2	Odd pixel data input 2 (LVDS level)
12	DA2+		
13	GND	Ground	Connect to system ground
14	CKA-	Odd pixlel clock input	Odd pixel clock input (LVDS level)
15	CKA+		
16	GND	Ground	Connect to system ground
17	DA3-	Odd pixlel data input 3	Odd pixel data input 3 (LVDS level)
18	DA3+		
19	GND	Ground	Connect to system ground
20	NC	Non-connection	Keep the termainal open

Notes 1. Signal ground for logic and LCD driving. GND should be connected to system ground. Neither GND nor GNDB is connected to frame.

2. Connect all pins and GND terminal. Cable use 100 twist pair.
Connect all pins (except 1, 2, 20) to avoid noise issue.
Use 100 twist pair wires for the cable.

CN1: Figure from socket view



Part No. : 53780-3010
Adaptable socket : 51146-3000
Supplier : Molex Incorporated.

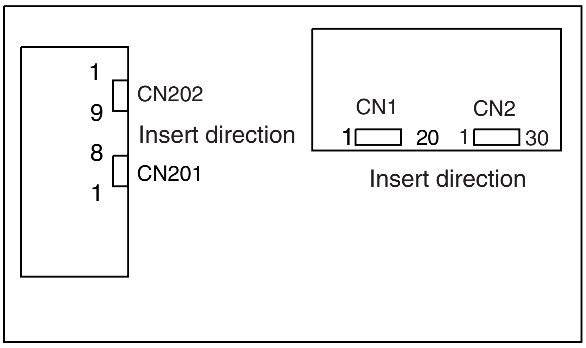
CN2

Pin No.	Symbols	Signal type	Function
1	N.C.	Non-connection	Keep the terminal open
2	N.C.		
3	GND	Ground	Connect to system ground
4	GND		
5	DB0-	Even Pixel Data0	Even pixel data input 0 (LVDS level)
6	DB0+		
7	GND	Ground	Connect to system ground
8	DB1-	Even Pixel Data1	Even pixel data input 1 (LVDS level)
9	DB1+		
10	GND	Ground	Connect to system ground
11	DB2-	Even Pixel Data 2	Even pixel data input 2 (LVDS level)
12	DB2+		
13	GND	Ground	Connect to system ground
14	CKB-	Even Pixel Clock	Even pixel clock input (LVDS level)
15	CKB+		
16	GND	Ground	Connect to system ground
17	DB3-	Even Pixel Data3	Even pixel data input 3 (LVDS level)
18	DB3+		
19	GND	Ground	Connect to system ground
20	Res.	Reserved	Keep the terminal open
21	Res.		
22	Res.		
23	Res.		
24	GND	Ground	Connect to system ground
25	GND		
26	GND		
27	N.C.	Non-connection	Keep the terminal open
28	VDD	+12V Power Supply	12V±5%
29	VDD		
30	VDD		

Note 1: GND is signal ground for logic and LCD driving. GND is connected to FG (Frame Ground) in the LCD module. Neither GND nor FG is connected to GNDB (Backlight Ground).
GND, FG and GNDB should be connected to the system ground.

Remark: Connect all pins except 1, 2 and 27 to avoid noise issues. Use 100 ohm twist pair wires for the cable.

CN2: Figure from stock view



(2) Connector for backlight unit

Part No. : DF3-8P-2H
Adaptable socket: DF3-8S-2C
Supplier : HIROSE Electric Co., Ltd.

CN201: Figure from socket view

1 2 .... 7 8

CN201

Pin No.	Symbols	Signal type	Function
1	GNDB	Ground for backlight	Note 1
2	GNDB		
3	GNDB		
4	GNDB		
5	VDDB	12V power supply	+12V+/-10%
6	VDDB		
7	VDDB		
8	VDDB		

Note 1. GNDB is not connected to GND or the frame.

Part No. ; IL-Z-9PL1-SMTY
Adaptable socket : IL-Z-9S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

CN202: Figure from socket view

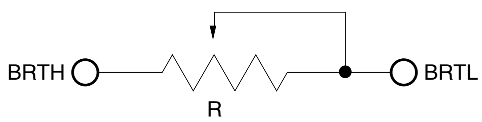
9 8 .... 2 1

CN202

Pin No.	Symbols	Signal type	Function
1	GNDB	Ground for backlight	Note 1
2	GNDB		
3	N.C.	Non-connection	Keep the terminal open
4	BRTC	Backlight ON/OFF control signal	"H" or "Open" Backlight on "L" Backlight off
5	BRTH	Luminance control signal	Note 2
6	BRTL	Luminance control signal	
7	BRTP	Luminance control signal	Note 2
8	GNDB	Ground for backlight	Note 1
9	PWSEL	Luminance control select signal	Note 2

Note 1. GNDB is not connected to GND or the frame.
2. There are three ways of controlling luminance.

1) A way of luminance control by a variable resistor (PWSEL="H" or "Open", BRTP="Open")
The variable resistor for luminance control should be 10 k type, and zero point of the resistor corresponds to the minimum of luminance.



Mating variable resistor : 10 K ±5 %, B curve
Maximum luminance (100 %): R = 10 K
Minimum luminance (30 %) : R = 0

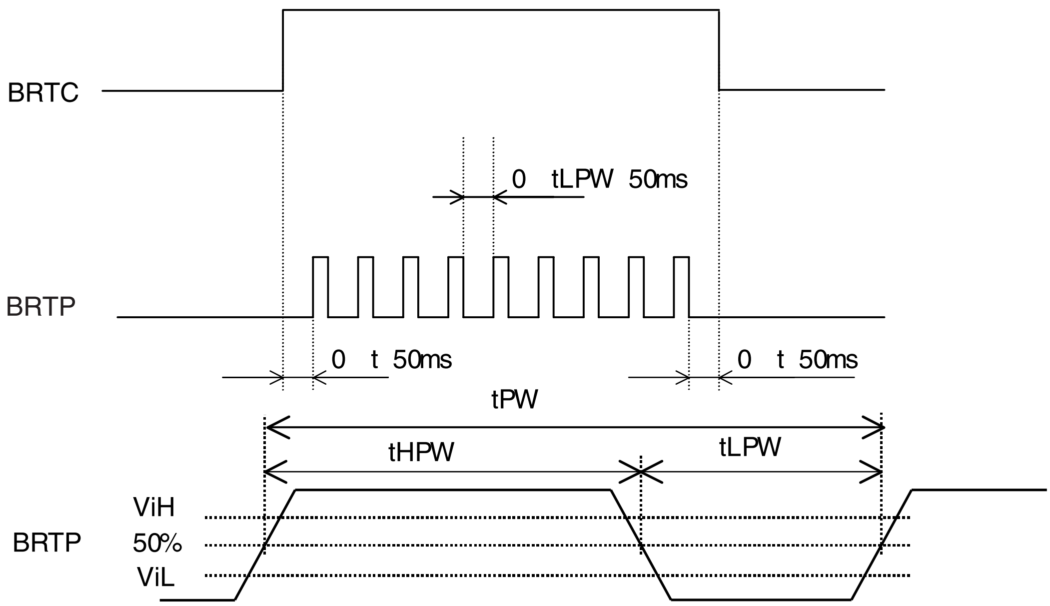
2) A way of luminance control by voltage (PWSEL="H" or "Open", BRTP="Open")
BRTH should be fixed to 0 V to control luminance by voltage. The range of input voltage between BRTL and GNDB is as follows.
Maximum luminance (100%) : 1 V (typ.)
Minimum luminance (30%) : 0 V

3) A way of luminance control by PWM

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.

Duty=100%: luminance is maximum.

Duty=20%: luminance is minimum.



Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
Frequency	1/tPW	185	-	325	Hz	-
"L" period	tLPW	-	-	50	ms	-
Pulse-width	tHPW/tPW	20	-	100	%	at Max. luminance (100%)
Input voltage	ViL	0	-	0.8	V	-
	ViH	2.0	-	5.25	V	-

Regarding set up for frequency, refer to the below method.

Set up frequency = Vsync frequency x (n+0.25) or (n+0.75)

Adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

(3) Display position of input data

D (0, 0)	D (1, 0)	---	D (X, 0)	---	D (1022, 0)	D (1023, 0)
D (0, 1)	D (1, 1)	---	D (X, 1)	---	D (1022, 1)	D (1023, 1)
¦	¦	-+-	¦	-+-	¦	¦
D (0, Y)	D (1, Y)	---	D (X, Y)	---	D (1022, Y)	D (1023, Y)
¦	¦	-+-	¦	-+-	¦	¦
D (0, 766)	D (1, 766)	---	D (X, 766)	---	D (1022, 766)	D (1023, 766)
D (0, 767)	D (1, 767)	---	D (X, 767)	---	D (1022, 767)	D (1023, 767)

METHOD OF CONNECTION FOR THC63LVDF63A

System side ◀──▶ LCD module side

			TRANSMITTER					I/F CN				RECIVER				INPUT to LCD
			pin	THC63LVDF83A		pin		pin	CN1		pin		THC63LVDM84A	pin		
Odd pixel data and control data	RA	->	51	TA0				1	N.C.				RA0	27	->	RA2
	RA	->	52	TA1				2	N.C.				RA1	29	->	RA3
	RA	->	54	TA2				3	GND				RA2	30	->	RA4
	RA	->	55	TA3				4	GND				RA3	32	->	RA5
	RA	->	56	TA4	TA-	48	->	5	DA0-	->	9	RA-	RA4	33	->	RA6
	RA	->	3	TA5	TA+	47	->	6	DA0+	->	10	RA+	RA5	35	->	RA7
	GA2	->	4	TA6				7	GND				RA6	37	->	GA2
	GA3	->	6	TB0	TB-	46	->	8	DA1-	->	11	RB-	RB0	38	->	GA3
	GA4	->	7	TB1	TB+	45	->	9	DA1+	->	12	RB+	RB1	39	->	GA4
	GA5	->	11	TB2				10	GND				RB2	43	->	GA5
	GA6	->	12	TB3	TC-	42	->	11	DA2-	->	15	RC-	RB3	45	->	GA6
	GA7	->	14	TB4	TC+	41	->	12	DA2+	->	16	RC+	RB4	46	->	GA7
	BA2	->	15	TB5				13	GND				RB5	47	->	BA2
	BA3	->	19	TB6	TCLK-	40	->	14	CKA-	->	17	RCLK-	RB6	51	->	BA3
	BA4	->	20	TC0	TCLK+	39	->	15	CKA+	->	18	RCLK+	RC0	53	->	BA4
	BA5	->	22	TC1				16	GND				RC1	54	->	BA5
	BA6	->	23	TC2	TD-	38	->	17	DA3-	->	19	RD-	RC2	55	->	BA6
	BA7	->	24	TC3	TD+	37	->	18	DA3+	->	20	RD+	RC3	1	->	BA7
	Hsync	->	27	TC4				19	GND				RC4	3	->	Hsync
	Vsync	->	28	TC5				20	Reserved				RC5	5	->	Vsync
	DE	->	30	TC6									RC6	6	->	DE
	RA0	->	50	TD0									RD0	7	->	RA0
	RA1	->	2	TD1									RD1	34	->	RA1
	GA0	->	8	TD2									RD2	41	->	GA0
	GA1	->	10	TD3									RD3	42	->	GA1
	BA0	->	16	TD4									RD4	49	->	BA0
	BA1	->	18	TD5									RD5	50	->	BA1
	RSVD	->	25	TD6									RD6	2	->	RSVD
	CLK	->	31	CLKIN				pin	CN2				CLKOUT	26	->	CLKA
Even pixel data	RB2	->	51	TA0				1	N.C.				RA0	27	->	RB2
	RB3	->	52	TA1				2	N.C.				RA1	29	->	RB3
	RB4	->	54	TA2				3	GND				RA2	30	->	RB4
	RB5	->	55	TA3				4	GND				RA3	32	->	RB5
	RB6	->	56	TA4	TA-	48	->	5	DB0-	->	9	RA-	RA4	33	->	RB6
	RB7	->	3	TA5	TA+	47	->	6	DB0+	->	10	RA+	RA5	35	->	RB7
	GB2	->	4	TA6				7	GND				RA6	37	->	GB2
	GB3	->	6	TB0	TB-	46	->	8	DB1-	->	11	RB-	RB0	38	->	GB3
	GB4	->	7	TB1	TB+	45	->	9	DB1+	->	12	RB+	RB1	39	->	GB4
	GB5	->	11	TB2				10	GND				RB2	43	->	GB5
	GB6	->	12	TB3	TC-	42	->	11	DB2-	->	15	RC-	RB3	45	->	GB6
	GB7	->	14	TB4	TC+	41	->	12	DB2+	->	16	RC+	RB4	46	->	GB7
	BB2	->	15	TB5				13	GND				RB5	47	->	BB2
	BB3	->	19	TB6	TCLK-	40	->	14	CKB-	->	17	RCLK-	RB6	51	->	BB3
	BB4	->	20	TC0	TCLK+	39	->	15	CKB+	->	18	RCLK+	RC0	53	->	BB4
	BB5	->	22	TC1				16	GND				RC1	54	->	BB5
	BB6	->	23	TC2	TD-	38	->	17	DB3-	->	19	RD-	RC2	55	->	BB6
	BB7	->	24	TC3	TD+	37	->	18	DB3+	->	20	RD+	RC3	1	->	BB7
	RSVD	->	27	TC4				19	GND				RC4	3	->	RSVD
	RSVD	->	28	TC5				20	Reserved				RC5	5	->	RSVD
	RSVD	->	30	TC6				21	Reserved				RC6	6	->	RSVD
	RB0	->	50	TD0				22	Reserved				RD0	7	->	RB0
	RB1	->	2	TD1				23	Reserved				RD1	34	->	RB1
	GB0	->	8	TD2				24	GND				RD2	41	->	GB
	GB1	->	10	TD3				25	GND				RD3	42	->	GB
	BB0	->	16	TD4				26	GND				RD4	49	->	BB0
	BB1	->	18	TD5				27	N.C.				RD5	50	->	BB1
	RSVD	->	25	TD6				28	VDD:12V				RD6	2	->	RSVD
	CLK	->	31	CLKIN				29	VDD:12V				CLKOUT	26	->	CLKB
								30	VDD:12V							

Notes 1. 100 twist pair.

DISPLAY COLORS vs. INPUT DATA SIGNALS

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7 RB7	RA6 RB6	RA5 RB5	RA4 RB4	RA3 RB3	RA2 RB2	RA1 RB1	RA0 RB0	GA7 GB7	GA6 GB6	GA5 GB5	GA4 GB4	GA3 GB3	GA2 GB2	GA1 GB1	GA0 GB0	BA7 BB7	BA6 BB6	BA5 BB5	BA4 BB4	BA3 BB3	BA2 BB2	BA1 BB1	BA0 BB0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					:								:								:				
					:								:								:				
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
					:								:								:				
					:								:								:				
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
					:								:								:				
					:								:								:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note Colors are developed in combination with 8-bit signals (256 steps in grayscale) of each primary red, green, and blue color.
This process can result in up to 16,777,216 (256 x 256 x 256) colors.

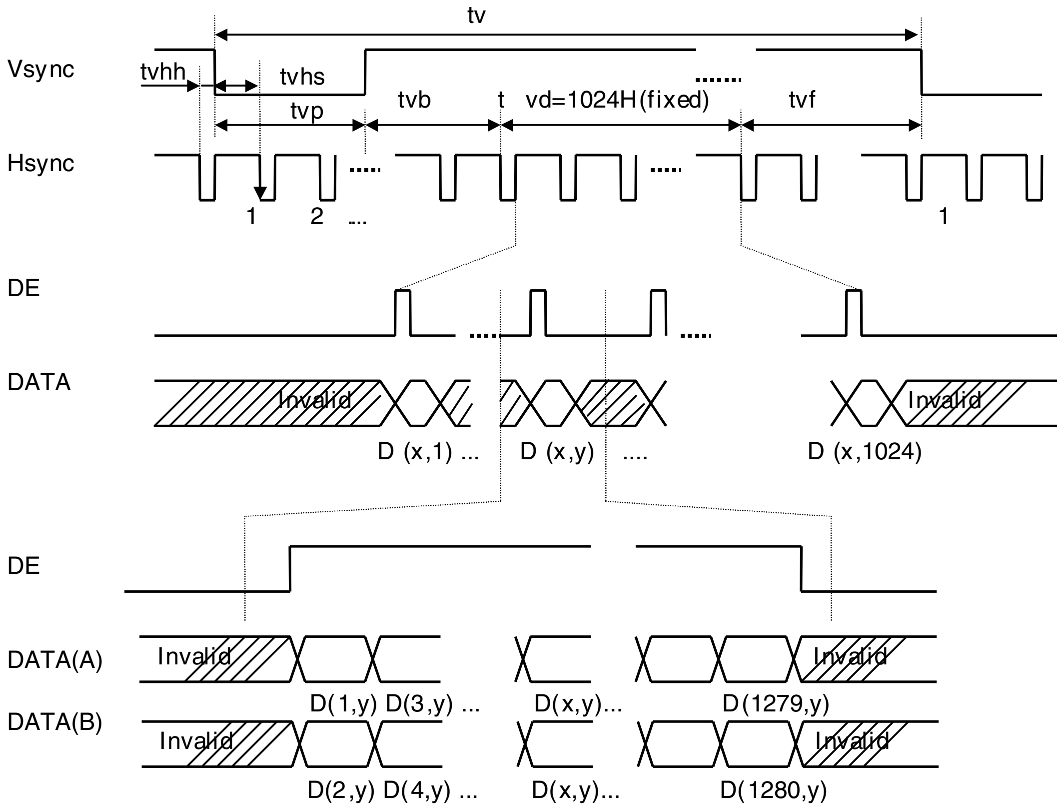
INPUT SIGNAL TIMING

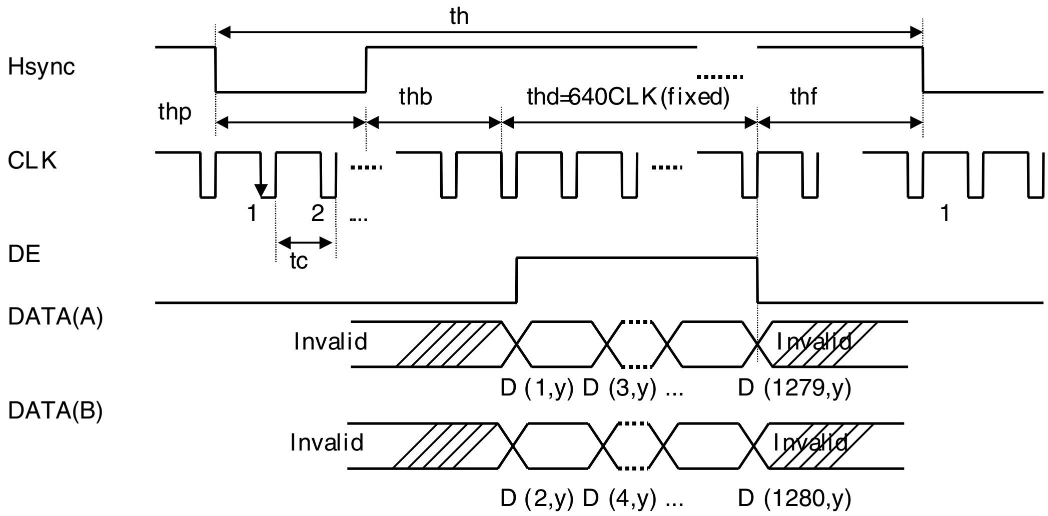
(1) Input signal specifications for LCD controller

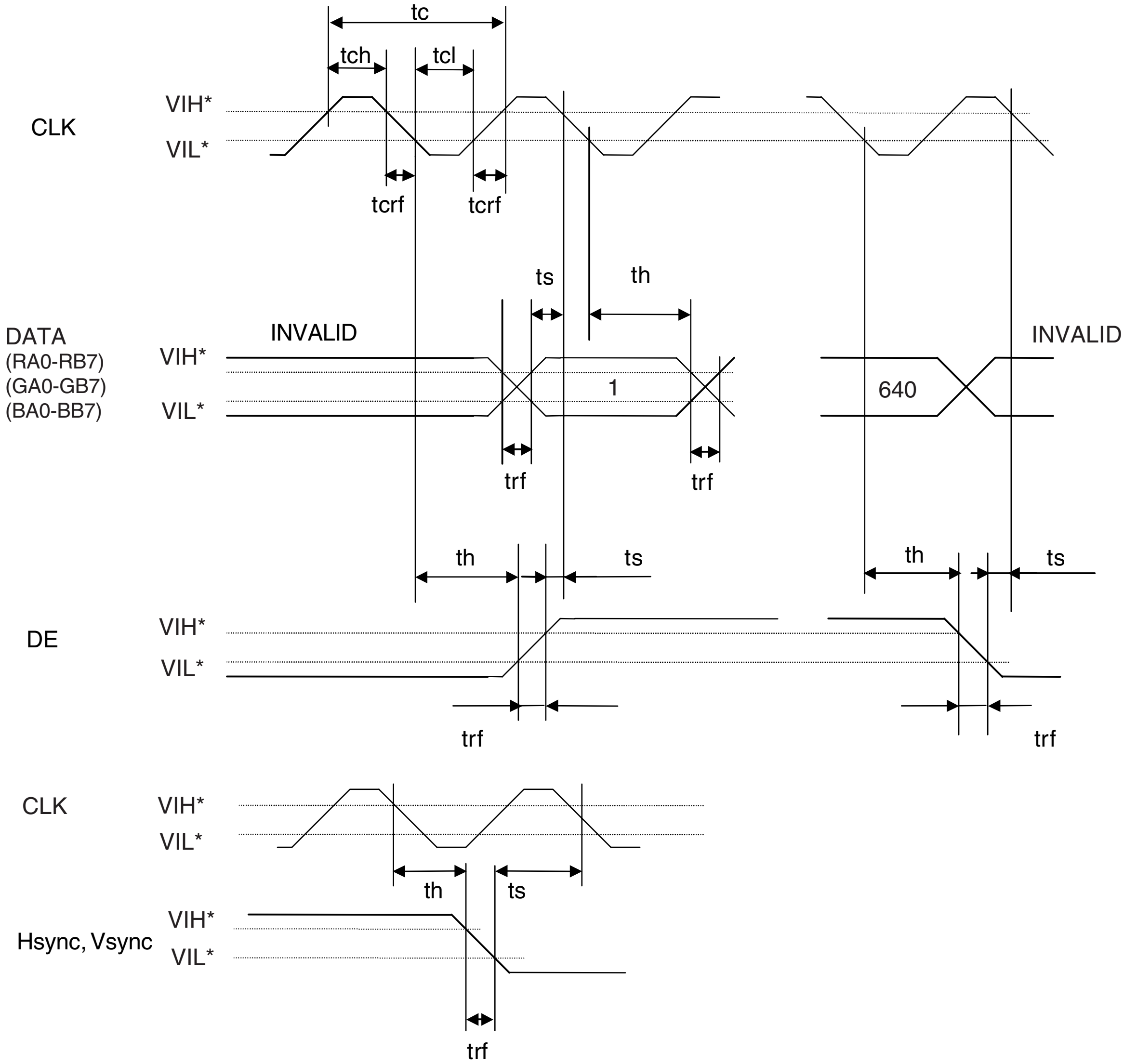
	Parameters		Symbols	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	Vf =75Hz	1/ tc	65.0 -	67.5 14.815	70.0 -	MHz ns	-
		Vf =60Hz		51.5 -	54.0 18.52	56.5 -	MHz ns	
	Duty		tc/tcl	Note 1			-	-
	Rise, fall		tcrf				ns	-
Hsync	Period	Vf =75Hz	th	(12.3) (750)	12.504 844	- -	s CLK	Typ=80.0kHz
		Vf =60Hz		(12.3) (750)	15.630 844	- -	s CLK	Typ=64.0kHz
	Display period		thd	-	640	-	CLK	-
	Front-porch		thf	-	-	-	CLK	-
	Pulse width	Vf =75Hz	thp *	-	72	-	CLK	-
		Vf =60Hz		-	56	-	CLK	-
	Back-porch		thb *	-	124	-	CLK	-
	* thp + thb			(110)	-	-	CLK	-
Vsync	Period	Vf =75Hz	tv	- (1027)	13.329 1066	- -	ms H	Typ=75.0Hz
		Vf =60Hz		- (1027)	16.661 1066	- -	ms H	Typ=60.0Hz
	Display period		tvd	-	1024	-	H	-
	Front-porch		tvf *	-	1	-	H	-
	Pulse width		tvp *	-	3	-	H	-
	Back-porch		tvb *		38	-	H	-
	* tvp + tvb +tvf			(1980)	-	-	CLK	-
	Vsync-Hsync timing		tvhs	1	-	-	CLK	-
	Hsync-Vsync timing		tvhh	1	-	-	CLK	-
DATA	DATA-CLK (Set up)		ts	Note 1			ns	-
	CLK-DATA (Hold)		th				ns	-
	Rise, fall		trf				ns	-

Note These values are in the timing regulation of THC63LVDM83A (THine).
The product equivalent to THC63LVDM83A (THine) is recommended to the input of LVDS transmitter.
The Timing regulation prescribes in the input of the LVDS transmitter.

(2) Definition of input signal timing







*1: Refer to the specification of LVDS manufacture for the detail timing design.

(3) Display positions of input data

Odd Pixel: RA = R DATA Even Pixel : RB =R DATA
Odd Pixel: GA= G DATA Even Pixel : GB =G DATA
Odd Pixel: BA = B DATA Even Pixel : BB =B DATA

D (1, 1)			D (1, 2)		
RA	GA	BA	RB	GB	BB

D(1, 1)	D(1, 2)		D(1, 1280)
D(2, 1)	D(2, 2)		D(2, 1280)
D(1024,1)	D(1024,2)		D(1024,1280)

Memo

Intentionally blank

OPTICAL CHARACTERISTICS

(T_a = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V)

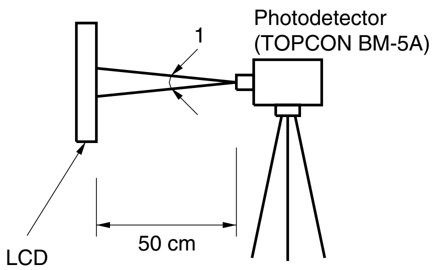
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remark
Luminance	Lumax	"White"	150	200	–	cd/m^2	**Note 1**
Contrast ratio	CR	X = ±0°, Y = ±0°, at center	150	250	–	–	**Note 2**
Luminance uniformity	–	$\frac{\text{Maximum}}{\text{luminance}}$	–	1.1	1.30	–	**Note 3**

Reference data

(T_a = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remark
Chromaticity Coordinate			Y = ±0° X = ±0°	–		–	–	
Viewing angle range	Horizontal	X+	CR > 10, Y = ±0°	70	85	–	deg.	**Note 4**
		X–	CR > 10, Y = ±0°	70	85	–	deg.	
	Vertical	Y+	CR > 10, X = ±0°	70	85	–	deg.	
		Y–	CR > 10, X = ±0°	70	85	–	deg.	
Color gamut		C	To NTSC	50	60	–	%	–
Response time		ton	White to black	–	45	TBD	ms	**Note 5**
		toff	Black to white	–	35	TBD		

Notes 1. The luminance is measured after 20 minutes from the module works, with all pixels in white. Typical value is measured after luminance saturation.

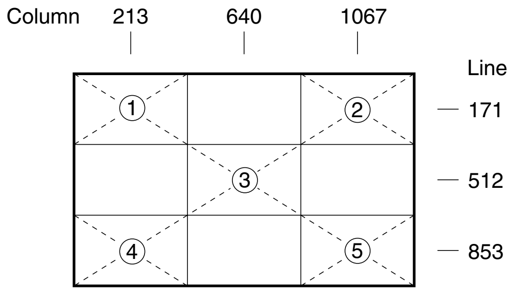


2. The contrast ratio is calculated by using the following formula.

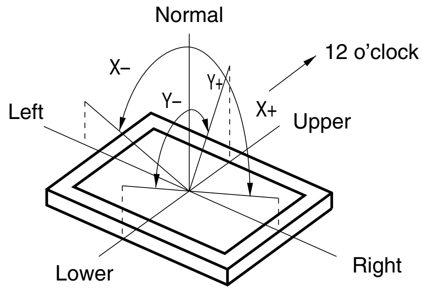
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in white}}{\text{Luminance with all pixels in black}}$$

The Luminance is measured in darkroom.

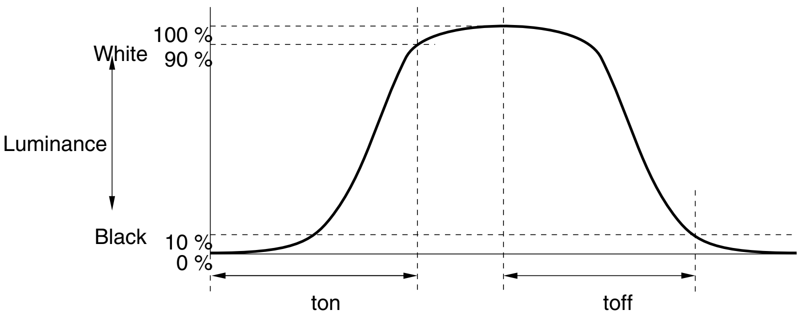
3. The luminance is measured at near the five points shown below.



4. Definitions of viewing angle are as follows.



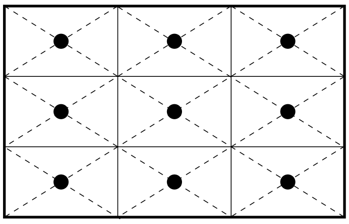
5. Definition of response time is as follows.
Photo-detector output signal is measured when the luminance changes "white" to "black" or "black" to "white".



RELIABILITY TEST

Test item	Test condition
High temperature/humidity operation **Note 1**	60 ± 2°C, 60% relative humidity 240 hours Display data is black.
Heat cycle (operation) **Note 1**	<1> 0°C ± 3°C ··· 1 hour 55°C ± 3°C ··· 1 hour <2> 50 cycles, 4 hours/cycle <3> Display data is black.
Thermal shock (non-operation) **Note 1**	<1> –20°C ± 3°C ··· 30 minutes 60°C ± 3°C ··· 30 minutes <2> 100 cycles <3> Temperature transition time within 5 minutes
Vibration (non-operation) **Notes 1, 2**	<1> 5 - 100 Hz, 1.2G 1 minute/cycle X, Y, Z direction <2> 50 times each direction
Mechanical shock (non-operation) **Notes 1, 2**	<1> 30 G, 11 ms X, Y, Z direction <2> 3 times each direction
ESD (operation) **Notes 1, 3**	150 pF, 150 , ±10 kV 9 places on a panel 10 times each place at one-second intervals
Dust (operation) **Note 1**	15 kinds of dust (JIS Z 8901) Hourly 15 seconds stir, 8 times repeat

Notes 1. Display function is checked by the same condition as LCD module out-going inspection.
2. Physical damage.
3. Discharge points "z " are shown in the figure.



GENERAL CAUTIONS

Next figures and sentence are very important. Please understand these contents as follows.

CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate

CAUTION

Do not touch an inverter, on which is stuck a caution label, while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module
- a) Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module
- a) As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.
- b) As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- c) As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- d) Do not pull the interface connectors in or out while the LCD module is operating.
- e) Put the module display side down on a flat horizontal plane.
- f) Handle connectors and cables with care.
- g) When the module is operating, do not lose CLK, Hsync or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.
- h) The torque to mounting screw should never exceed 0.392 N·m (4 kgf·cm).

(3) Cautions for the atmosphere
- a) Dew drop atmosphere should be avoided.
- b) Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an anti-static pouch and under the room temperature atmosphere is recommended.
- c) This module uses cold cathod fluorescent lamp. Therefore, the life time of lamp becomes short if the module is operated under the low temperature environment.
- d) Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

a) Do not apply fixed pattern data signal for a long time to the LCD module. It may cause image sticking. Please use screen savers if the display pattern is fixed more than one hour.

b) This module has the retardation film which may cause the variation of the color hue in the different viewing angles. The ununiformity may appear on the screen under the high temperature operation.

c) The light vertical stripe may be observed depending on the display pattern. This is not defects or malfunctions.

d) The noise from the inverter circuit may be observed in the luminance control mode. This is not defects or malfunctions.

(5) Other cautions

a) Do not disassemble and/or reassemble LCD module.

b) Do not readjust variable resistors or switches in the module.

c) When returning the module for repair or etc, please pack the module properly to avoid any damages. We recommend using the original shipping packages.

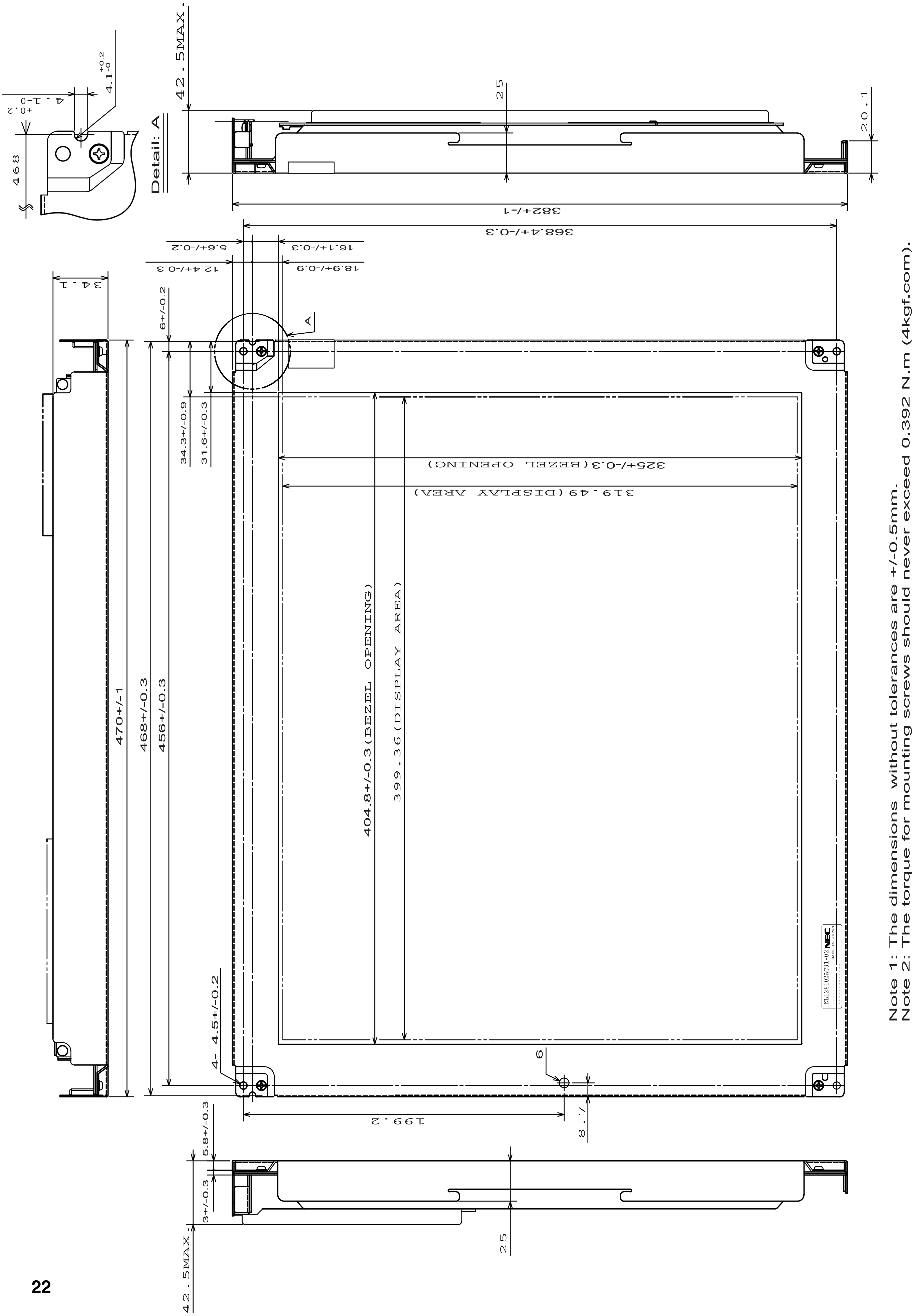
d) In case that the scan converter is used to convert VGA signal to NTSC, it is recommended using the frame-memory type, not the line-memory.

Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

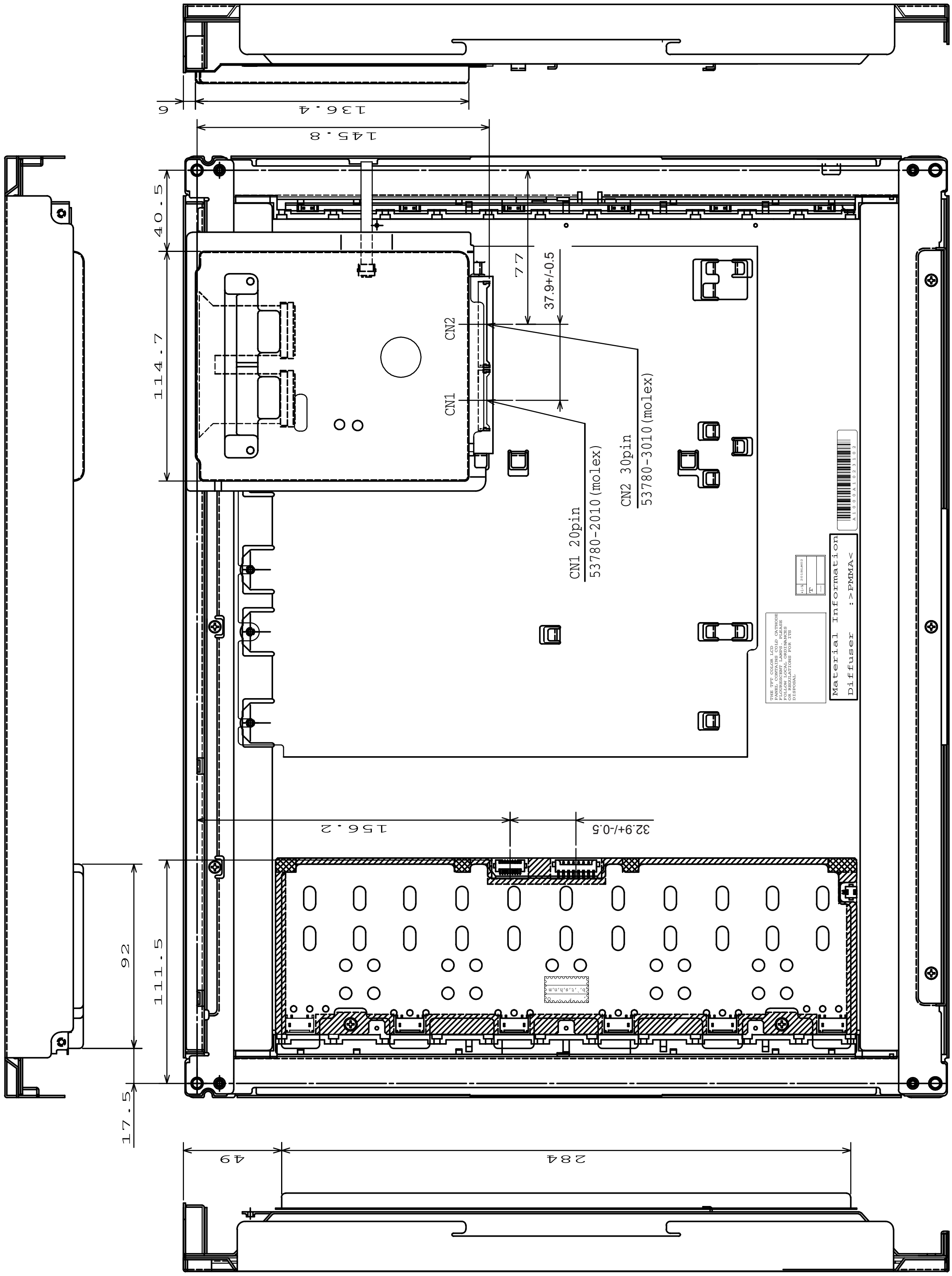
The optical characteristics of this module may be affected by the ambient temperature.
This module has cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will be changed by the progress in time.

Uneven brightness and/or small spots may be observed depending on different display patterns.

OUTLINE DRAWING (1/2): Front View (Unit: mm)



OUTLINE DRAWING (2/2): Rear View (Unit: mm)



Note 1: The dimensions without tolerances are +/-1.0mm.
Note 2: The torque for mounting screws should never exceed 0.392 N.m (4kgf.com).