LC78616PE

Advance Information

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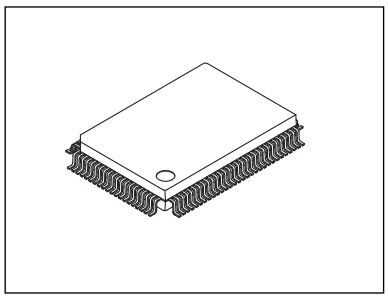
CMOS LSI

Compact Disc Player IC

Overview

The LC78616PE integrates RF signal processor for CD-DA/R/RW, servo control, EFM signal processing, anti-shock processing and playback controller (Sequencer : 8-bit CPU). It is possible to make CD player system using with micro controller, driver and SDRAM IC's with less components.



PQFP100 14x20 / QIP100E

Features

- RF signal processing for CD-DA/R/RW, servo control and EFM signal processing
- Outputs CDDA, CDROM data
- Maximum approximately 40 seconds shock protection by shock proof function with external 64M-bit SDRAM
- CD-TEXT decoded data are stored in external SDRAM.
- CD playback system is realized with simple macro commands by the external controller because of the internal Sequencer (8-bit CPU).
- Operating Voltage : 3.3V Typical
- Operating Temperature : –40°C to +85°C
- Package : QIP100E(14×20)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

January 2015 - Rev. P0

Publication Order Number :
LC78616PE/D

Detail of Functions

[CD-DSP functions]

< Playback functions>

- Playback mode : CLV playback / Jitter free playback (VCEC)
- Playback speed : Normal speed, double speed, quadruple speed (CLV playback / Jitter free playback)

<RF processing block>

- RF system : AGC, CD-R and CD-R/W playback support, peak hold, bottom hold
- Error system : TE signal generation, FE signal generation
- Detection : Track count signal, Jitter, Defect (black, mirror)
- LASER power controller (APC)
- DC offset voltage cancellation

<Servo control block>

- All servo systems as tracking, focus, sled and spindle are implemented with digital processing.
- Automatic adjustment functions : focus gain, focus bias, focus offset, tracking gain, tracking offset and tracking balance
- Shock detection / Interruption detection

<CD signal processing block>

- EFM signal synchronization detection, protection and interpolation
- Error detection, correction (C1=double, C2=quadruple/double)
- Jitter margin ±19 frames

<CD-TEXT processing block>

- Buffers CD-TEXT decoded data to the buffer memory.
- Starts buffering of CD-TEXT decoded data from desired ID3/ID4.

<Shock proof processing block>

- Shock proof processing using with external 16M-bit or 64M-bit Memory
  Approximately 10sec. with 16M-bit or 40sec. with 64M-bit

[CD data processing functions]

<CDDA data processing block>

- Interpolation
- Mute function (−12dB, −∞)
- Digital attenuator
- De-emphasis filter

<CDROM data processing block>

- CLV playback : Fixed normal speed or double speed
- Jitter free playback (VCEC) : Free speed within quadruple speed

*CDROM Data is not buffering to SDRAM and output directly

<Outputs format>

- Digital 3 lines output(LRCK,BCK,DATA)
- Supports various external audio data output format
  IIS (48fs), MSB First, Right-Justified, Left-Justified (32fs/48fs), 16 bit data length
- Slave mode
  Output DATA synchronized to external Clock input (LRCK and BCK)
- Digital output (S/PDIF, only CLV playback mode)

[Internal Microcontroller functions]

<Sequencer control>

- CD playback control
  Servo control, CD-TEXT processing, Digital data output control, etc.

<Communication control between main controller>

- The SIO interface using CE, CL, DI, DO and BUSYB pins is available as communication format.
- External main controller can control this IC directly such as “stop oscillation” or “restart oscillation” or so on at the internal register open mode (REG_READY high condition).
- Even while the oscillation is stopped, some of general port can be controlled by host controller.

<Peripheral interface block>

- GPIO port 8 ports maximum (Shared with other functionslerate.)

<Program memory block>

- Mask-ROM type
- ROM Collect function is built in for the partial change of the program and Host controller can use this.

<Others>

- Watch Dog Timer
  Notifies to outside from a pin or resets internally.
- Power management (Two kinds of sleep mode)
  (1) Only the clock for CPU core is operating and clocks for other blocks are stopping.
  (2) All clocks are stopping.

[Others]

<Internal power supply>

- 1.5V regulator for internal blocks

Specifications

Absolute Maximum Ratings at Ta=25°C, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	DVDD, AVDD, XVDD, VVDD1	–0.3 to +3.95	V
Input voltage 1	V_{IN}1		–0.3 to DV_{DD}+0.3	
Output voltage	V_{OUT}		–0.3 to DV_{DD} +0.3	
Allowable power dissipation	Pd max	Ta ≤ 85°C Mounted reference PCB(*)	300	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–40 to +125	

(*) Reference PCB : 114.3mm×76.1mm×1.6mm, glass epoxy resin

<Notes>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta=–40 to 85°C, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

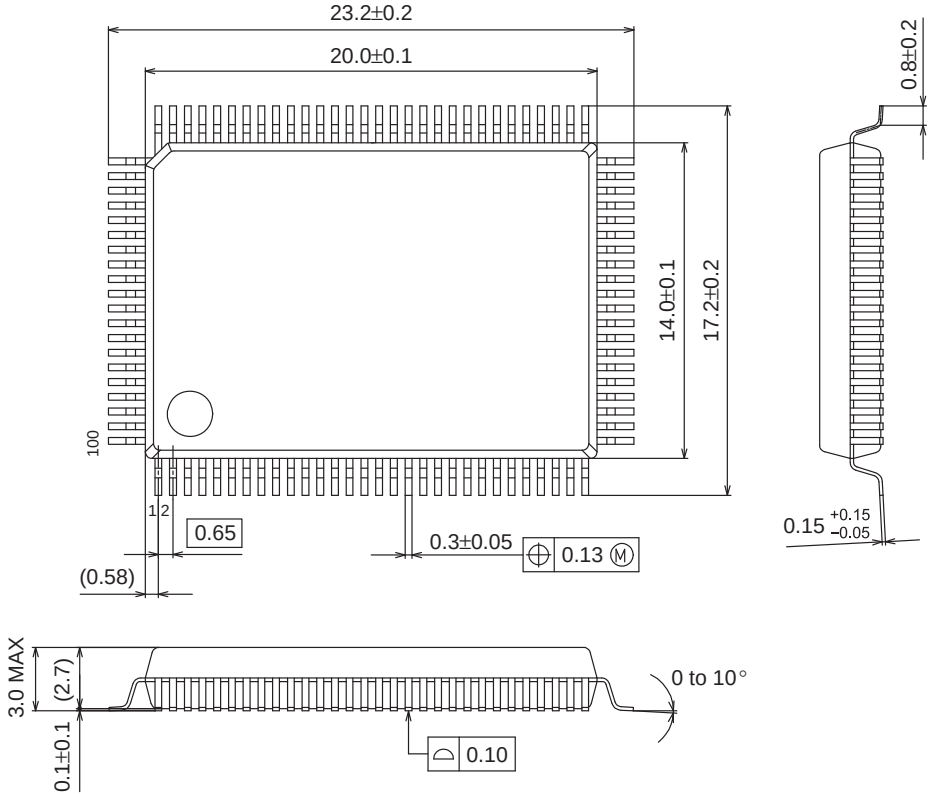
Parameter	Symbol	Pin Names	Type	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}	DVDD, AVDD, XVDD, VVDD1			3.00		3.60	V
High-level input voltage	V_{IH}	XIN,RESB, MODE, MODE3, CE, CL, DI, CONT00, CONT01, CONT02, CONT03, CONT04, CONT05, CONT08, CONT09, CONT10, DO, SDDAT00 to 15, SDADRS11, SDADRS12	Schmitt		2.00		V_{DD}	
Low-level input voltage	V_{IL}	XIN, RESB, TEST, MODE3, CE, CL, DI, CONT00, CONT01, CONT02, CONT03, CONT04, CONT05, CONT08, CONT09, CONT10, DO, SDDAT00 to 15, SDADRS11, SDADRS12	Schmitt		0.00		0.80	
Crystal Oscillator Frequency	FX	XIN XOUT	Oscillator circuit			16.9344		MHz
External clock Input	EXCK	XIN	Schmitt			16.9344	18.0	MHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

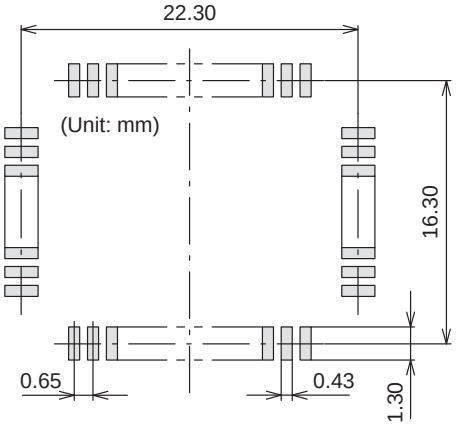
Package Dimensions

unit : mm

PQFP100 14x20 / QIP100E
CASE 122BV
ISSUE A



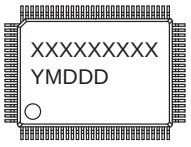
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

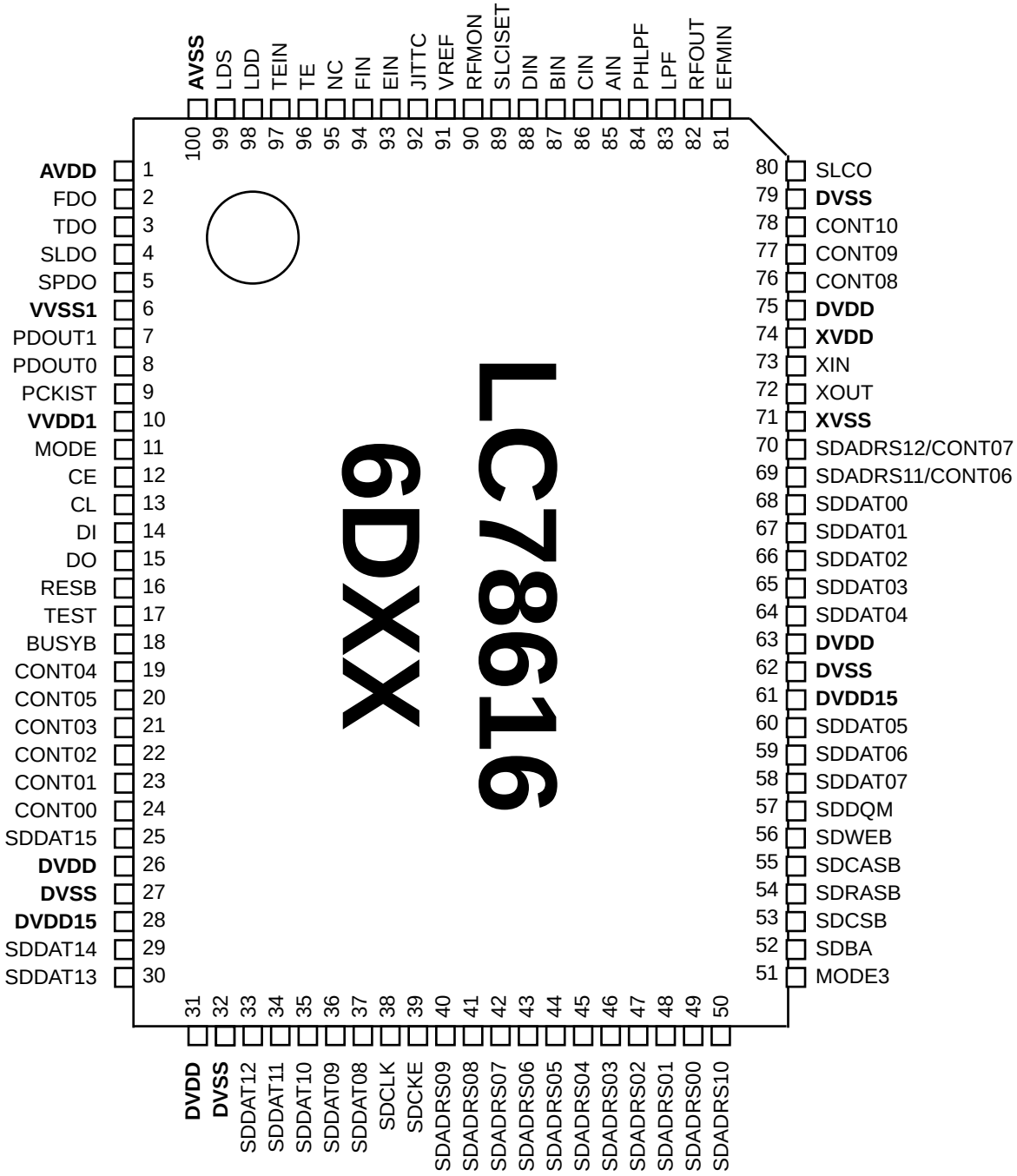
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

PIN Assignment



Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	AVDD	–	–	Analog system power supply
2	FDO	AO	AVDD/2	Focus control signal output
3	TDO	AO	AVDD/2	Tracking control signal output
4	SLDO	AO	AVDD/2	Sled control signal output
5	SPDO	AO	AVDD/2	Spindle control signal output
6	VVSS1	–	–	EFMPLL ground. This pin must be connected to the 0V level.
7	PDOUT1	AO	Undefined	EFMPLL charge pump output 1
8	PDOUT0	AO	Undefined	EFMPLL charge pump output 0
9	PCKIST	AI	Input	EFMPLL charge pump current setting resistor connection pin
10	VVDD1	–	–	EFMPLL power supply
11	MODE	I	Input	LSI mode set pin. This pin must be connected to the DVDD level.
12	CE	I	Input	Host I/F Enable signal input for serial communication This pin must be connected to the 0V level in IIC communication mode.
13	CL	I/O	Input	Host I/F Data transfer clock input for serial communication Data transfer clock input for IIC communication (N-ch. open drain)
14	DI	I/O	Input	Host I/F Data input for serial communication Data input/output for IIC communication (N-ch. open drain)
15	DO	I/O	Input	Host I/F Data output for serial communication This pin must be pulled down to the 0V level or be pulled up to the DVDD level in IIC communication mode.
16	RESB	I	Input	IC reset input.(Low active) This pin must be set low once after power is first applied.
17	TEST	I	Input	Test input. This pin must be connected to the 0V level.
18	BUSYB	O	Low	Host I/F BUSYB output(High : Communication available)
19	CONT04	I/O	Input	General purpose I/O port with pull down resistor Digital audio output<S/PDIF> FS384 clock output for Audio DAC Clock input/output for CDTEXT interface (exclusive with CONT01 and CONT09) Watch Dog Timer state monitor output
20	CONT05	I/O	Input	General purpose I/O port with pull down resistor Serial data output for CDTEXT interface
21	CONT03	I/O	Input	General purpose I/O port with pull down resistor Digital audio output<S/PDIF> FS384 clock output for Audio DAC SBCK clock input for CD subcode data Data request signal input for CDTEXT interface (exclusive with CONT00 and CONT08) Watch Dog Timer state monitor output
22	CONT02	I/O	Input	General purpose I/O port with pull down resistor Data output for Digital Audio interface PW data output in CD subcode Serial data output for CDTEXT interface
23	CONT01	I/O	Input	General purpose I/O port with pull down resistor Bit clock output for CD data Bit clock input for CD data (exclusive with CONT09) Frame synchronization signal (SFSY) output for CD subcode Clock input/output for CDTEXT interface (exclusive with CONT04 and CONT09)
24	CONT00	I/O	Input	General purpose I/O port LR clock output for CD data LR clock input for CD data (exclusive with CONT08) Block synchronization signal (SBSY) output for CD subcode Data request signal input for CDTEXT interface (exclusive with CONT03 and CONT08)
25	SDDAT15	I/O	Input(Low)	SDRAM data 15

Pin No.	Pin name	I/O	State when "Reset"	Function
26	DVDD	–	–	Digital system power supply
27	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
28	DVDD15	AO	High	Capacitor connection pin for internal regulator
29	SDDAT14	I/O	Input(Low)	SDRAM data 14
30	SDDAT13	I/O	Input(Low)	SDRAM data 13
31	DVDD	–	–	Digital system power supply
32	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
33	SDDAT12	I/O	Input(Low)	SDRAM data 12
34	SDDAT11	I/O	Input(Low)	SDRAM data 11
35	SDDAT10	I/O	Input(Low)	SDRAM data 10
36	SDDAT09	I/O	Input(Low)	SDRAM data 9
37	SDDAT08	I/O	Input(Low)	SDRAM data 8
38	SDCLK	O	Low	SDRAM system clock output
39	SDCKE	O	Low	SDRAM clock enable output
40	SDADRS09	O	Low	SDRAM address output 9
41	SDADRS08	O	Low	SDRAM address output 8
42	SDADRS07	O	Low	SDRAM address output 7
43	SDADRS06	O	Low	SDRAM address output 6
44	SDADRS05	O	Low	SDRAM address output 5
45	SDADRS04	O	Low	SDRAM address output 4
46	SDADRS03	O	Low	SDRAM address output 3
47	SDADRS02	O	Low	SDRAM address output 2
48	SDADRS01	O	Low	SDRAM address output 1
49	SDADRS00	O	Low	SDRAM address output 0
50	SDADRS10	O	Low	SDRAM address output 10
51	MODE3	I	Input	LSI mode set pin
52	SDBA	O	Low	SDRAM Bank select Address output Connect SDRAM-BANK pin when 16Mbit SDRAM using Connect SDRAM-BANK1 pin when 64Mbit SDRAM using
53	SDCSB	O	Low	SDRAM Chip Select output
54	SDRASB	O	Low	SDRAM Row Address Strobe output
55	SDCASB	O	Low	SDRAM Column Address Strobe output
56	SDWEB	O	Low	SDRAM Write Enable output
57	SDDQM	O	Low	SDRAM Data Mask Control output Common both for 16M/64Mbit-SDRAM : Connect this pin both to SDRAM-DQMH(UDQM) and DQML(LDQM) pins
58	SDDAT07	I/O	Input(Low)	SDRAM data 7
59	SDDAT06	I/O	Input(Low)	SDRAM data 6
60	SDDAT05	I/O	Input(Low)	SDRAM data 5
61	DVDD15	AO	High	Capacitor connection pin for internal regulator
62	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
63	DVDD	–	–	Digital system power supply
64	SDDAT04	I/O	Input(Low)	SDRAM data 4
65	SDDAT03	I/O	Input(Low)	SDRAM data 3
66	SDDAT02	I/O	Input(Low)	SDRAM data 2
67	SDDAT01	I/O	Input(Low)	SDRAM data 1
68	SDDAT00	I/O	Input(Low)	SDRAM data 0
69	SDADRS11	I/O	Input(Low)	Connect to SDRAM ADRS11 pin when using 64M bit SDRAM. SDRAM address output 11 CONT06 is available when using 16M bit SDRAM. General purpose I/O port with pull down resistor
70	SDADRS12	I/O	Input(Low)	Connect to SDRAM BANK0 pin when using 64M bit SDRAM. SDRAM address output 12 CONT07 is available when using 16M bit SDRAM. General purpose I/O port with pull down resistor
71	XVSS	–	–	Oscillator ground. This pin must be connected to the 0V level.
72	XOUT	O	Oscillation	16.9344MHz oscillator connection
73	XIN	I	Oscillation	16.9344MHz oscillator connection
74	XVDD	–	–	Oscillator power supply
75	DVDD	–	–	Digital system power supply

Pin No.	Pin name	I/O	State when "Reset"	Function
76	CONT08	I/O	Input	General purpose I/O port with LR clock output for CD data LR clock input for CD data (exclusive with CONT00) Data request signal input for CDTEXT interface (exclusive with CONT00 and CONT03)
77	CONT09	I/O	Input	General purpose I/O port with pull down resistor Bit clock output for CD data Bit clock input for CD data (exclusive with CONT01) Clock input/output for CDTEXT interface (exclusive with CONT01 and CONT04)
78	CONT10	I/O	Input	General purpose I/O port with pull down resistor Data output for Digital Audio interface Digital audio output<S/PDIF> Serial data output for CDTEXT interface Watch Dog Timer state monitor output
79	DVSS	–	–	Digital system ground. This pin must be connected to the 0V level.
80	SLCO	AO	Undefined	Slice Level Control output
81	EFMIN	AI	Input	RF signal input
82	RFOUT	AO	Undefined	RF signal output
83	LPF	AO	Undefined	RF signal DC level detection low-pass filter capacitor connection
84	PHLPF	AO	Undefined	Defect detection low-pass filter capacitor connection
85	AIN	AI	Input	A signal input
86	CIN	AI	Input	C signal input
87	BIN	AI	Input	B signal input
88	DIN	AI	Input	D signal input
89	SLCISET	AI	Input	SLCO output current setting resistor connection
90	RFMON	AO	Undefined	IC internal analog signal monitor
91	VREF	AO	AVDD/2	Reference voltage output for RF
92	JITTC	AO	Undefined	Jitter detection capacitor connection
93	EIN	AI	Input	E signal input
94	FIN	AI	Input	F signal input
95	NC	–	–	NC Pin (Open)
96	TE	AO	Undefined	TE signal output
97	TEIN	AI	Input	TE signal input used for TES signal generation
98	LDD	AO	Undefined	Laser power control signal output
99	LDS	AI	Input	Laser power detection signal input
100	AVSS	–	–	Analog system ground. This pin must be connected to the 0V level.

<Notes>

(1) For Unused pins :

- The unused input pins must be connected to the GND(0V) level if there is no individual note in the above table.
- The unused output pins must be left open(No connection) if there is no individual note in the above table.
- The unused input/output pins must be connected to the GND(0V) or power supply pin for I/O block with internal pull down/up resistor OFF or be left open with internal pull down/up resistor ON when input pin mode or must be left open(No connection) when output pin mode if there is no individual note in the above table.
  When you connect an I/O pin which is an input pin without internal pull-down/up resistor at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

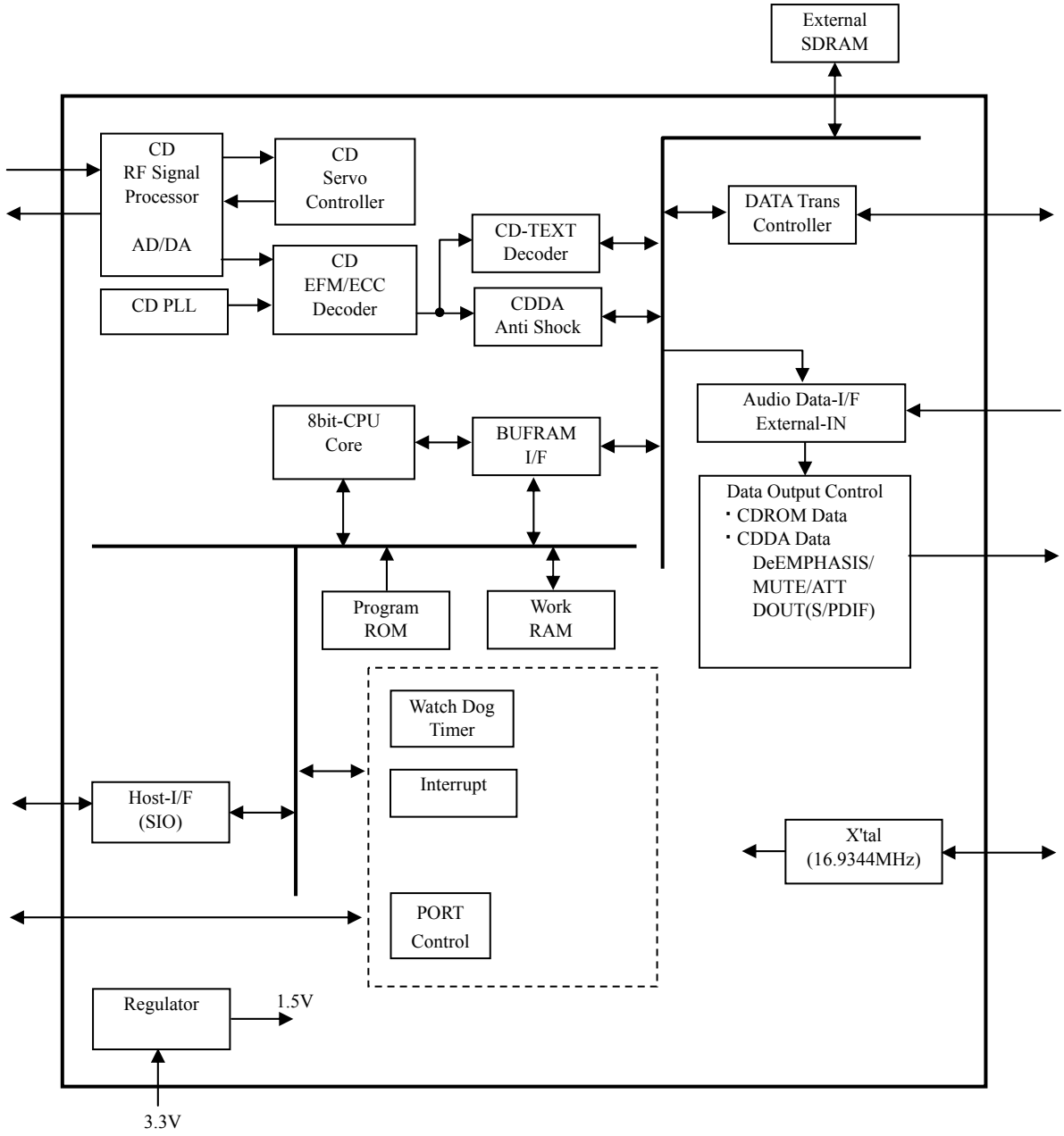
(2) For Power supply pins :

- Same voltage level must be supplied to DVDD, AVDD, XVDD and VVDD1 power supply pins.

(3) For "Reset" condition :

- This IC is not reset only by making the RESB pin "Low".
  Refer to "4. Power on and Reset control" for detail of "Reset" condition.

Block Diagram

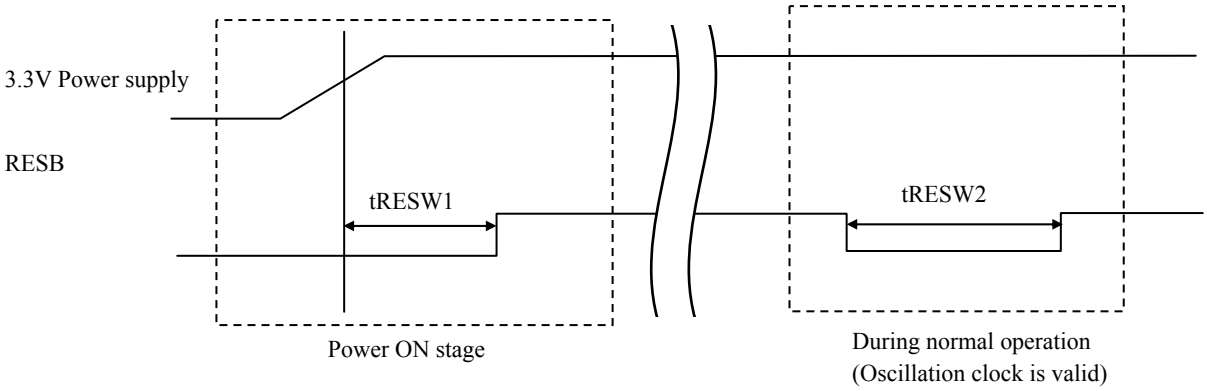


Power on and Reset control

Attention when power on

The RESB pin must be set to “Low” level when power is first supplied. At that time, it is necessary to input a stable clock to the XIN pin.

You may input the voltage of V_{DD} or less to each input terminal when the power supply is off.



Parameter	Symbol	Min	Typ	Max	Unit
Reset time(Power on)	tRESW1	20			ms
Reset time(Normal) (*1)	tRESW2	1			ms

*1 : The oscillation must be stable during tRESW2.

When the XIN clock has been stopped by the command etc. , the specification of tRESW2 could be larger than the value shown above, because it takes time that the XIN oscillator becomes stable.

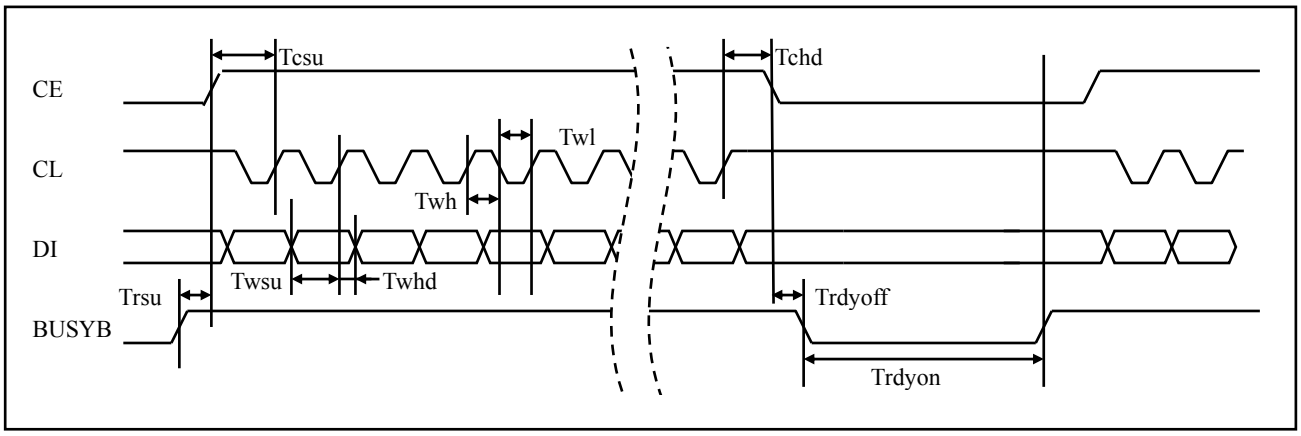
Host interface

The four wires serial interface is available as the data transmission protocol between this LSI and Host controller. It is able to know whether the internal sequencer could receive the command or not by the BUSYB pin.

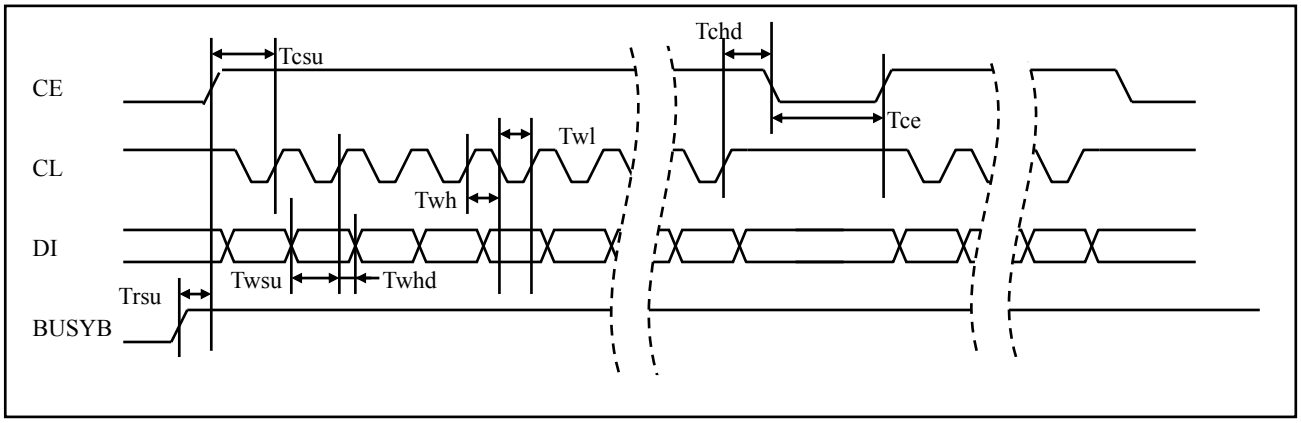
BUSYB	Command Acceptance situation
Low	All address command access disable
High	All address command access disable except A0h to A7h addresses BUSYB becomes Low if the A5h address command is transmitted. All address command except A0h to A7h addresses will be ignored.

By setting REG_READY command to High, internal register open mode is available. In this mode, Host controller can access to the all address command (internal sequencer can't control the CDDSP block). When the A5h address command is transmitted, REG_READY command and BUSYB pin is set to Low, and internal register open mode become finish.

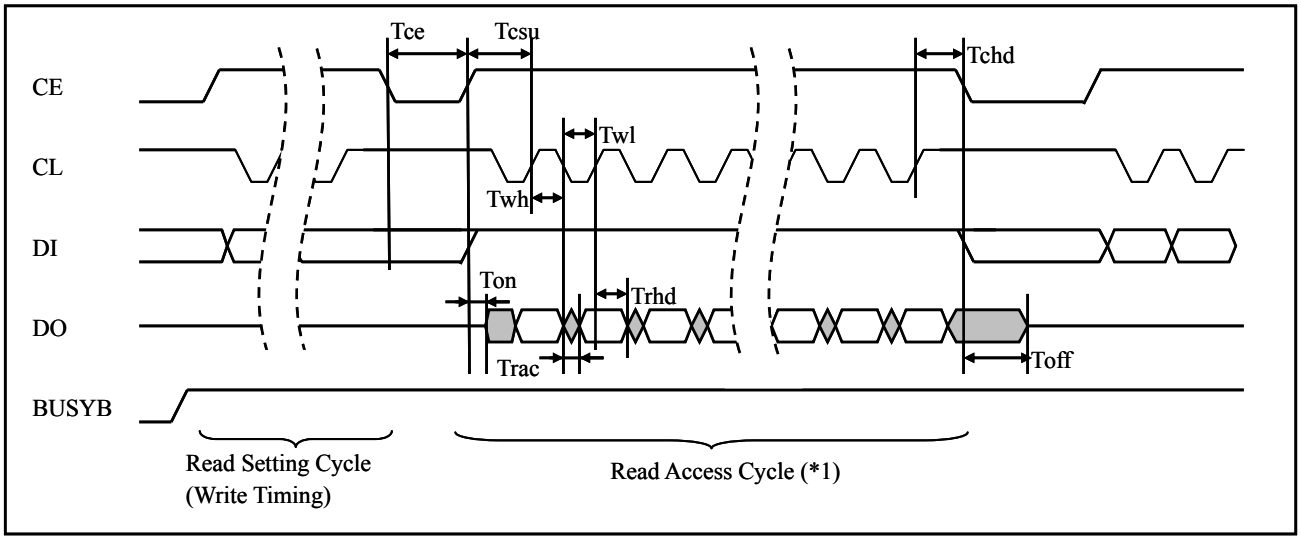
・Command Transfer Timing 1 : (Normal mode: BUSYB = "H" → "L")



・Command Transfer Timing 2 : (Internal register open mode: BUSYB = "H")

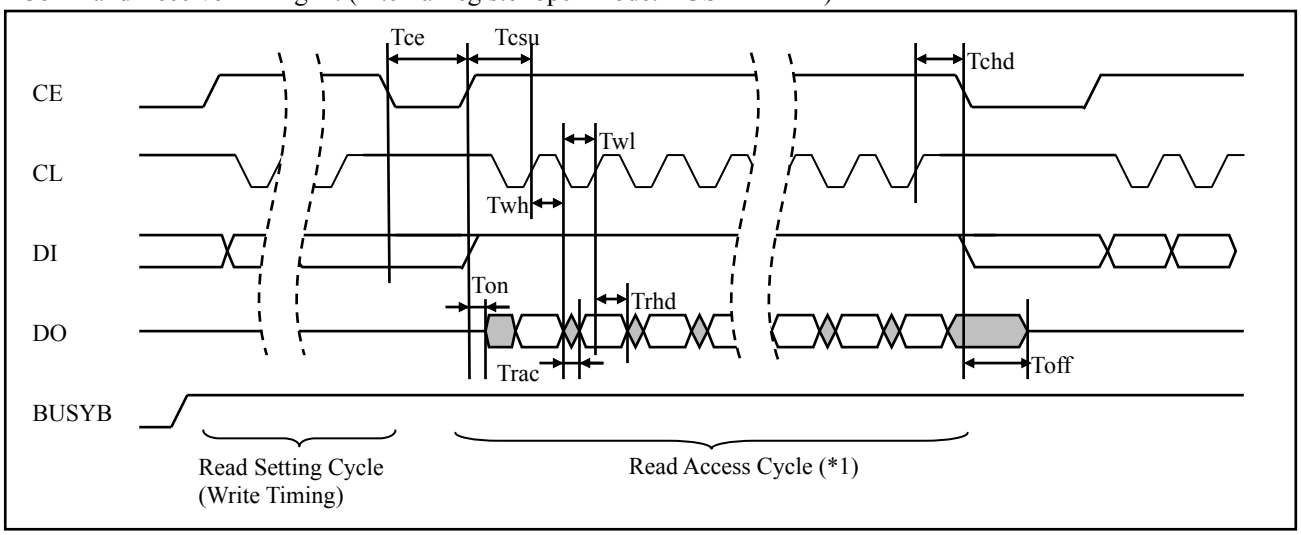


・Command Receive Timing 1 : (Normal mode : BUSYB = "H")



*1. High level must be supplied to the DI pin during Read Access Cycle.

・Command Receive Timing 2 : (Internal register open mode: BUSYB = "H")



*1. High level must be supplied to the DI pin during Read Access Cycle.

Parameter	Symbol	Pin Names	Min	Typ	Max	Unit
Setup time for READY	Trsu	CE, BUSYB	60			ns
Setup time for CE	Tcsu	CE, CL	400			
Hold time for CE	Tchd	CE, CL	200			
Setup time for DI	Twsu	DI, CL	100			
Hold time for DI	Twhd	DI, CL	100			
High level clock pulse width	Twh	CL	200			
Low level clock pulse width	Twl	CL	200			
Access time for read data	Trac	CL, DO	0		100	
Hold time for read data	Trhd	CL, DO	120			
Turn On Time for DO	Ton	CE, DO	150			
Turn Off Time for DO	Toff	CE, DO	0		300	
Command transfer time	Tce	CE	1			µs
Turn Off Time for READY	Trdyoff	CE, BUSYB	0		200	ns
Turn On Time for READY(*1)	Trdyon	CE, BUSYB	0.175		50000	µs

*1. Never communicate in this period.

CD data output function

Two modes can be available for CD data output.

(1) Normal mode
In this mode, output signals are LRCK, BCK and DATA. CLV or Jitter-Free(VCEC) playback is supported.
When CDDA playback, depending on the specification of Audio DAC, FS384 clock output is also available .

(2) Slave mode
In ths mode, output signal is DATA, and input signals are LRCK, BCK. The DATA output is synchronized to input clocks (LRCK,BCK).
It is enable to output CD data synchronized to Audio DAC without connecting FS384clock.
This mode is only available for CD normal playback, and LRCK frequency must be 44.1kHz.

1. Normal mode

・Available format

Mode : IIS, MSB First Right-Justified, MSB First Left-Justified
Slot Length : 32fs, 48fs
Data Length : 16-bit

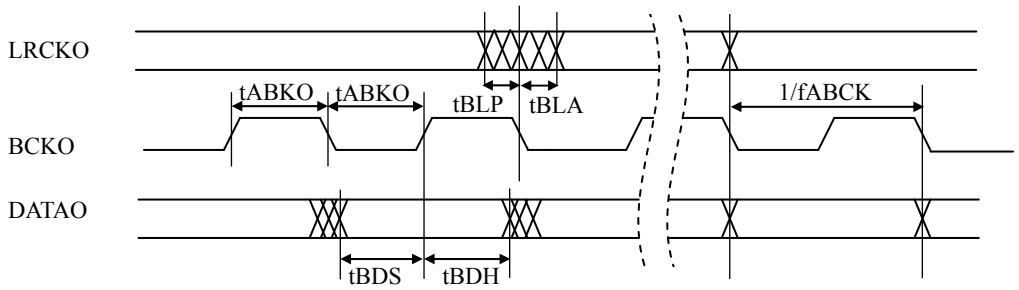
・Used Pin

LRCKO : CONT00, CONT08
BCKO : CONT01, CONT09
DATAO : CONT02, CONT10

・Note

When CDDA Playback, FS384 can be optionally output from CONT04 or CONT05. The signal input from XIN pin is output as FS384 signal.

・CD Data output timing



Parameter	Symbol	Pin Names	Min	Typ	Max	unit
Bit clock Frequency	fABCKO	BCKO			10.5	MHz
Bit clock "H" level width	tABKOH	BCKO	47.5			ns
Bit clock "L" level width	tABKOL	BCKO	47.5			ns
Setup time for LRCK (based on BCK negedge)	tBLP	BCKO, LRCKO	0		15	ns
Hold time for LRCK (based on BCK negedge)	tBLA	BCKO, LRCKO	0		15	ns
Setup time for DATA output	tBDS	BCKO, DATAO	30			ns
Hold time for DATA output	tBDH	BCKO, DATAO	30			ns

* In case of quadruple speed playback, and setting the output format as 48fs slot length.

2. Slave mode

In this mode, LRCK (Fs=44.1kHz) and BCK are input from external device, and output data is synchronized with input clocks. So, it is possible to play CDDA without FS384 or SRC (Sampling Rate Converter).

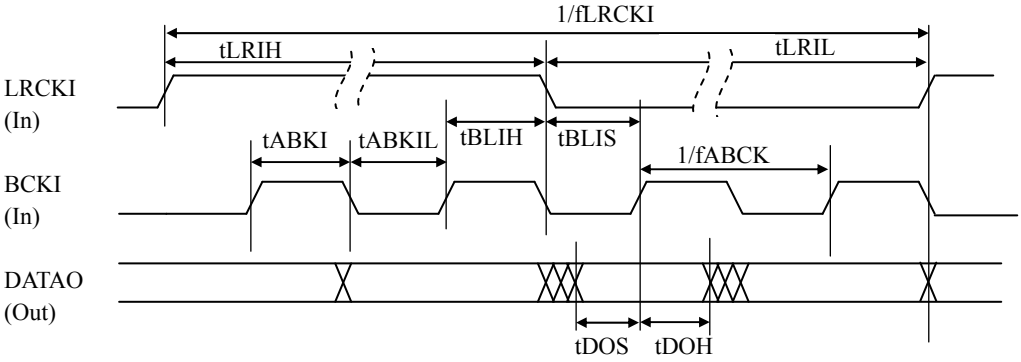
・Available format

Mode : IIS, MSB First Right-Justified, MSB First Left-Justified
Slot Length : 32fs, 48fs, 64fs
Data Length : 16-bit

・Used Pin

LRCKI : CONT00, CONT08
BCKI : CONT01, CONT09
DATAO : CONT02, CONT10

・Slave mode data timing



Parameter	Symbol	Pin Names	Min	Typ	Max	unit
LRCK frequency	fLRCKI	LRCKI		44.1	48.5	kHz
LRCK "H" level width	tLRIH	LRCKI	10.3	11.34		µs
LRCK "L" level width	tLRIL	LRCKI	10.3	11.34		µs
Bit clock frequency	fABCKI	BCKI		2.1168 *1	3.10	MHz
Bit clock "H" level width	tABKIH	BCKI	160	236.2 *1		ns
Bit clock "L" level width	tABKIL	BCKI	160	236.2 *1		ns
Setup time for LRCK input	tBRIS	LRCKI, BCKI	50			ns
Hold time for LRCK input	tBLIH	LRCKI, BCKI	50			ns
Setup time for DATA output	tDOS	DATAO, BCKI	50			ns
Hold time for DATA output	tDOH	DATAO, BCKI	50			ns

*1: In case of setting the output format as 48fs slot length.

CD Subcode Data Output function

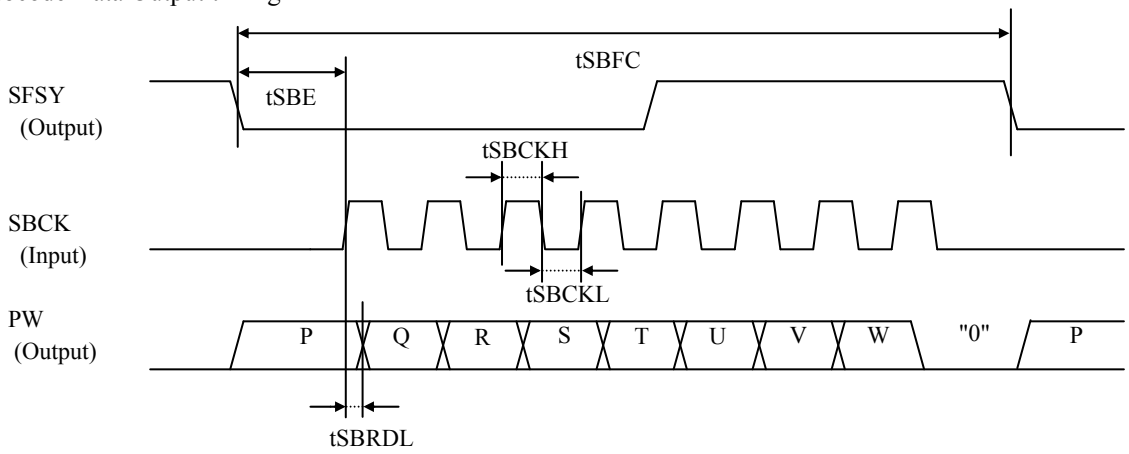
It is possible to output the subcode data (PW data) according to the terminal setting when CD playback mode.
The PW data are output at the rising edge of SBCK signal when the SBCK clock signal is input.

<Note>
The CD-TEXT function and the CD Subcode data output function are exclusive functions. It is impossible to use those two functions simultaneously.

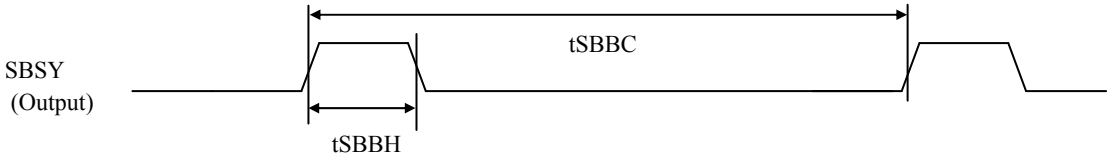
・Used pins

SBSY (Subcode Block Synchronous signal) : CONT00
SFSY (Subcode Frame Synchronous signal) : CONT01
PW (Subcode PW data) : CONT02
SBCK (Subcode data read clock) : CONT03

・Subcode Data Output timing



・Subcode Block Synchronous Signal Output timing



Parameter	Symbol	Pin Names	Min	Typ	Max	unit
Subcode Read Cycle time	tSBFC	SFSY		136 *1		us
Subcode Read Enable time	tSBE	SFSY, SBCK	400			ns
SBCK clock "H" level width	tSBCKH	SBCK	250			ns
SBCK clock "L" level width	tSBCKL	SBCK	250			ns
PW data output Delay time	tSBRDL	SBCK, PW	0		100	ns
SBSY output Cycle time	tSBBC	SBSY		13.3 *2		ms
SBSY "H" level width	tSBBH	SBSY		272 *2		us

<Notes>
*1. When playback the CD at the normal speed (CLV playback).
This value changes depending on the playback speed.
*2. When playback the CD at the normal speed (CLV playback).
The SBSY signal becomes high level during the first two subcoding symbols (S0 and S1) are asserted.

CDTEXT data output function

CDTEXT data are decoded and buffered to external SDRAM.
There are two methods to output CDTEXT data from theSDRAM.

(1) Command Communication output mode
Outputs the CDTEXT data using the command communication protocol between this IC and external host controller.

(2) Hand shake output mode using with hardware interface function

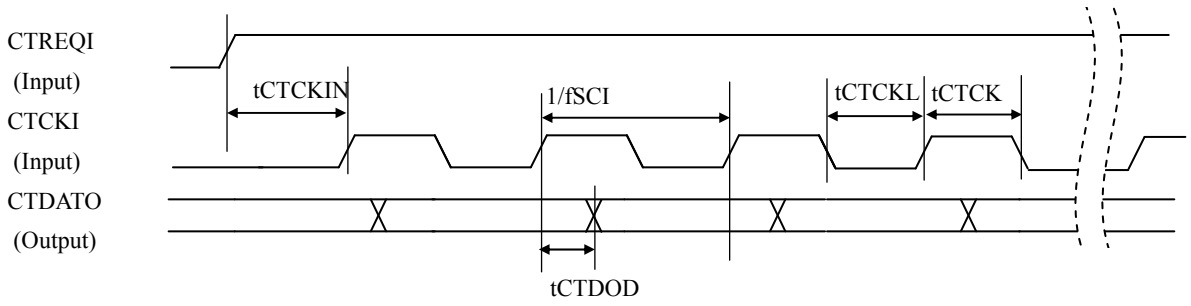
A. Inputs data request signal and transfer clock then outputs CDTEXT data
The CDTEXT data(CTDATO) will be output synchronizing with the CTCKI clock when the CTCKI clock is input after the CDTEXT data request signal is input(CTREQI="H").

B. Inputs data request signal then outputs transfer clock and CDTEXT data
The CTCKO and CTDATO synchronized with CTCKO will be output after the CDTEXT data request signal is input (CTREQI= "H").

In both operation modes (1) and (2), the data transfer unit bit length is 2 Bytes (16 bits).

* The CDTEXT function and CD subcode data output function are exclusive each other, and then those functions can not be used simultaneously.

・CDTEXT data output Timing 1 : CTCK input mode



<Supplement>
Both modes below are available.

A. CTCKI="L" start mode
The CTDATO is output synchronized with the rising edge of the CTCKI clock.
The host controller should latch the CTDATO data at the falling edge of the CTCKI clock.

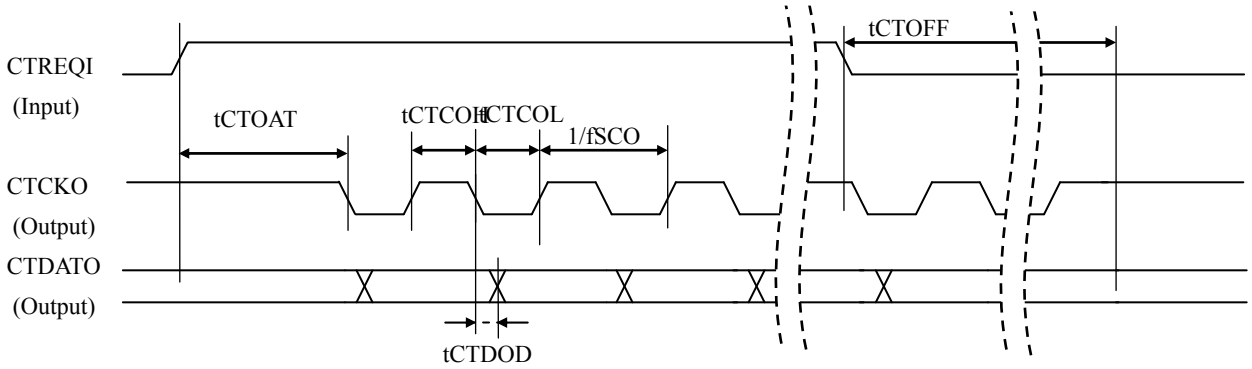
B. CTCKI="H" start mode
The CTDATO is output synchronized with the falling edge of the CTCKI clock.
The host controller should latch the CTDATO data at the rising edge of the CTCKI clock.

* The relationship between the signals in figure 8-1 and the pins is shown below.
CTREQI : CONT00, CONT03, CONT08
CTCKI : CONT01, CONT04, CONT09
CTDATO :CONT02, CONT05, CONT10

Parameter	Symbol	Pin Names	Min	Typ	Max	unit
CTCKI clock Frequency	fSCI	CTCKI			1.25	MHz
CTCKI clock input start time	tCTCKIN	CTREQI, CTCKI	1000			ns
CTCKI clock "H" level width	tCTCKH	CTCKI	400			ns
CTCKI clock "L" level width	tCTCKL	CTCKI	400			ns
CTDATO output Delay time	tCTDODL1	CTCKI, CTDATO			250	ns

Note : The above figure shows the case of mode A that the clock starts low level (CTCKI="L").
The timings are same when the clock starts high level (CTCKI="H").

・CDTEXT data output Timing 2 : CTCK output mod



<Supplement>

The CTCKO will be output starting with the high level then the CTDATO will be output synchronized with the falling edge of the CTCKO clock.

The host controller should latch the CTDATO data at the rising edge of the CTCKO clock.

* The relationship between the signals in figure 8-2 and the pins is shown below.

CTREQI : CONT00, CONT03, CONT08

CTCKO : CONT01, CONT04, CONT09

CTDATO : CONT02, CONT05, CONT10

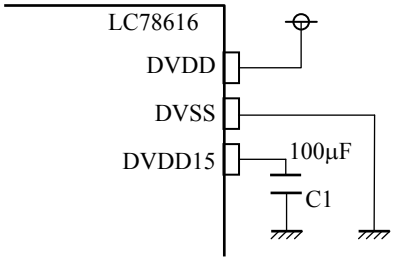
Parameter	Symbol	Pin Names	Min	Typ	Max	unit
CTCKO clock Frequency	fSCO	CTCKO	1.05		4.2	MHz
CDTEXT data output start time	tCTOAT	CTREQI, CTCKO			(1/fSCO) ×32	ns
CDTEXT data output stop time	tCTOFF	CTREQI, CTCKO			(1/fSCO) ×32	ns
CTCKO clock "H" level width	tCTCOH	CTCKO	400		100	ns
CTCKO clock "L" level width	tCTCOL	CTCKO	400		100	ns
CTDATO output Delay time	tCTDODL2	CTDATO, CTCKO	0		50	ns

Internal Voltage Regulator

at Ta=–40°C to 85°C, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage	DVDD15	V_{DD}=3.0 to 3.6V	1.35	1.50	1.65	V
Load current	Iope	V_{DD}=3.3V			50	mA

・Example circuit for Regulator



* Same circuit need to be mounted both for two regulator pins. (No.28 and No.61)

* C1 is the capacitor to avoid oscillation. This capacitor value must be low ESR and greater than 30µF in the range of the operating temperature. Because there is a possibility of the oscillation when the capacity value changes by the temperature change etc. (The recommended value is 100µF.)

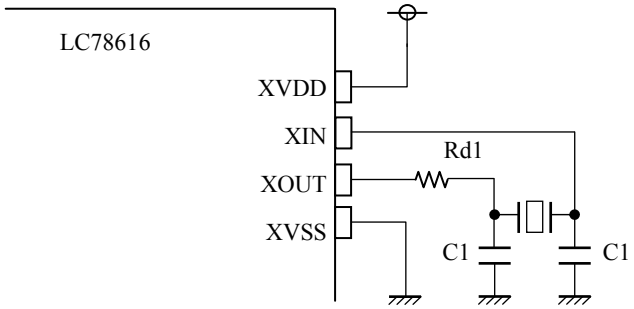
A/D, D/A converter Characteristics for servo

at Ta=–40°C to 85°C, V_{DD}=3.3V, DV_{SS}=AV_{SS}=XV_{SS}=VV_{SS}1=0V

Parameter	Symbol	Min	Typ	Max	Unit
Resolution	Res		8		bit
Maximum input/output range	Vaio1		4/5×V_{DD}		V
Minimum input/output range	Vaio2		1/5× V_{DD}		V

Oscillator

・Example circuit for Oscillator



XIN/XOUT : 16.9344MHz

・For System clock of internal micro controller, CD control and Audio control

・Recommended Oscillators

Murata Manufacturing Co., Ltd.

SMD	: CSTCE16M9V53-R0	<Built-in C>
	: CSTCW16M9X51008-R0	<Built-in C>
Lead	: CSTLS16M9X53-B0	<Built-in C>

<Notes>

・Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.

・Concerning about internal circuit for XIN/XOUT, refer to the "Analog Pin Internal Equivalent Circuits" section.

The XIN pin can also be supplied from an external clock instead of connecting the oscillator. In this case, XOUT pin must be left open.

SDRAM Interface

(1) Required specification for external SDRAM

Memory size : 16M-bit or 64M-bit
Data width : 16-bit
CAS latency : 2
Burst length : Full

(2) Interface pins to external SDRAM

Pin Name	Function at 16M-bit SDRAM	Function at 64M-bit SDRAM	Signal name in Figure 12-1, 2, 3
SDDAT15 to SDDAT00	Data Input/Output (16-bit)	Data Input/Output (16-bit)	DDAT[15:0] DDAT[15:0]
SDADRS10 to SDADRS00	Address Output (11-bit)	Address Output (11-bit)	DADD[10:0] DADD[10:0]
SDADRS11	Not used *1	Address(A11) Output	– DADD[11]
SDADRS12	Not used *2	Address(A12) or Bank0 Output	– DADD[12]
SDBA	Bank Output	Bank or Bank1 Output	DADD[11] DADD[13]
SDDQM	DQMH/DQML (UDQM/LDQM) Output *3	DQMH/DQML (UDQM/LDQM) Output *3	SDDQM SDDQM
SDCSB	CSB Output	CSB Output	SDCSB SDCSB
SDRASB	RASB Output	RASB Output	SDRASB SDRASB
SDCASB	CASB Output	CASB Output	SDCASB SDCASB
SDWEB	WEB Output	WEB Output	SDWEB SDWEB
SDCKE	Clock Enable Output	Clock Enable Output	SDCKE SDCKE
SDCLK	Clock Output	Clock Output	SDCLK SDCLK

<Notes>

*1. SDADRS11 in 16M-bit SDRAM using mode can be used as CONT06 pin.

*2. SDADRS12 in 16M-bit SDRAM using mode can be used as CONT07 pin.

*3. The SDRAM access data width of this IC is sixteen bits. Therefore, connect the SDDQM of this IC to both the DQMH(UDQM) and DQML(LDQM) pins of SDRAM.

*4. The all pins used for SDRAM interface are input pin mode and internal pull down resistor on mode in initial condition after reset of this IC. All the resistors will be off when the SDRAM use mode is set to be ON.

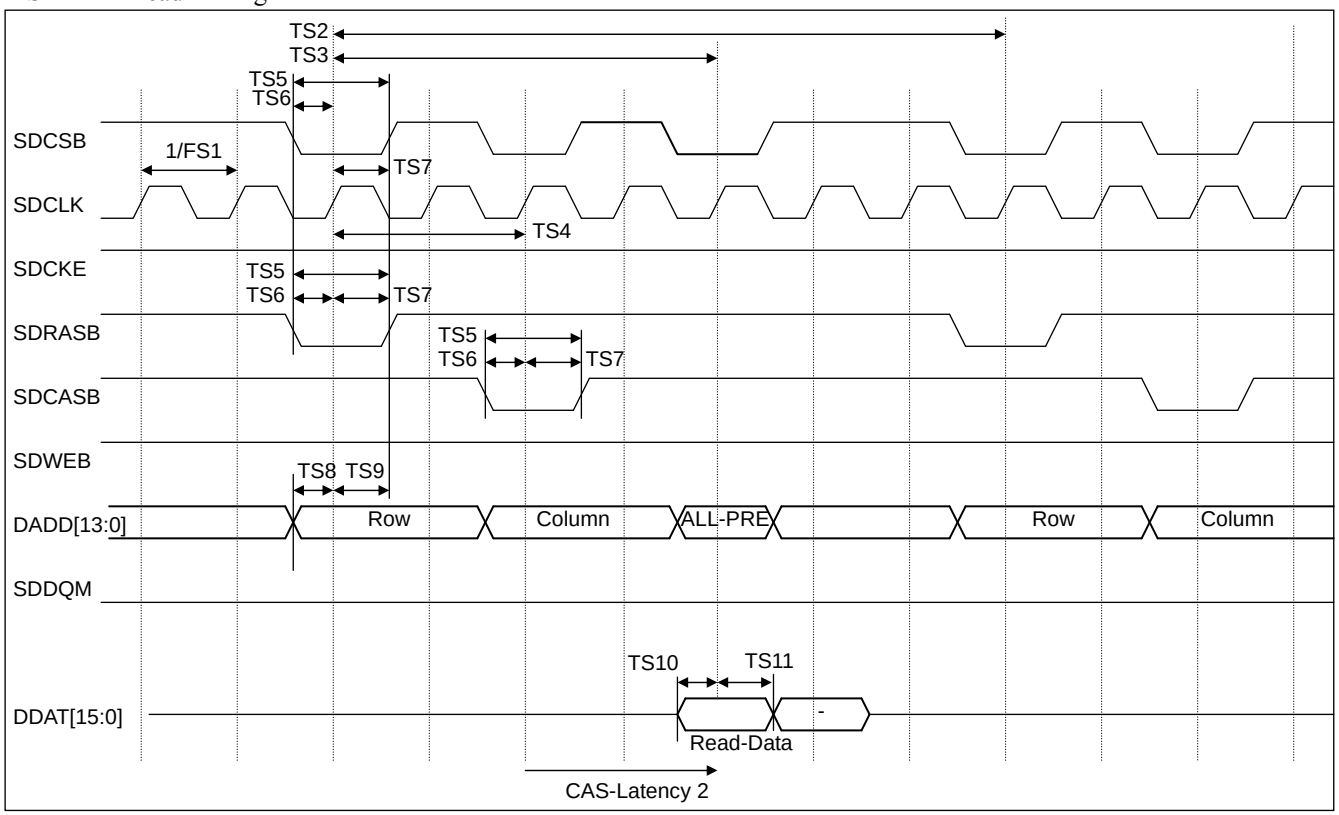
*5. Some signals used in Figure 12-1 to Figure 12-3 use different pins according to the using SDRAM. The signal name in Figure 12-1 to Figure 12-3 for the actual pin is shown at the most right column in above table.

Upper step : Signal name in 16M-bit SDRAM using mode

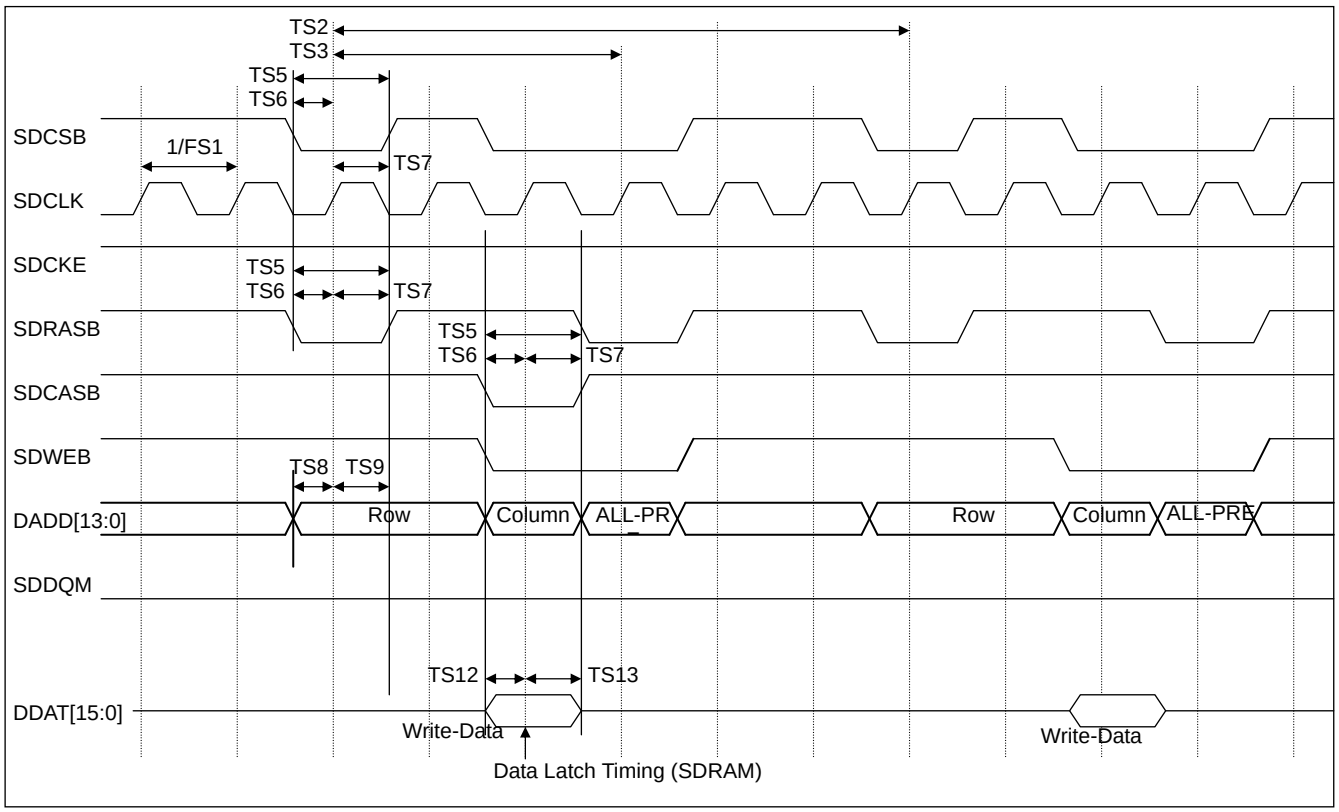
Lower step : Signal name in 64M-bit SDRAM using mode

(3) SDRAM Access Timing

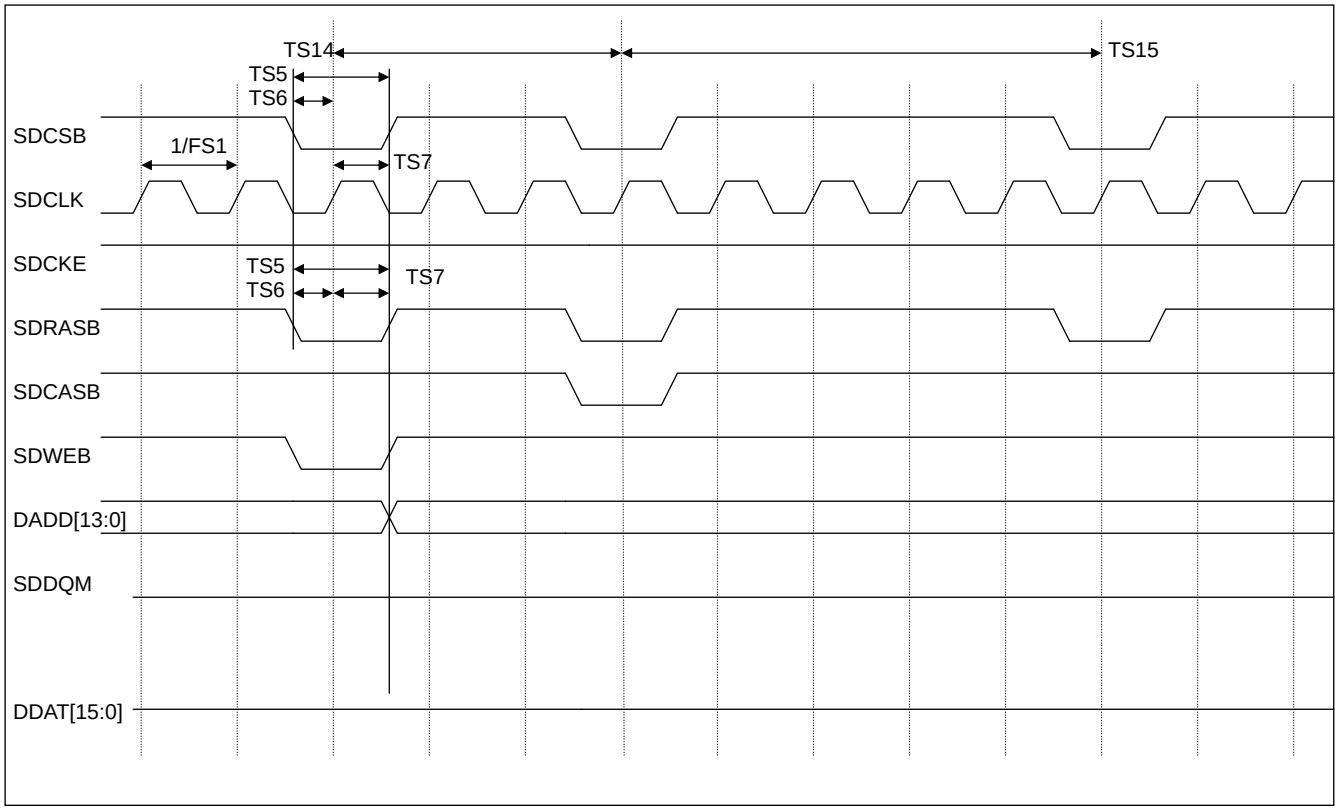
・SDRAM Read Timing



・SDRAM Write Timing



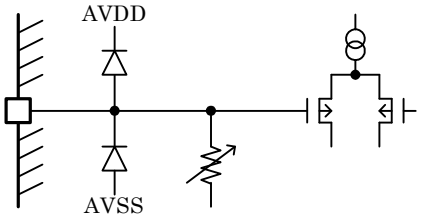
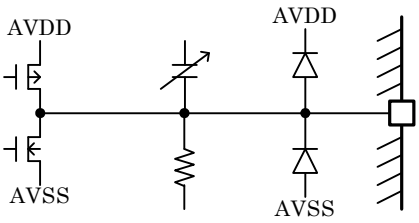
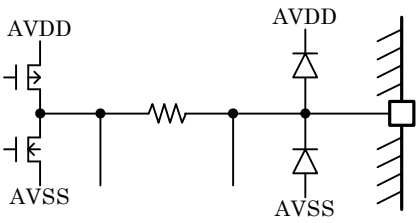
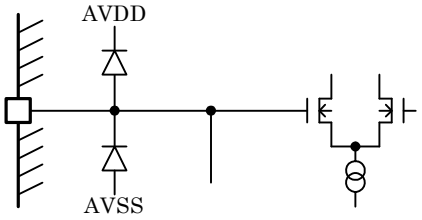
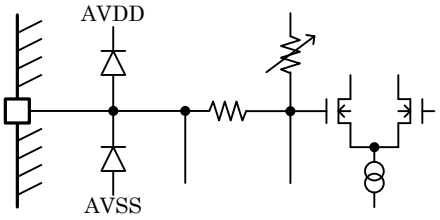
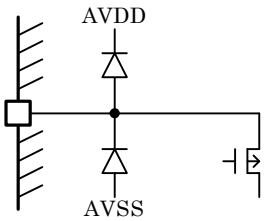
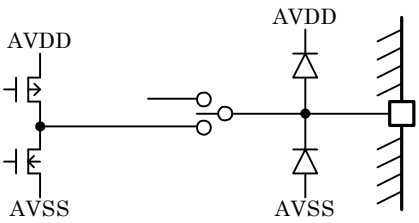
・SDRAM Refresh Timing (Auto Refresh)

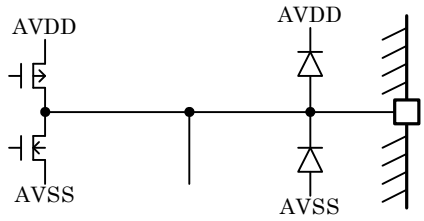
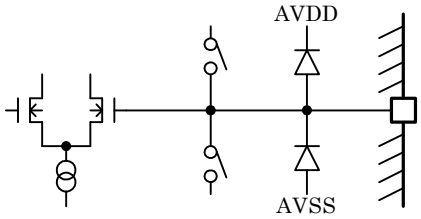
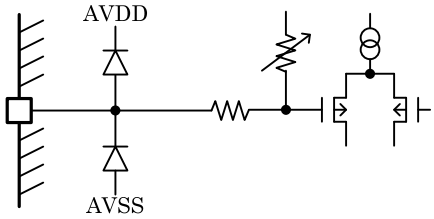
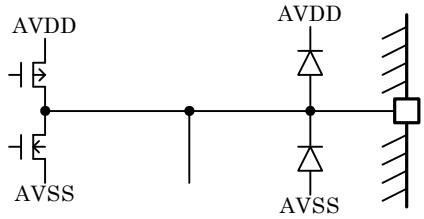
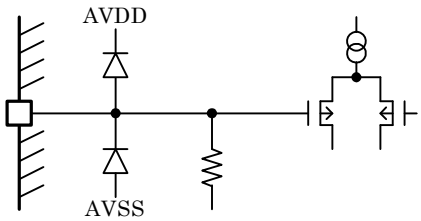
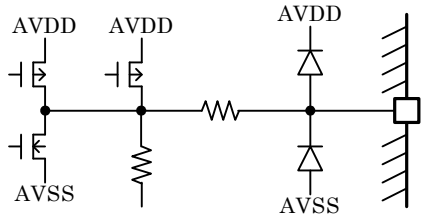
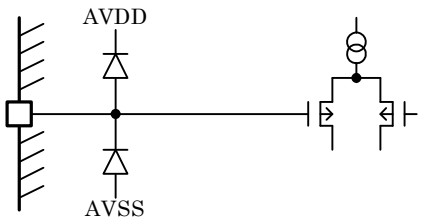


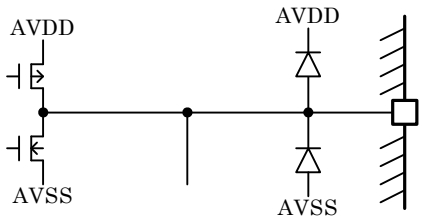
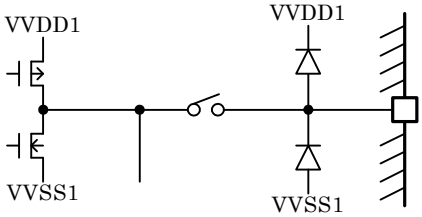
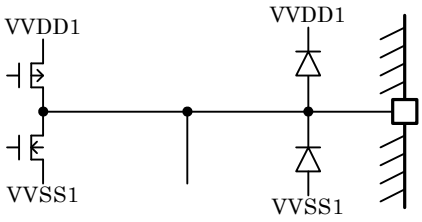
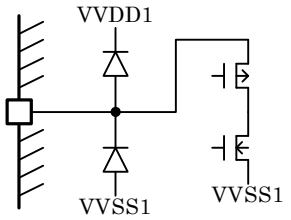
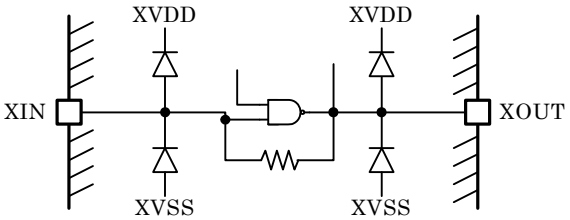
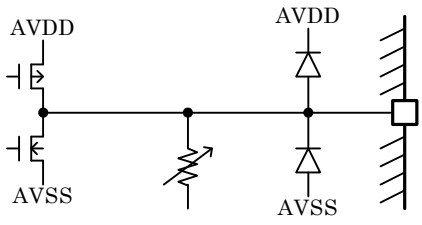
symbol	parameter	Min	typ	max	unit
FS1	SDRAM clock(SDCLK) Frequency		16.9344		MHz
TS2	Row(SDRASB) Cycle time	(1/FS1)×5	–	–	ns
TS3	Row(SDRASB) Active time	(1/FS1)×3	–	–	ns
TS4	RASB-CASB Delay time(SDRASB-SDCASB)	(1/FS1)×2	–	–	ns
TS5	Command "L" level width (SDCSB, SDCKE, SDRASB, SDCASB, SDWEB)	40	–	–	ns
TS6	Command Setup time (SDCSB, SDCKE, SDRASB, SDCASB, SDWEB, SDDQMU, SDDQML)	10	–	–	ns
TS7	Command Hold time (SDCSB, SDCKE, SDRASB, SDCASB, SDWEB, SDDQMU, SDDQML)	10	–	–	ns
TS8	Address(DADD) Setup time	10	–	–	ns
TS9	Address(DADD) Hold time	10	–	–	ns
TS10	SDRAM Read Data Setup time (Data read from SDRAM)	20	–	–	ns
TS11	SDRAM Read Data Hold time (Data read from SDRAM)	0	–	–	ns
TS12	SDRAM Write Data Hold time before rising edge of SDCLK (Data write to SDRAM)	10	–	–	ns
TS13	SDRAM Write Data Hold time after rising edge of SDCLK (Data write to SDRAM)	10	–	–	ns
TS14	Row(SDRASB) Pre-charge time	(1/FS1)×3	–	–	ns
TS15	Row(SDRASB) Active time after Refresh	(1/FS1)×5	–	–	ns

<Notes>
・Setup time and Hold time specifications in above table are measured from the rising edge of SDCLK signal.
・All the specifications in above table are applied to Read mode, Write mode and Refresh mode.

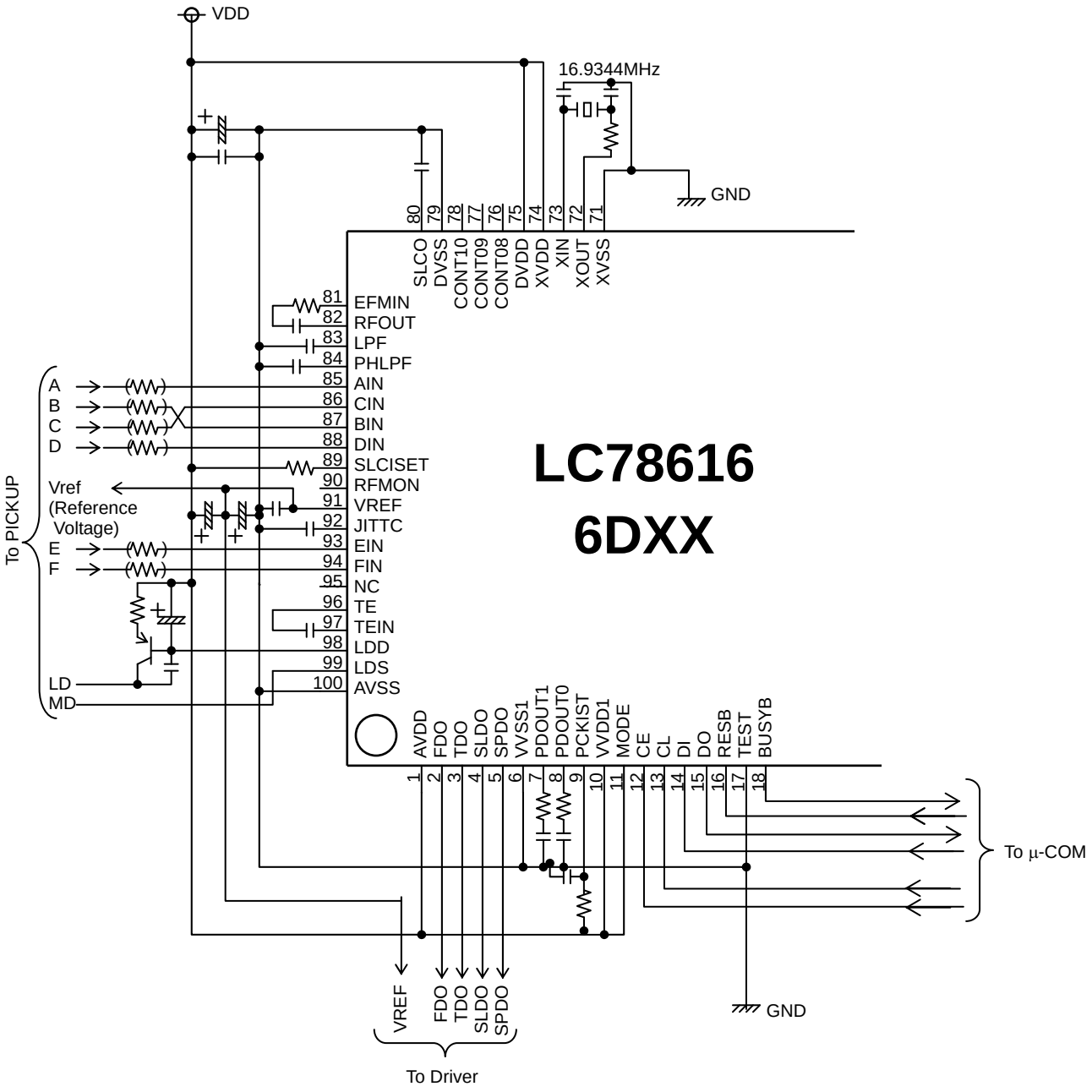
Analog Pin Internal Equivalent Circuits

Pin Name(Pin No.)	Equivalent Circuit
EFMIN (81)	
RFOUT (82)	
LPF (83)	
PHLPF (84)	
AIN (85) CIN (86) BIN (87) DIN (88)	
SLCISET (89)	
RFMON (90)	

Pin Name(Pin No.)	Equivalent Circuit
VREF (91)	
JITTC (92)	
EIN (93) FIN (94)	
TE (96)	
TEIN (97)	
LDD (98)	
LDS (99)	

Pin Name(Pin No.)	Equivalent Circuit
FDO (2) TDO (3) SLDO (4) SPDO (5)	
PDOUT1 (7)	
PDOUT0 (8)	
PCKIST (9)	
XOUT(72) XIN(73)	
SLCO (80)	

Sample Application Circuit



* This sample circuit is only for CD servo block and each PLL block.
The value of each component needs to be adjusted under the target conditions.
The circuit for CD servo shown above could be changed depending on the CD mechanism used.