

**KS54AHCT 821/822**  
**KS74AHCT**

**10-Bit Bus Interface Flip-Flops**  
**with 3-State Outputs**

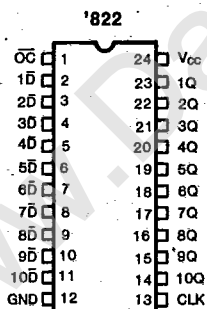
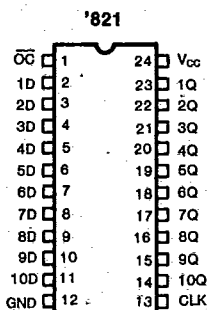
Preliminary Specifications

T-4607-05

**FEATURES**

- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**PIN CONFIGURATIONS**



**DESCRIPTION**

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLES**

(Each Flip-Flop)  
 '821

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
L	H	X	$Q_0$
H	X	X	Z

'822

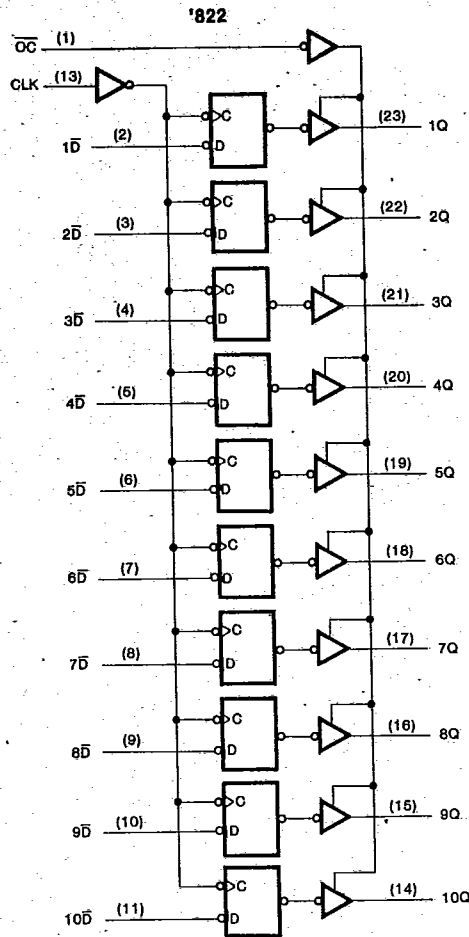
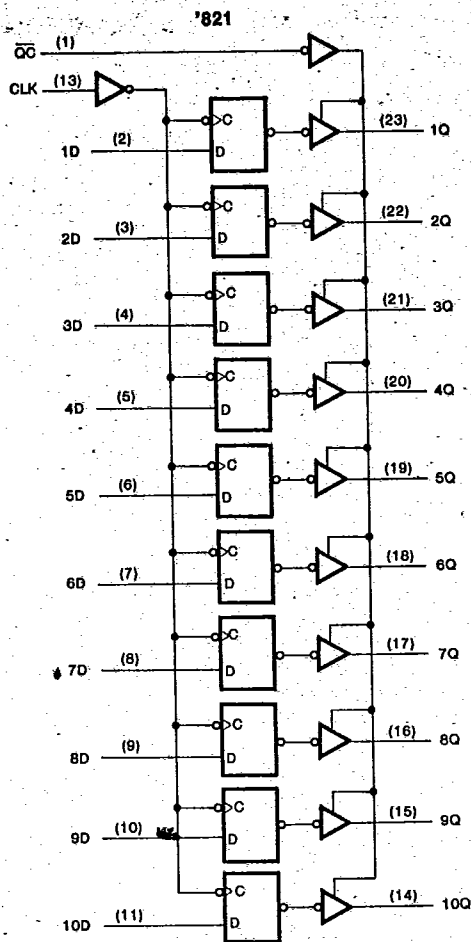
Inputs			Output
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	$Q_0$
L	H	X	$Q_0$
H	X	X	Z

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**LOGIC DIAGRAMS**



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**10-Bit Bus Interface Flip-Flops**  
**with 3-State Outputs T-46-07-05**

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable, $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

KS54AHCT 821/822  
KS74AHCT10-Bit Bus Interface Flip-Flops  
with 3-State Outputs T-46-07-05AC ELECTRICAL CHARACTERISTICS (Input  $t_r, t_f < 2$  ns), AHCT821, AHCT822

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit	
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	V <sub>CC</sub> = 5.0V ± 10%			
			Typ	Min	Max	Min	Max		
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	50	35		30			MHz
Propagation Delay CLK to any Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	8 11		14 19		17 23		ns
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	8 11		14 19		17 23		ns
Output Enable Time, OC to any Q	t <sub>pZL</sub>	R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 14		18 23		22 28		ns
	t <sub>pZL</sub>		11 14		18 23		22 28		ns
Output Disable Time, OC to any Q	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	13		18		22		ns
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	13		18		22		ns
Pulse Width, CLK High or Low	t <sub>w</sub>		9	15		18			ns
Setup Time, Data before CLK†	t <sub>su</sub>		9	14		17			ns
Hold Time, Data after CLK†	t <sub>h</sub>		-3	0		0			ns
Input Capacitance	C <sub>IN</sub>		5						pF
Output Capacitance	C <sub>OUT</sub>	Output Disabled	10						pF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC = V <sub>CC</sub>	5						pF
		OC = GND	30						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

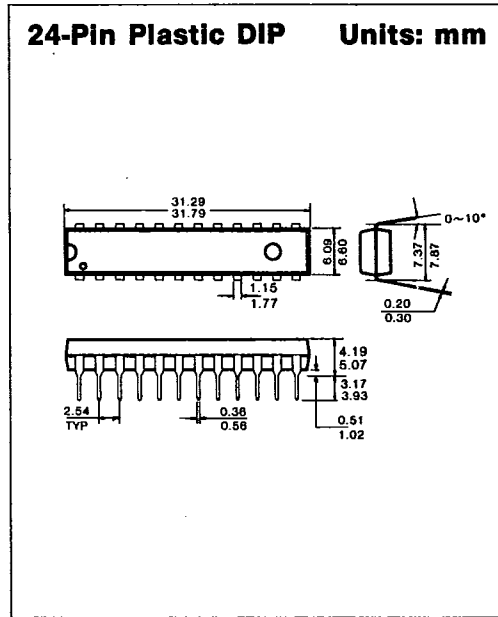
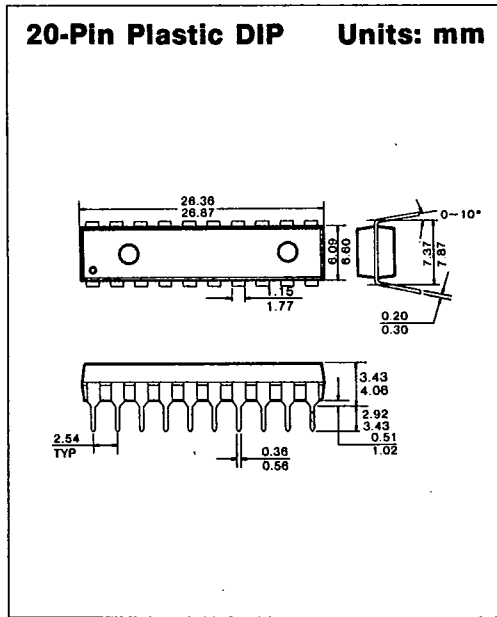
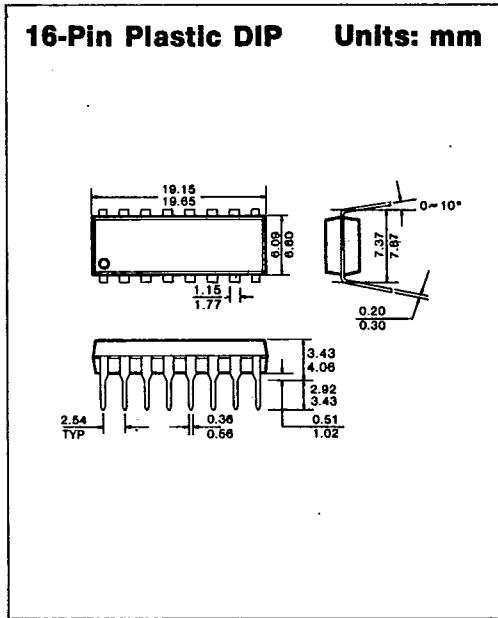
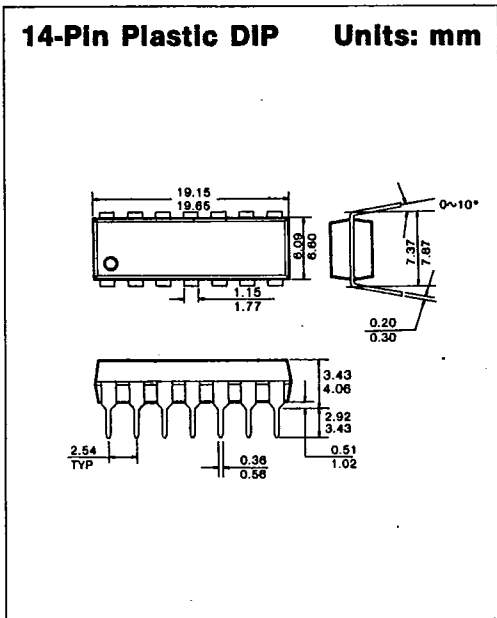
† For AC switching test circuits and timing waveforms see section 2.



**PACKAGE DIMENSIONS**

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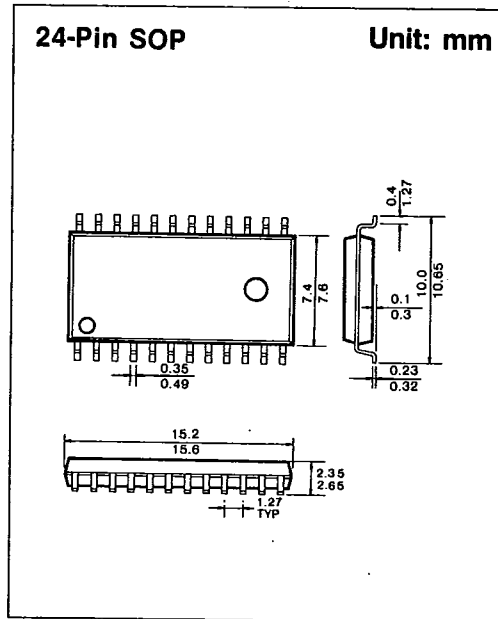
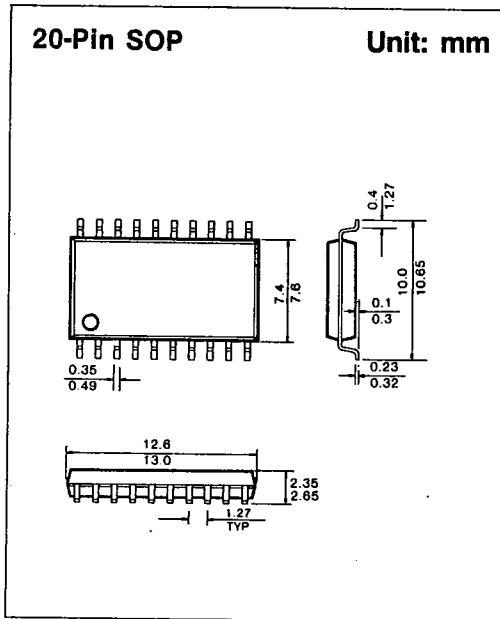
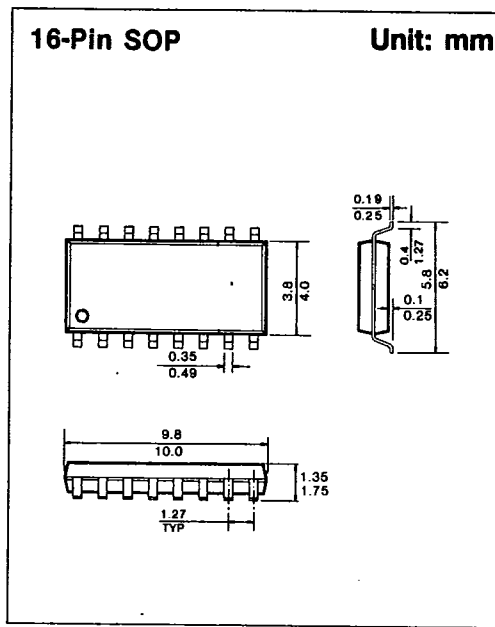
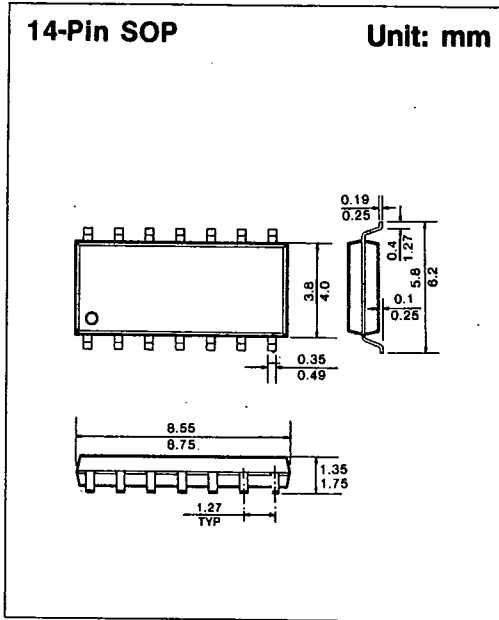
**1. PLASTIC PACKAGES**



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**PACKAGE DIMENSIONS**

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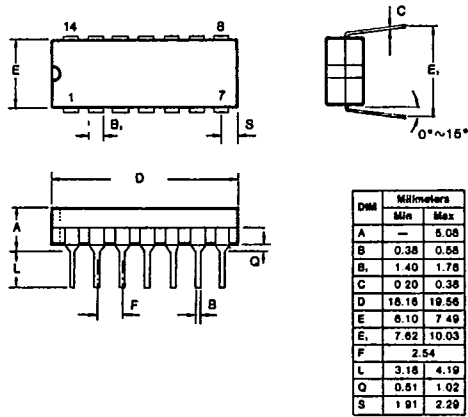


**PACKAGE DIMENSIONS**

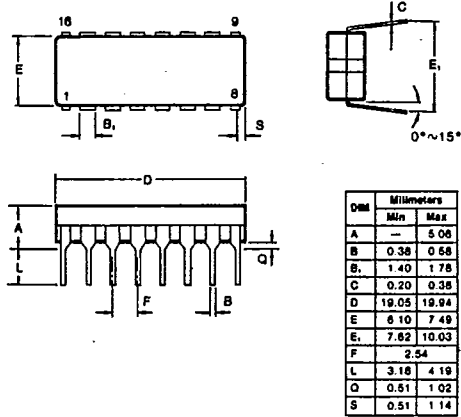
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**2. CERAMIC PACKAGES**

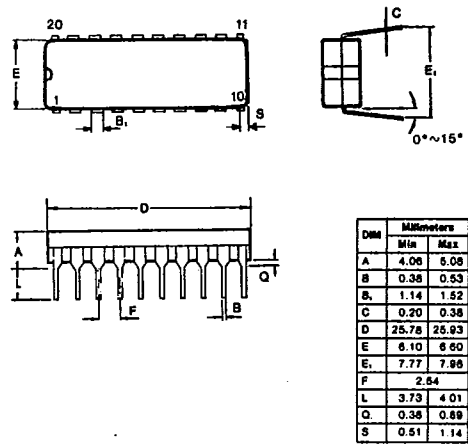
**14-Pin Ceramic DIP Units: mm**



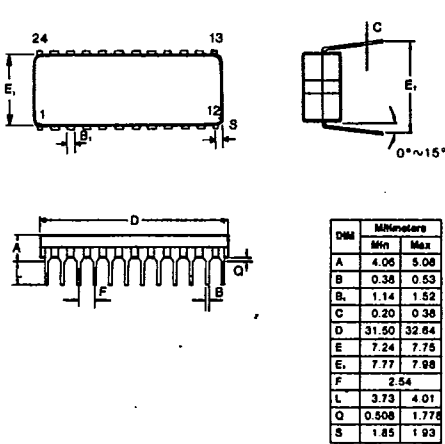
**16-Pin Ceramic DIP Units: mm**



**20-Pin Ceramic DIP Units: mm**



**24-Pin Ceramic DIP Units: mm**



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