EUP8060X

EUTECH MICROELECTRONICS

1A Li-Ion/Polymer Charger IC with Thermal Regulation and OVP

DESCRIPTION

The EUP8060X series are highly integrated single cell Li-Ion/Polymer battery charger IC designed for handheld devices. The EUP8060X integrates internal power FET, current sensor, charge status, reverse current protection and overvoltage protection (OVP) in a single monolithic devices. When AC-adapter is applied, an external resistor sets the magnitude of the charge current, which may be programmed up to 1A. Thermal feedback also regulates the charge current to limit the die temperature when fast charging or while exposed to high ambient temperature.

The EUP8060X charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety for charge termination. The EUP8060X can operate in an LDO mode which is used primary during system level testing of the handset to eliminate the need for battery insertion. The EUP8060X automatically re-starts the charge if the battery voltage falls below an internal threshold. The EUP8060X also automatically enters sleep mode when DC supplies are removed. No external sense resistor or blocking diode is required for charging.

FEATURES

- Programmable Charge Current up to 1A
- ±1% Voltage Regulation Accuracy
- Thermal Regulation to Maximize Charge Rate
- Input Overvoltage Protection: 6.6V and 11V Options
- Charge Termination by Minimum Current and Time
- Precharge Conditioning with Safety Timer
- Status Outputs to Indicate Charge, Fault, and Power good Outputs
- Reverse Leakage Protection Prevents Battery Drainage
- Short-Circuit and Thermal Protection
- Automatic Sleep Mode for Low Power Consumption
- LDO Mode Operation for System Level Testing without Battery Insertion
- 3mm×3mm TDFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Mobile Phone, PDA, MP3 Players, Digital Cameras
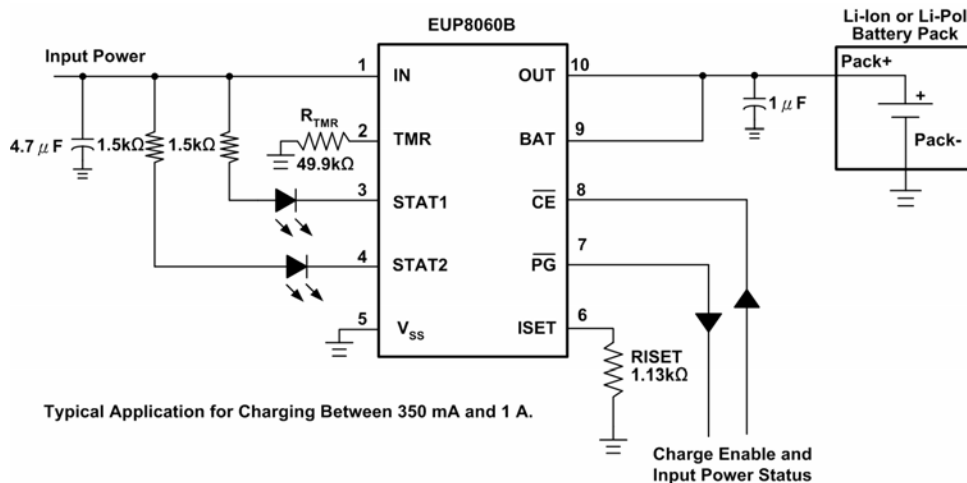- Mobile Internet Devices (M1D)
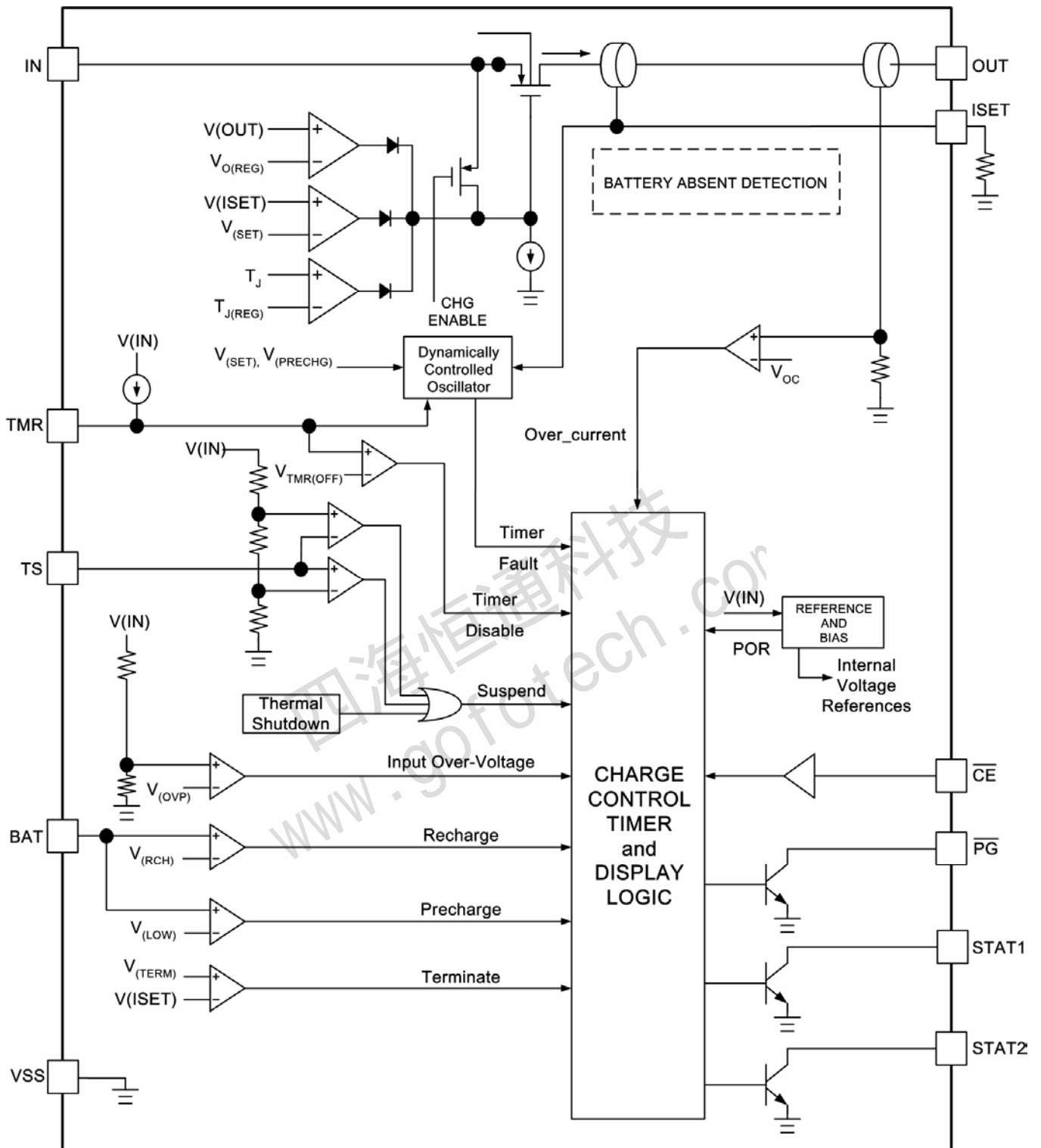
Typical Application Circuit

Figure 1. EUP8060B

Block Diagram

Figure 2. Block Diagram

Pin Configurations

Package Type	Pin　Configurations	Package Type	Pin　Configurations
EUP8060A/D TDFN-10		EUP8060B TDFN-10	
EUP8060C TDFN-10			

Pin Description

PIN	A,D	B	C	I/O	DESCRIPTION
IN	1	1	1	I	Charge Input Voltage and internal supply. Connect a 1- µF (minimum) capacitor from IN to VSS. $C_{IN} \geq C_{OUT}$
TMR	2	2	2	I	Safety Timer Program Input, timer disabled if floating. Connect a resistor to VSS pin to program safety timer timeout value
STAT1	3	3	3	O	Charge Status Output 1 (open-collector, see Table 3)
STAT2	4	4	4	O	Charge Status Output 2 (open-collector, see Table 3)
VSS	5	5	5	I	Ground
ISET	6	6	6	O	Charge current set point, resistor connected from ISET to VSS sets charge current value. Connect a 0.47-µF capacitor from BAT to ISET.
$\overline{PG}$	7	7	—	O	Power Good status output (open-collector), active low
$\overline{CE}$	—	8	7	I	Charge enable Input. $\overline{CE}$ = LO enables charger. $\overline{CE}$ = HI disables charger.
$\overline{TE}$	—	—	8	I	Termination enable Input. $\overline{TE}$ = LO enables termination detection and battery absent detection. $\overline{TE}$ = HI disables termination detection and battery absent detection.
TS	8	—	—	I	Temperature Sense Input, connect to battery pack thermistor. Connect an external resistive divider to program temperature thresholds.
BAT	9	9	9	I	Battery Voltage Sense Input. Connect to the battery positive terminal. Connect a 200Ω resistor from BAT to OUT.
OUT	10	10	10	O	Charge current output. Connect to the battery positive terminal. Connect a 1-µF (minimum) capacitor from OUT to VSS.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP8060AJIR1	TDFN-10	XXXXX 8060A	-40 °C to 85°C
EUP8060BJIR1	TDFN-10	XXXXX 8060B	-40 °C to 85°C
EUP8060CJIR1	TDFN-10	XXXXX 8060C	-40 °C to 85°C
EUP8060DJIR1	TDFN-10	XXXXX 8060D	-40 °C to 85°C

EUP8060X

Lead Free Code
1: Lead Free   0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TDFN
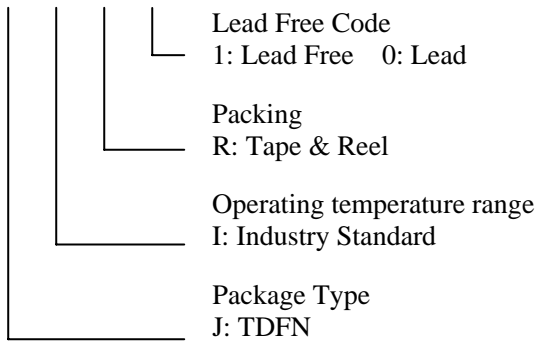
Absolute Maximum Ratings

- Supply voltage (IN with respect to Vss)--- -0.3V to18V
- Input Voltage on IN, STATx, $\overline{PG}$, TS, $\overline{CE}$, $\overline{TE}$ (all with respect to Vss) --------------------- -0.3V to VIN
- Input Voltage on OUT,BAT,ISET,TMR (all with respect to Vss) ------------------------------- -0.3V to 7V
- Output Sink Current (STATx)+PG --- 15mA
- Output Current (OUT pin) --- 1.5A
- Junction temperature range, T_J -- 150°C
- Storage temperature range, Tstg -- -65°C to 150°C
- Lead temperature (soldering, 10s) -- 260°C

Dissipation Ratings

Package	JA	$T_A < 40°C$ Power Rating	Derating Factor Above $T_A = 25°C$
TDFN-10	48°C/W	1.5W	0.0208 W/°C

Recommended Operating Conditions

	Min.	Max.	Unit
Supply voltage, V_{IN}	4.35	16.5	V
Operating junction temperature range, T_J	-40	125	°C

Electrical Characteristics over recommended operating, $T_J = 0\sim125°C$ range, See the Application Circuits section, typical values at $T_J = 25°C$ (unless otherwise noted).

SYMBOLE	PARAMETER	TEST CONDITIONS		EUP8060X			
				MIN	TYP	MAX	UNIT
POWER DOWN THRESHOLD – UNDERVOLTAGE LOCKOUT							
$V_{(UVLO)}$	Power down threshold	increase V(IN): 0 4 V		1.5		3.5	V
INPUT POWER DETECTION, $\overline{CE}$ = HI or LOW, V(IN) > 3.5 V							
$V_{IN(DT)}$	Input power detection threshold	$V_{(IN)}$ detected at [V(IN) – V(OUT)] > $V_{IN(DT)}$				180	mV
$V_{HYS(INDT)}$	Input power detection hysteresis	Input power not detected at $[V_{(IN)}- V_{(OUT)}] < [V_{IN(DT)}- V_{HYS(INDT)}]$		30			mV
$T_{DGL(INDT1)}$	Deglitch time, input power detected status	$\overline{PG}$:HI LO, Thermal regulation loop not active, $R_{TMR} = 50\ K\Omega$ or $V_{(TMR)}$ = OPEN		1.5		3.5	ms
$T_{DGL(NOIN)}$	Delay time, input power not detected status	$\overline{PG}$: LO HI after $T_{DGL(NOIN)}$				10	µs
$T_{DLY(CHGOFF)}$	Charger off delay	Charger turned off after $T_{DLY(CHGOFF)}$, Measured from $\overline{PG}$: LO HI; Timer reset after $T_{DLY(CHGOFF)}$		28		32	ms
INPUT OVERVOLTAGE PROTECTION							
$V_{(OVP)}$	Input overvoltage detection threshold	V(IN) increasing	EUP8060A/B/C	6.2	6.6	7.0	V
			EUP8060D	10.2	11	11.7	
$V_{HYS(OVP)}$	Input overvoltage hysteresis	V(IN) decreasing	EUP8060A/B/C		30		mV
			EUP8060D		30		mV
$T_{DGL(OVDET)}$	Input overvoltage detection delay	$\overline{CE}$ = HI or LO, Measured from V(IN) > $V_{(OVP)}$ to $\overline{PG}$: LO HI; VIN increasing			10	100	µs
$T_{DGL(OVNDET)}$	Input overvoltage not detected delay	$\overline{CE}$ = HI or LO, Measured from V(IN) < $V_{(OVP)}$ to $\overline{PG}$: HI LO; VIN decreasing			10	100	µs

Electrical Characteristics over recommended operating, $T_J = 0\sim125°C$ range, See the Application Circuits section, typical values at $T_J = 25°C$ (unless otherwise noted).

SYMBOLE	PARAMETER	TEST CONDITIONS		EUP8060X			
				MIN	TYP	MAX	UNIT
QUIESCENT CURRENT							
$I_{CC(CHGOFF)}$	IN pin quiescent current, charger off	Input power detected, $\overline{CE}$ = HI	$V_{(IN)}$ = 6 V		50	200	μA
			$V_{(IN)}$ = 16.5 V		250		
$I_{CC(CHGON)}$	IN pin quiescent current, charger on	Input power detected, $\overline{CE}$ = LO, V_{BAT} = 4.5 V			0.7	1.5	mA
$I_{BAT(DONE)}$	Battery leakage current after termination into IC	Input power detected, charge terminated, $\overline{CE}$ = LO			1	5	μA
$I_{BAT(CHGOFF)}$	Battery leakage current into IC, charger off	Input power detected, $\overline{CE}$ = HI OR input power not detected, $\overline{CE}$ = LO			1	5	μA
TS PIN COMPARATOR							
$V_{(TS1)}$	Lower voltage temperature threshold	Hot detected at V(TS) < $V_{(TS1)}$; NTC thermistor		29	30	31	%V(IN)
$V_{(TS2)}$	Upper voltage temperature threshold	Cold detected at V(TS) > $V_{(TS2)}$; NTC thermistor		57	58	59	%V(IN)
$V_{HYS(TS)}$	Hysteresis	Temp OK at V(TS) > [$V_{(TS1)}$ + $V_{HYS(TS)}$] OR $V_{(TS)}$ < [$V_{(TS2)}$– $V_{HYS(TS)}$]			2		%V(IN)
$\overline{CE}$ INPUT							
V_{IL}	Input (low) voltage	V($\overline{CE}$) increasing		0		1	V
V_{IH}	Input (high) voltage	V($\overline{CE}$) decreasing		2.0			
STAT1, STAT2 AND PG OUTPUTS , V(IN) VO(REG) + V(DO-MAX)							
V_{OL}	Output (low) saturation voltage	Ioutput = 5 mA (sink)				1.2	V
THERMAL SHUTDOWN							
$T_{(SHUT)}$	Temperature trip	Junction temperature, temp rising			155		°C
$T_{(SHUTHYS)}$	Thermal hysteresis	Junction temperature			20		°C
VOLTAGE REGULATION, V(IN) VO(REG) + V(DO-MAX), I(TERM) < I(OUT) < IO(OUT), CHARGER ENABLED, NO FAULT CONDITIONS DETECTED							
$V_{O(REG)}$	Output voltage	EUP8060A/B/C/D			4.20		V
$V_{O(TOL)}$	Voltage regulation accuracy			–1%		1%	
$V_{(DO)}$	Dropout voltage, V(IN) – V(OUT)	$I_{(OUT)}$ = 1 A			800		mV
CURRENT REGULATION , V(IN) > V(OUT) > V(DO-MAX), CHARGER ENABLED, NO FAULT CONDITIONS DETECTED							
$I_{O(OUT)}$	Output current range	$V_{(BAT)} > V_{(LOWV)}$, $I_{O(OUT)} = I_{(OUT)} = K_{(SET)} \times V_{(SET)}/R_{SET}$		100		1000	mA
$V_{(SET)}$	Output current set voltage	V(ISET) = $V_{(SET)}$, $V_{(LOWV)}$ < V(BAT) $V_{O(REG)}$		2.45	2.50	2.55	V
$K_{(SET)}$	Output current set factor	100 mA $I_{O(OUT)}$ 1000 mA	$\dfrac{mA \times k\Omega}{Volts}$	325		445	
R_{ISET}	External resistor range	Resistor connected to ISET pin		0.7		10	kΩ
VOLTAGE AND CURRENT REGULATION TIMING, V(IN) > V(OUT) + V(DO-MAX), CHARGER ENABLED, NO FAULT CONDITIONSDETECTED, RTMR = 50K or V(TMR) = OPEN; Thermal regulation loop not active							
$T_{PWRUP(CHG)}$	Input power detection to full charge current time delay	Measured from $\overline{PG}$:HI LO to I(OUT) > 100 mA, $\overline{CE}$ = LO, $I_{O(OUT)}$ = 1 A, V(BAT) = 3.5 V			25	35	ms
$T_{PWRUP(EN)}$	Charge enable to full charge current delay	Measured from $\overline{CE}$:HI LO to I(OUT) >100 mA, $I_{O(OUT)}$ = 1A, $V_{(BAT)}$= 3.5 V, $V_{(IN)}$ = 4.5 V, Input power detected			25	35	ms
$T_{PWRUP(LDO)}$	Input power detection to voltage regulation delay, LDO mode set, no battery or load connected	Measured from $\overline{PG}$:HI LO to V(OUT) > 90% of charge voltage regulation; $V_{(TMR)}$ = OPEN, LDO mode set, no battery and no load at OUT pin, $\overline{CE}$ = LO			25	35	ms
PRECHARGE AND OUTPUT SHORT-CIRCUIT CURRENT REGULATION, V(IN)–V(OUT) > V(DO-MAX) , V(IN) ≥ 4.5V, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, RTMR = 50K or V(TMR)=OPEN; Thermal regulation loop not active							
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	$V_{(BAT)}$ increasing		2.8	2.95	3.15	V
$V_{(SC)}$	Precharge to short-circuit transition threshold	$V_{(BAT)}$ decreasing		1.2	1.4	1.6	V

Electrical Characteristics over recommended operating, T_J = 0~125°C range, See the Application Circuits section, typical values at T_J = 25°C (unless otherwise noted).

SYMBOLE	PARAMETER	TEST CONDITIONS		EUP8060X			UNIT
				MIN	TYP	MAX	
PRECHARGE AND OUTPUT SHORT-CIRCUIT CURRENT REGULATION, V(IN)–V(OUT) > V(DO-MAX) , V(IN) ≥ 4.5V, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, RTMR = 50K or V(TMR)=OPEN; Thermal regulation loop not active							
$V_{(SCIND)}$	Short-circuit indication	$V_{(BAT)}$ decreasing		1.6	1.8	2.0	V
$I_{O(PRECHG)}$	Precharge current range	$V(SC) < VI(BAT) < V(LOWV)$, $t < T(PRECHG)$ $IO(PRECHG) = K(SET) \times V(PRECHG)/R(ISET)$		10		100	mA
$V_{(PRECHG)}$	Precharge set voltage	$V_{(ISET)} = V_{(PRECHG)}$, $V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$, $t < T_{(PRECHG)}$		225	250	280	mV
$I_{O(SHORT)}$	Output shorted regulation current	$V_{SS} \quad V_{(BAT)} \quad V_{(SCI)}$, $I_{O(SHORT)} = I_{(OUT)}$, $V_{(BAT)}$=VSS	$V_{POR} < V_{IN} < 6.0V$	15	22	30	mA
			$6.0\ V < V_{IN} < V_{OVP}$		25		
TEMPERATURE REGULATION (Thermal regulation™), CHARGER ENABLED, NO FAULT CONDITIONS DETECTED							
$T_{J(REG)}$	Temperature regulation limit	$V(IN) = 5.5\ V$, $V(BAT) = 3.2\ V$, Fast charge current set to 1A		101	112	125	°C
$I_{(MIN\_TJ(REG))}$	Minimum current in thermal regulation	$V(LOWV) < V(BAT) < VO(REG)$, $0.7k\Omega < RISET < 3.5k\Omega$			100	160	mA
CHARGE TERMINATION DETECTION, VO(REG) = 4.2 V, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, Thermal regulation LOOP NOT ACTIVE, RTMR = 50K or TMR pin OPEN							
$I_{(TERM)}$	Termination detection current range	$V_{(BAT)} > V_{(RCH)}$, $I_{(TERM)} = K_{(SET)} \times V_{(TERM)}/R_{ISET}$		10		100	mA
$V_{(TERM)}$	Charge termination detection set voltage[1]	$V_{(BAT)} > V_{(RCH)}$		225	250	275	mV
$T_{DGL(TERM)}$	Deglitch time, termination detected	$V_{(ISET)}$ decreasing		15	25	35	ms
BATTERY RECHARGE THRESHOLD							
$V_{(RCH)}$	Recharge threshold detection	$[V_{O(REG)}–V(BAT)] > V_{(RCH)}$		75	100	135	mV
$T_{DGL(RCH)}$	Deglitch time, recharge detection	$V_{(BAT)}$ decreasing		15	25	35	ms
TIMERS, $\overline{CE}$ = LO, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, V(TMR) < 3 V, TIMERS ENABLED							
$T_{(CHG)}$	Charge safety timer range	$T_{(CHG)} = K_{(CHG)} \times R_{TMR}$; thermal loop not active		3		10	hours
$K_{(CHG)}$	Charge safety timer constant	$V_{(BAT)} > V_{(LOWV)}$		0.08	0.1	0.12	hr/kΩ
$T_{(PCHG)}$	Pre-charge safety timer range	$T_{(PCHG)} = K_{(PCHG)} \times T_{(CHG)}$; Thermal regulation loop not active		1080		3600	sec
$K_{(PCHG)}$	Pre-charge safety timer constant	$V_{(BAT)} < V_{(LOWV)}$		0.08	0.1	0.12	
$V_{TMR(OFF)}$	Charge timer and termination enable threshold	[Charge timer AND termination disabled] at $V_{(TMR)}$ > $V_{(TMR(OFF)}$	EUP8060A/B/D	2.5	3.0	3.5	V
	Charge timer enable threshold	[Charge timer disabled] at $V_{(TMR)}$ > $V_{(TMR(OFF)}$	EUP8060C				
I_{TMR}	TMR pin source current	$V_{(TMR)} = 3.5\ V$, $V_{(IN)} = 4.5\ V$		1		6	µA
BATTERY DETECTION THRESHOLDS							
$I_{DET(DOWN)}$	Battery detection current (sink)	$2\ V < V_{(BAT)} < V_{O(REG)}$		1	2	3.2	mA
$I_{DET(UP)}$	Battery detection current (source)	$2\ V < V_{(BAT)} < V_{O(REG)}$			IO(PRECHG)		
$T_{(DETECT)}$	Battery detection time	$2\ V < V_{(BAT)} < V_{O(REG)}$, Thermal regulation loop not active; $R_{TMR} = 50\ k\Omega$, $I_{DET(down)}$ or $I_{DET\ (UP)}$		85	120	150	ms
TIMER FAULT RECOVERY							
$I_{(FAULT)}$	Fault Current (source)	$V_{(OUT)} < V_{(RCH)}$			-10		mA
CHARGE OVERCURRENT DETECTION, V(IN) 4.5 V, CHARGER ENABLED							
$I_{CH(OI)}$	Charge overcurrent detection threshold	$V_{(ISET)}$ = VSS			1.8		A
$T_{DGL(OI)}$	Overcurrent detection delay time	Measured from $V_{(ISET)}$ = VSS to $I_{O(OUT)} = 0$			100		µs

(1) The voltage on the ISET pin is compared to the V(TERM) voltage to determine when the termination should occur.

Typical Operating Characteristics
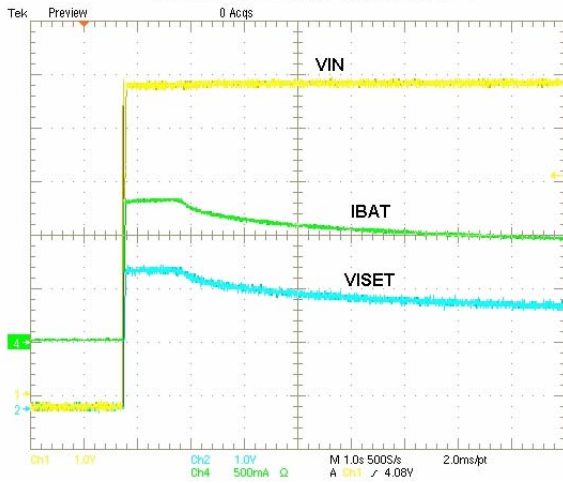
Figure3.

Figure4.

Figure5.

Figure6.

Figure7.

Figure8.

FAST-CHARGE CURRENT vs BATTERY VOLTAGE

Figure9.

FAST-CHARGE CURRENT vs BATTERY VOLTAGE

Figure10.

KSET LINEARITY vs CHARGE CURRENT

Figure11.

KSET LINEARITY vs CHARGE CURRENT

Figure12.

BATTERY REGULATION VOLTAGE vs INPUT VOLTAGE
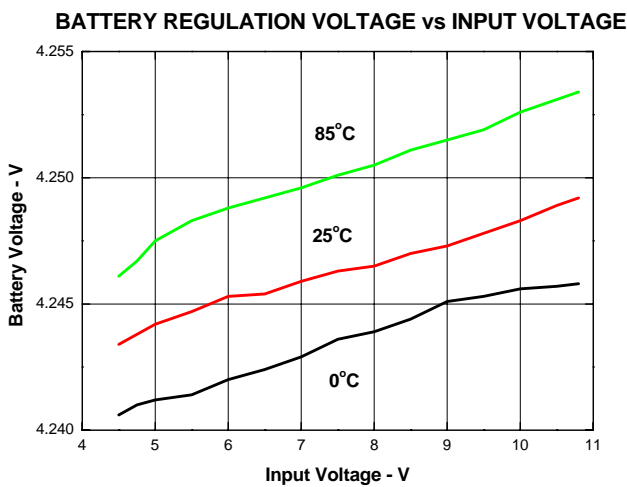

Figure13.

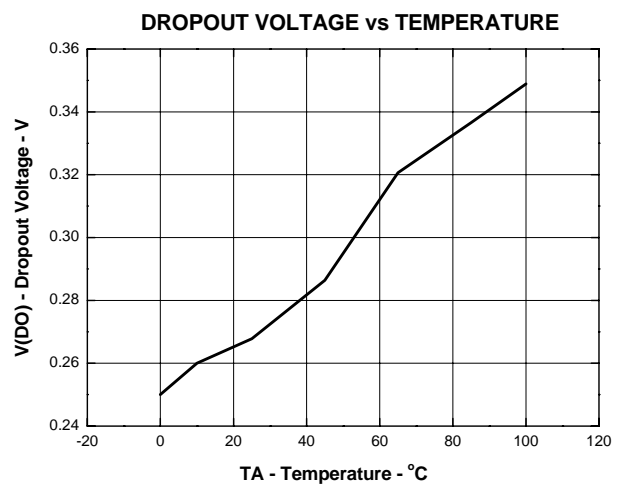**DROPOUT VOLTAGE vs TEMPERATURE**
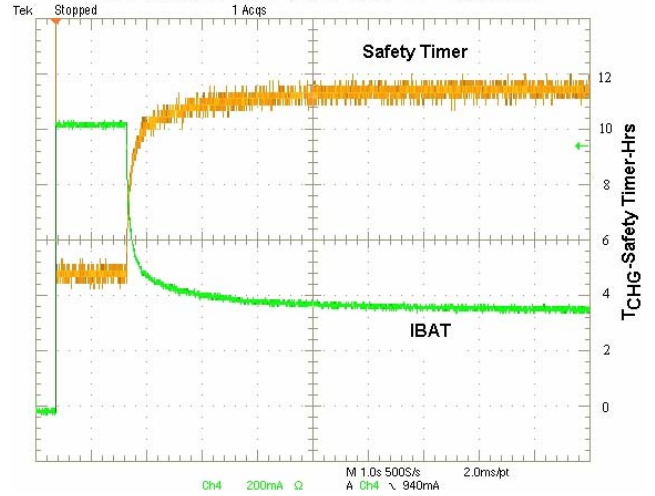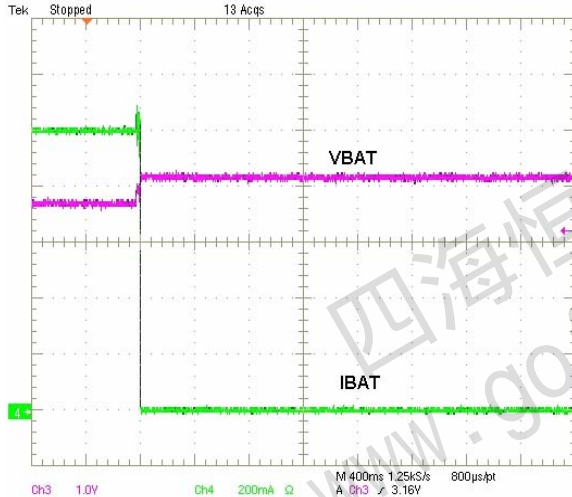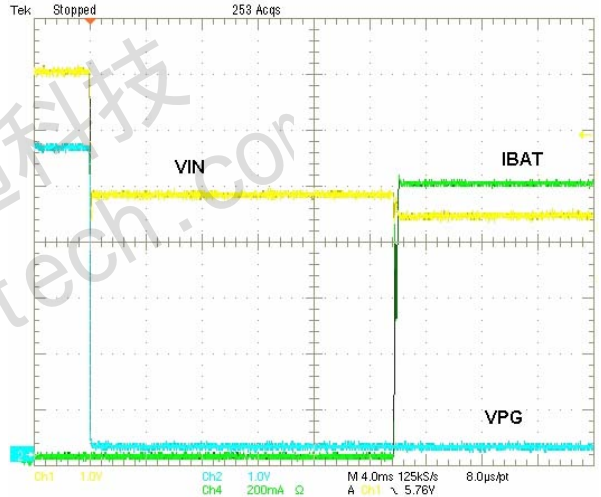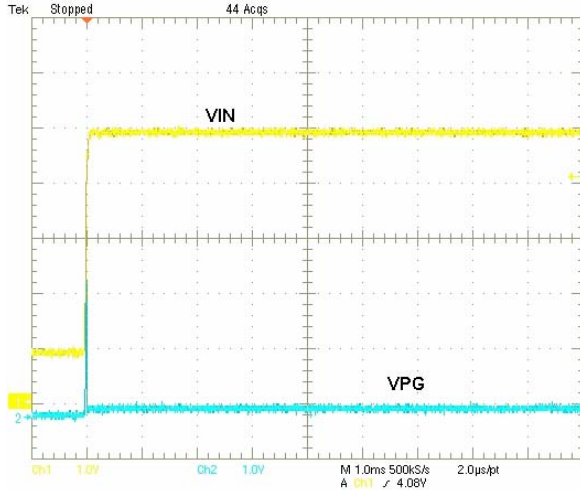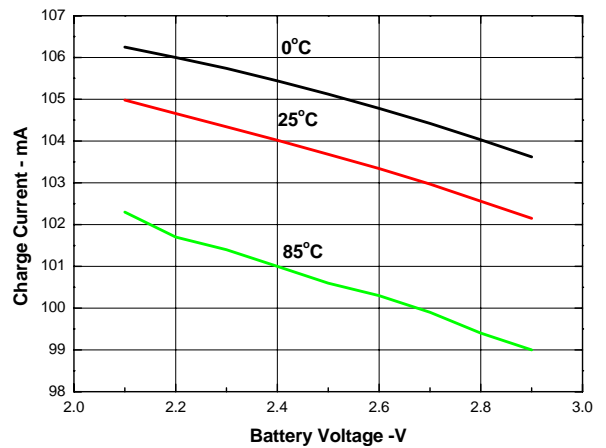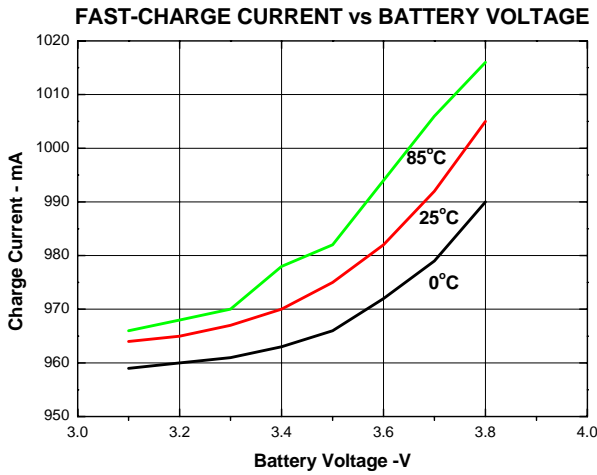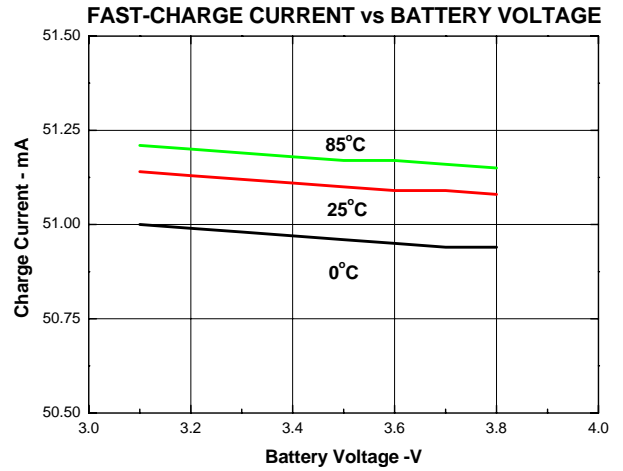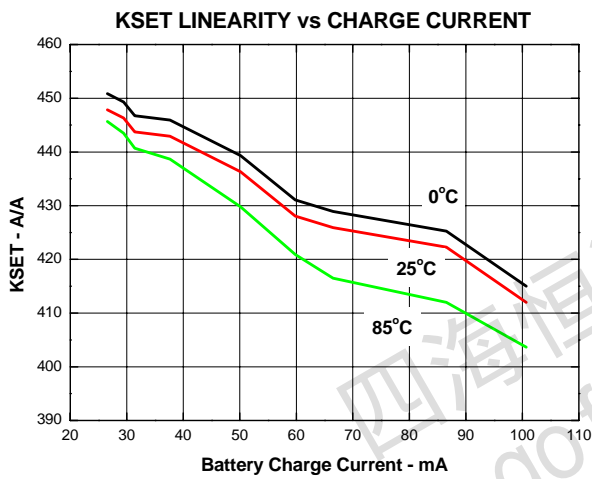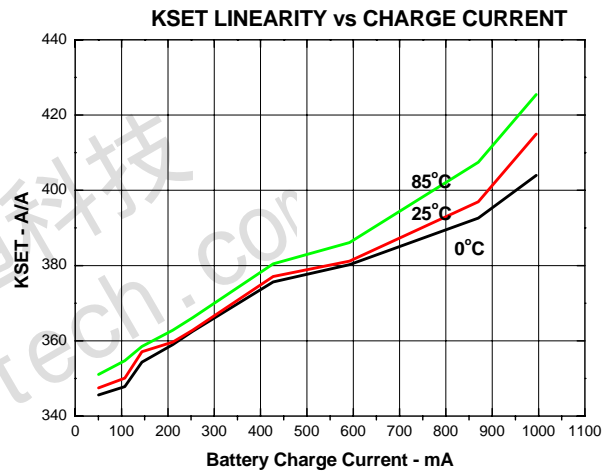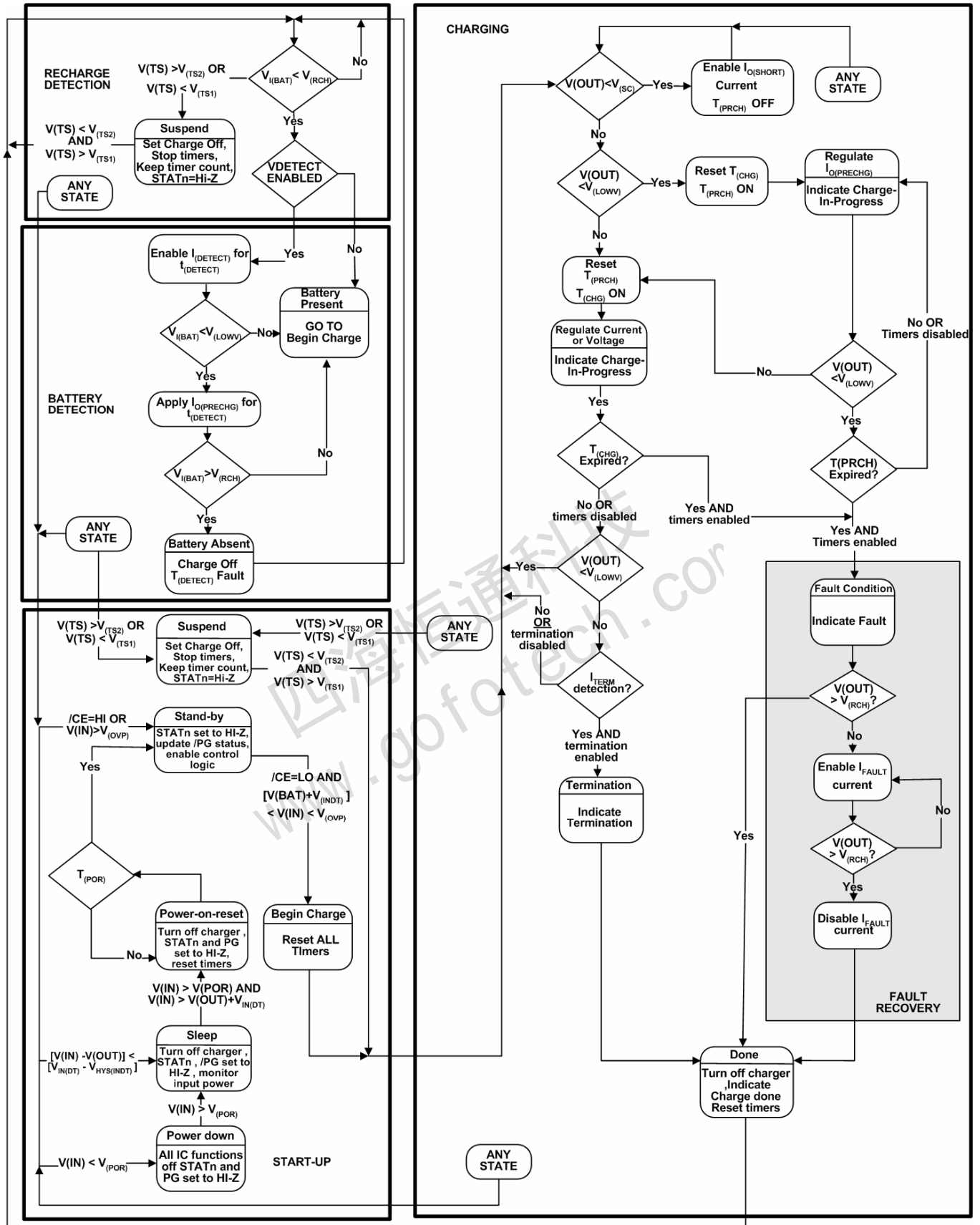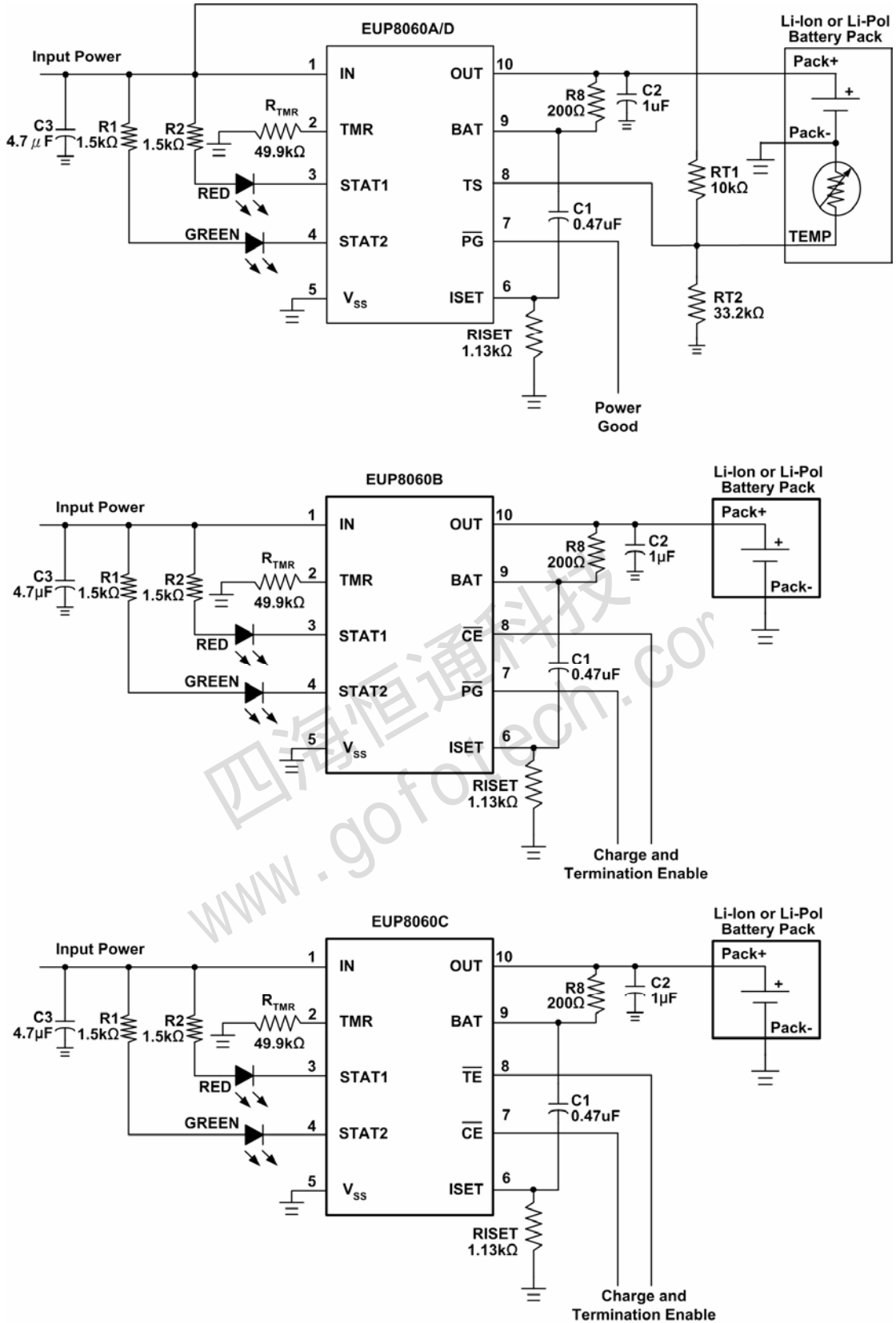

Figure14.

State Machine Diagram

Figure 15. Operational Flow chart

Typical Application

NOTE: Temp window set between 0   and 45   for application w/TS pin.

Figure 16. Application Circuit

FUNCTIONAL DESCRIPTION

The charge current is programmable using external components (R_{ISET} resistor). A typical charge profile is shown below, for an operation condition that does not cause the IC junction temperature to exceed $T_{J(REG)}$, (112 typical).
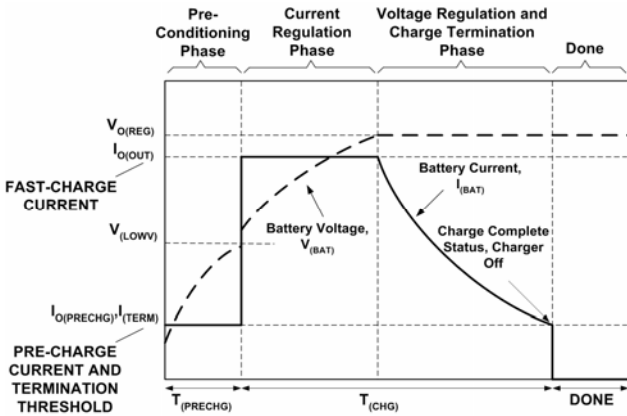

Figure 17.Charging Profile Within $T_{J(REG)}$

If the operating conditions cause the IC junction temperature to exceed $T_{J(REG)}$, the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to $T_{J(REG)}$, effectively regulating the IC junction temperature.

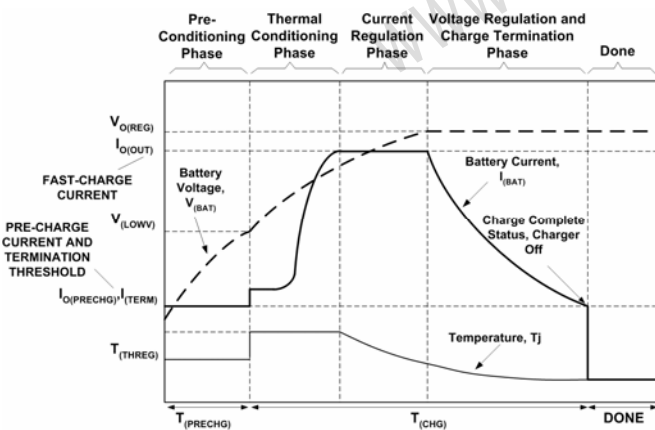A modified charge cycle, with the thermal loop active, is shown in Figure 18.

Figure 18.Charging Profile ,Thermal Loop Active

OPERATING MODES

Power Down

The EUP8060X family is in a power-down mode when the input power voltage (IN) is below the power-down threshold $V_{(UVLO)}$. During the power down mode all IC functions are off, and the host commands at the control pins are not interpreted. The status output pins STAT1 and STAT2 are set to high impedance mode and $\overline{PG}$ output is set to the high impedance state.

Sleep Mode

The EUP8060X enters the sleep mode when the input power voltage (IN) is above the power down threshold $V_{(UVLO)}$ but still lower than the input power detection threshold, $V(IN) < V(OUT) + V_{IN(DT)}$.

During the sleep mode the charger is off, and the host commands at the control pins are not interpreted. The status output pins STAT1 and STAT2 are set to the high impedance state and the $\overline{PG}$ output indicates input power not detected.

The sleep mode is entered from any other state, if the input power (IN) is not detected.

Overvoltage Lockout

The input power is detected when the input voltage V(IN) > V(OUT) + $V_{IN(DT)}$. The EUP8060X transitions from the sleep mode to the power-on-reset mode. In this mode of operation an internal timer $T_{(POR)}$ is started. Until the timer expires the STAT1 and STAT2 outputs indicate charger OFF, and the $\overline{PG}$ output indicates the input power status as not detected.

At the end of the power-on-reset delay. The STAT1, STAT2 and $\overline{PG}$ pins are active.

Stand-By Mode

In the EUP8060B/C the stand-by mode is started at the end of the power-on-reset phase, if the input power is detected and $\overline{CE}$ = HI. In the stand-by mode selected blocks in the IC are operational, and the control logic monitors system status and control pins to define if the charger will set to on or off mode. The quiescent current required in stand-by mode is 50 µA typical.

If the $\overline{CE}$ pin is not available the EUP8060X enters the begin charge mode at the end of the power-on-reset phase.

Begin Charge Mode

All blocks in the IC are powered up, and the EUP8060X is ready to start charging the battery pack. A new charge cycle is started when the control logic decides that all conditions required to enable a new charge cycle are met. During the begin charge phase all timers are reset, after that the IC enters the charging mode.

Charge Mode

When the charging mode is active the EUP8060X executes the charging algorithm, as described in the operational flow chart, Figure 15.

Suspend Mode

The suspend mode is entered when the pack temperature is not within the valid temperature range. During the suspend mode the charger is set to off, but the timers are not reset.

The normal charging mode resumes when the pack temperature is within range.

LDO Mode Operation

The *LDO Mode* (TMR pin open circuit) disables the charging termination circuit, disables the battery detect routine and holds the safety timer clock in reset. This is often used for operation without a battery or in production testing. The OUT pin current can be monitored via the ISET pin. If in LDO mode without a battery present, It is recommended that a 200Ω feedback resistor,R8, be used, see Figure 16.

CONTROL LOGIC OVERVIEW

An external host can enable or disable the charging process using a dedicated control pin, $\overline{CE}$. A low-level signal on this pin enables the charge, and a high-level signal disables the charge. The EUP8060X is in stand-by mode with $\overline{CE}$ = HI. When the charger function is enabled ($\overline{CE}$ = LO) a new charge is initiated. Table 1 describes the charger control logic operation, in EUP8060X versions without the TS pin the pack temp status is internally set to OK.

In both STANDBY and SUSPEND modes the charge process is disabled. In the STANDBY mode all timers are reset; in SUSPEND mode the timers are held at the count stored when the suspend mode was set.

The timer fault, termination and output short circuit variables shown in the control logic table are latched in the detection circuits, outside the control logic. Refer to the timers, termination and short circuit protection sections for additional details on how those latched variables are reset.

Temperature Qualification
(Applies only to versions with TS pin option)

The EUP8060X continuously monitors battery temperature by measuring the voltage between the TS and VSS pins.

An internal current source provides the bias for most common 10-k negative-temperature coefficient thermistors (NTC). The device compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected the device immediately suspend the charge. The device suspend charge by turning off the power FET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

However the user may modify these thresholds by adding two external resistors. See Figure 16.

Input Overvoltage Detection, Power Good Status Output

The input power detection status for pin IN is shown at the open collector output pin $\overline{PG}$.

Table 2. Input Power Detection Status

INPUT POWER DETECTION (IN)	$\overline{PG}$ STATE
NOT DETECTED	High impedance
DETECTED, NO OVERVOLTAGE	LO
DETECTED, OVERVOLTAGE	High impedance

The EUP8060X detects an input overvoltage when V(IN) > $V_{(OVP)}$. The charger function is turned off and the EUP8060X is set to standby mode of operation. The OVP detection is not latched, and the IC returns to normal operation when the fault condition is removed.

Table 1. Control Logic Functionality

EUP8060X OPERATION MODE	$\overline{CE}$	INPUT POWER	TIMER FAULT (latched)	OUTPUT SHORT CIRCUIT	TERMI-NATION (latched)	PACK TEMP	THERMAL SHUTDOWN	POWER DOWN	CHARGER POWER STAGE
POWER DOWN	LO	Low	X	X	X	X	X	Yes	**OFF**
SLEEP	X	Not Detected	X	X	X	X	X	No	**OFF**
STANDBY	HI	Detected	X	X	X	X	X	No	**OFF**
SEE STATE DIAGRAM	LO	Detected	X	Yes	X	X	X	No	
	LO	Detected	No	No	Yes	X	X	No	**OFF**
	LO	Detected	Yes	No	No	X	X	No	**IFAULT**
	LO	Detected	No	No	Yes	Absent	$T_J<T_{SHUT}$	No	**IDETECT**
	LO	Detected	No	No	No	Hot or Cold	$T_J<T_{SHUT}$	No	**OFF**
	LO	Detected	No	No	No	Ok	$T_J>T_{SHUT}$	No	**OFF**
	LO	Over Voltage	No	No	No	Ok	$T_J<T_{SHUT}$	No	**OFF**
CHARGING	LO	Detected	No	No	No	Ok	$T_J<T_{SHUT}$	No	**ON**

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 3. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-collector transistor is turned off.

Table 3. Charge Status [1]

Charge State	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Done (termination enabled only)	OFF	ON
Charge Suspend (temperature)	OFF	OFF
Timer Fault		
Charger off		
Selected input power overvoltage detected		
Battery absent		
Batteryshort		

(1) Pulse loading on the OUT pin may cause the IC to cycle between Done and charging states (LEDs Flashing)

(2) When termination is disabled (TMR pin floating or $\overline{TE}$ = Hi, EUP8060C) the Done state is not available; the status LEDs indicate fast charge if $V_{BAT} > V_{LOWV}$ and precharge if $V_{BAT} < V_{LOWV}$. The available output current is a function of the OUT pin voltage, See Figure 23.

Battery Charging: Constant Current Phase

TheEUP8060 family offers on-chip current regulation. The current regulation is defined by the value of the resistor connected to ISET pin.

During a charge cycle the fast charge current $I_{O(OUT)}$ is applied to the battery if the battery voltage is above the $V_{(LOWV)}$ threshold (2.95 V typical):

$$I(OUT) = I_{O(OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{ISET}} \quad (3)$$

Where $K_{(SET)}$ is the output current set factor and $V_{(SET)}$ is the output current set voltage.

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold a pre-charge current $I_{(PRECHG)}$ is applied to the battery. This feature revives deeply discharged cells.

$$I(OUT) = I_{(PRECHG)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{ISET}} \sim \frac{I_{O(OUT)}}{10} \quad (4)$$

Where $K_{(SET)}$ is the output current set factor and $V_{(PRECHG)}$ is the precharge set voltage.

At low constant current charge currents, less than 350 mA, it is recommended that a 0.47μF capacitor be placed between the ISET and BAT pins to insure stability, see Figure 16.

Charge Current Translator

When the charge function is enabled internal circuits generate a current proportional to the charge current at the ISET pin. This current, when applied to the external charge current programming resistor R_{ISET} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the OUT pin.

$$V(ISET) = I(OUT) \times \frac{R_{ISET}}{K_{(SET)}} \quad (5)$$

Battery Voltage Regulation

The battery pack voltage is sensed through the BAT pin, which is tied directly to the positive side of the battery pack. The EUP8060X monitors the battery pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold the voltage regulation phase begins and the charging current begins to taper down.The voltage regulation threshold $V_{O(REG)}$ is fixed by an internal IC voltage reference.

Pre-Charge Timer

The EUP8060X family activates an internal safety timer during the battery pre-conditioning phase. The charge safety timer time-out value is set by the external resistor connected to TMR pin, RTMR and the timeout constants $K_{(PCHG)}$ and $T_{(CHG)}$:

$$T_{(PCHG)} = K_{(PCHG)} \times T_{(CHG)}$$

The pre-charge timer operation is detailed in Table 4.

Table 4. Pre-Charge Timer Operational Modes

8060X Mode	VOUT > $V_{(LOWV)}$	PRE-CHARGE TIMER MODE
STANDBY ($\overline{CE}$ = Hi)	X	*RESET*
CHARGING	Yes	*RESET*
SUSPEND (TS out of range)	Yes	*RESET*
SUSPEND (TS out of range)	No	*Hold*
CHARGING, TMR PIN NOT OPEN	No	*COUNTING, EXTERNAL PROGRAMMED RATE*
CHARGING, TMR PIN OPEN	X	*RESET*

In SUSPEND mode the pre-charge timer is put on hold (i.e., pre-charge timer is not reset), normal operation resumes when the timer returns to the normal operating mode (COUNTING). If V(BAT) does not reach the internal voltage threshold $V_{(LOWV)}$ within the pre-charge timer period a fault condition is detected, the charger is turned off and the pre-charge safety timer fault condition is latched.

When the pre-charge timer fault latch is set the charger is turned off. Under those conditions a small current I_{FAULT} is applied to the OUT pin, as long as input power (IN) is detected AND V(OUT) < $V_{(LOWV)}$, as part of a timer fault recovery protocol. This current allows the output voltage to rise above the pre-charge threshold $V_{(LOWV)}$, resetting the pre-charge timer fault latch when the pack is removed. Table 5 further details the pre-charge timer fault latch operation.

Table 5. Pre-Charge Timer Latch Functionality

PRE-CHARGE TIMER FAULT ENTERED WHEN	PRE-CHARGE TIMER FAULT LATCH RESET AT
Pre-charge timer timeout **AND** V(OUT) > $V_{(LOWV)}$	$\overline{CE}$ rising edge or OVP detected
	Input power removed (not detected)
	Timer function disabled

Thermal Protection Loop

An internal control loop monitors the EUP8060X junction termperature (T_J) to ensure safe operation during high power dissipations and or increased ambient temperatures. This loop monitors the EUP8060X junction temperature and reduces the charge current as necessary to keep the junction temperature from exceeding, $T_{J(REG)}$, (112°C, typical).

The EUP8060X 's thermal loop control can reduce the charging current down to ~100mA if needed. If the junction temperature continues to rise, the IC will enter thermal shutdown.

Thermal Shutdown and Protection

Internal circuits monitor the junction temperature, T_J, of the die and suspends charging if T_J exceeds an internal threshold $T_{(SHUT)}$ (155°C typical). Charging resumes when T_J falls below the internal threshold $T_{(SHUT)}$ by approximately 20°C.

Dynamic Timer Function

The charge and pre-charge safety timers are programmed by the user to detect a fault condition if the charge cycle duration exceeds the total time expected under normal conditions. The expected charge time is usually calculated based on the fast charge current rate.

When the thermal loop is activated the charge current is reduced, and EUP8060X activates the dynamic timer control, an internal circuit that slows down the safety timer's clock frequency. The dynamic timer control circuit effectively extends the safety time duration for either the precharge or fast charge timer modes. This minimizes the chance of a safety timer fault due to thermal regulation.

The EUP8060X dynamic timer control (DTC) monitors the voltage at pin ISET during pre-charge and fast charge, and if in thermal regulation slows the clock frequency proportionately to the change in charge current. The time duration is based on ripple counter, so slowing the clock frequency is a real time correction. The DTC circuit changes the safety timers clock period based on the $V_{(SET)}/V_{(ISET)}$ ratio (fast charge) or $V_{(PRECHG)}/V_{(SET)}$ ratio (pre-charge). Typical safety timer multiplier values relative to the $V_{(SET)}/V_{(ISET)}$ ratio is shown in Figure 19 and Figure 20.

Charge Termination Detection and Recharge

The charging current is monitored during the voltage regulation phase. Charge termination is indicated at the STATx pins (STAT1 = Hi-Z; STAT2 = Low) once the charge current falls below the termination current threshold $I_{(TERM)}$. A deglitch period $T_{DGL(TERM)}$ is added to avoid false termination indication during transient events.

Charge termination is not detected if the charge current falls below the termination threshold as a result of the thermal loop activation. Termination is also not detected when charger enters the suspend mode, due to detection of invalid pack temperature or internal thermal shutdown. Table 6 describes the termination latch functionality.

Table 6. Termination Latch Functionality

TERMINATION DETECTED LATCHED WHEN	TERMINATION LATCH RESET AT
I(OUT)<$I_{(TERM)}$ AND t >$T_{DGL(TERM)}$ **AND** V(OUT) > $V_{(RCH)}$	$\overline{CE}$ rising edge or OVP detected
	New charging cycle started; see state diagram
	Termination disabled

The termination function is DISABLED:
1. In EUP8060A/B/D the termination is disabled when the TMR pin is left open (floating).
2. In EUP8060C leaving TMR pin open (floating) does NOT disable the termination. The only way to disable termination in the EUP8060C is to set $\overline{TE}$ = HIGH.
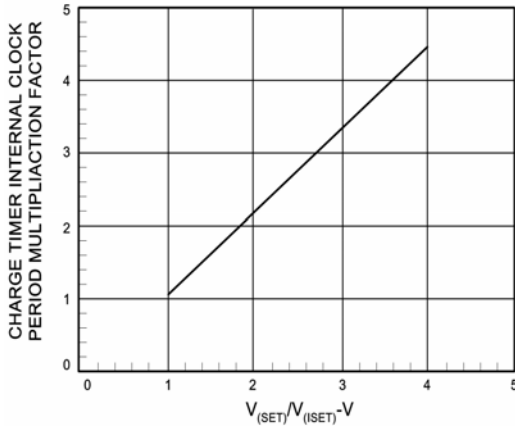

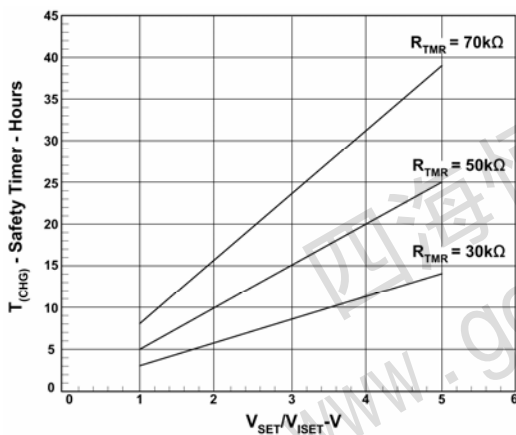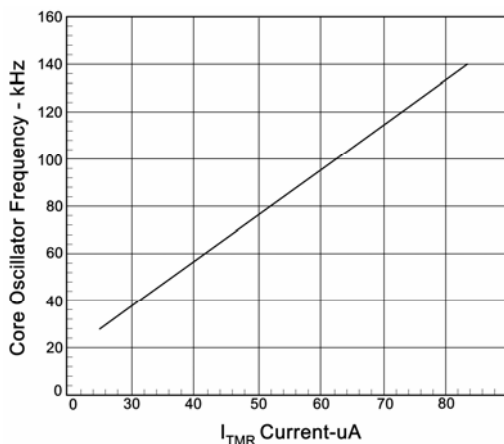**Figure 19. Safety Timer Linearity Internal Clock Period Multiplication Factor**

Figure 20. Safety Timer Linearity for R_{TMR} Values

Figure 21. Oscillator Linearity vs I_{TMR} R_{TMR} 30KΩ-100KΩ

Battery Absent Detection-Voltage Mode Algorithm

The EUP8060X provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs. The detection circuit applies an internal current to the battery terminal, and detects battery presence based on the terminal voltage behavior. Figure 22 has a typical waveform of the output voltage when the battery absent detection is enabled and no battery is connected:
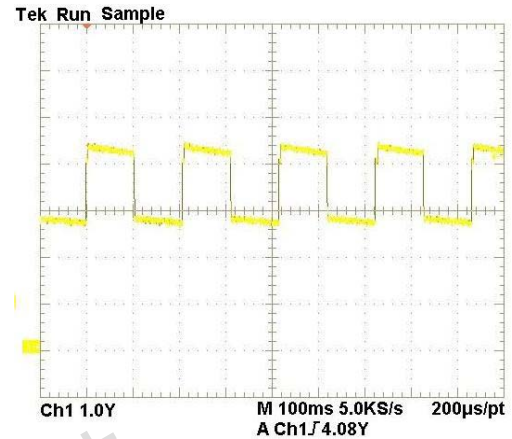

Figure 22. Battery-Absent Detection Waveforms

The battery absent detection function is disabled if the voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, after termination detection. When the voltage at the BAT pin falls to the recharge threshold, either by connection of a load to the battery or due to battery removal, the EUP8060 begins a battery absent detection test. This test involves enabling a detection current, $I_{DET(DOWN)}$, for a period of $T_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the precharge current, $I_{DET(UP)}$ is applied for a period of $T_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold.

Passing both of the discharge and charging tests (battery terminal voltage being below the pre-charge and above the recharge thresholds on the battery detection test) indicates a battery absent fault at the STAT1 and STAT2 pins. Failure of either test starts a new charge cycle. For the absent battery condition the voltage on the BAT pin rises and falls between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See the operation flowchart for more details on this algorithm. If it is desired to power a system load without a battery, it is recommended to float the TMR pin which puts the charger in *LDD mode* (disables termination).

The battery absent detection function is disabled when the termination is disabled.

Charge Safety Timer

As a safety mechanism the EUP8060X has a user-programmable timer that monitors the total fast charge time.

This timer (charge safety timer) is started at the beginning of the fast charge period. The safety charge timeout value is set by the value of an external resistor connected to the TMR pin (R_{TMR}); if pin TMR is left open (floating) the charge safety timer is disabled.

The charge safety timer time-out value is calculated as follows:

$$T_{(CHG)} = [K_{(CHG)} \times R_{(TMR)}]$$

The safety timer operation modes are shown in Table 7

Table 7. Charge Safety Timer Operational Modes

EUP8060X	VOUT > $V_{(LOWV)}$	CHARGE SAFETY TIMER MODE
STANDBY	X	*RESET*
CHARGING	No	*RESET*
SUSPEND	No	*RESET*
SUSPEND	Yes	*SUSPEND*
CHARGING, TMR PIN NOT OPEN	Yes	*COUNTING*
CHARGING, TMR PIN OPEN	X	*RESET*

In SUSPEND mode the charge safety timer is put on hold (i.e., charge safety timer is not reset), normal operation resumes when the TS fault is removed and the timer returns to the normal operating mode (COUNTING). If charge termination is not reached within the timer period a fault condition is detected. Under those circumstances the LED status is updated to indicate a fault condition and the charger is turned off.

When the charge safety timer fault latch is set and the charger is turned off a small current IFAULT is applied to the OUT pin, as long as input power (IN) is detected AND V(OUT) < $V_{(RCHG)}$, as part of a timer fault recovery protocol. This current allows the output voltage to rise above the recharge threshold $V_{(RCHG)}$ if the pack is removed, and assures that the charge safety timer fault latch is reset if the pack is removed and re-inserted. Table 8 further details the charge safety timer fault latch operation.

Table 8. Charge Safety Timer Latch Functionality

CHARGE SAFETY TIMER FAULT ENTERED	CHARGE SAFETY TIMER FAULT LATCH RESET AT
V(OUT) > $V_{(LOW\ V)}$	$\overline{CE}$ rising edge or OVP detected
	Input power removed (not detected)
	New charging cycle started; see state diagram

Short circuit Protection

The internal comparators monitor the battery voltage and detect when a short circuit is applied to the battery terminal. If the voltage at the BAT pin is less than the internal threshold V(scind) (1.8V typical), the STAT pins indicate a fault condition (STAT1 = STAT2 = Hi-Z). When the voltage at the BAT pin falls below a second internal threshold V(sc) (1.4V typical), the charger power stage is turned off. A recovery current, I(short) (22 mA typical), is applied to the BAT pin, enabling detection of the short circuit removal. The battery output current versus battery voltage is shown in the graph, Figure 23.
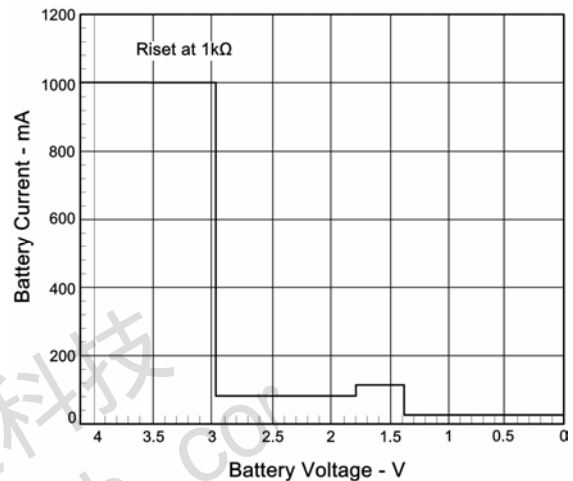

Figure 23. Short circuit Behavior

See the application section for additional details on start-up operation with $V(BAT) < V_{(SC)}$.

**Startup with Deeply Depleted Battery Connected**

The EUP8060X charger furnishes the programmed charge current if a battery is detected. If no battery is connected the EUP8060X operates as follows:

· The output current is limited to 22 mA (typical), if the voltage at BAT pin is below the short circuit detection threshold $V_{(SC)}$, 1.8 V typical.

· The output current is regulated to the programmed pre-charge current if $V_{(SC)} < V(BAT) < V_{(LOWV)}$.

· The output current is regulated to the programmed fast charge current If $V(BAT) > V_{(LOWV)}$ **AND** voltage regulation is not reached.

The output voltage collapses if no battery is present and the end equipment requires a bias current larger that the available charge current.

Packaging Information

TDFN-10

DETAIL A
Thermal Pad Option
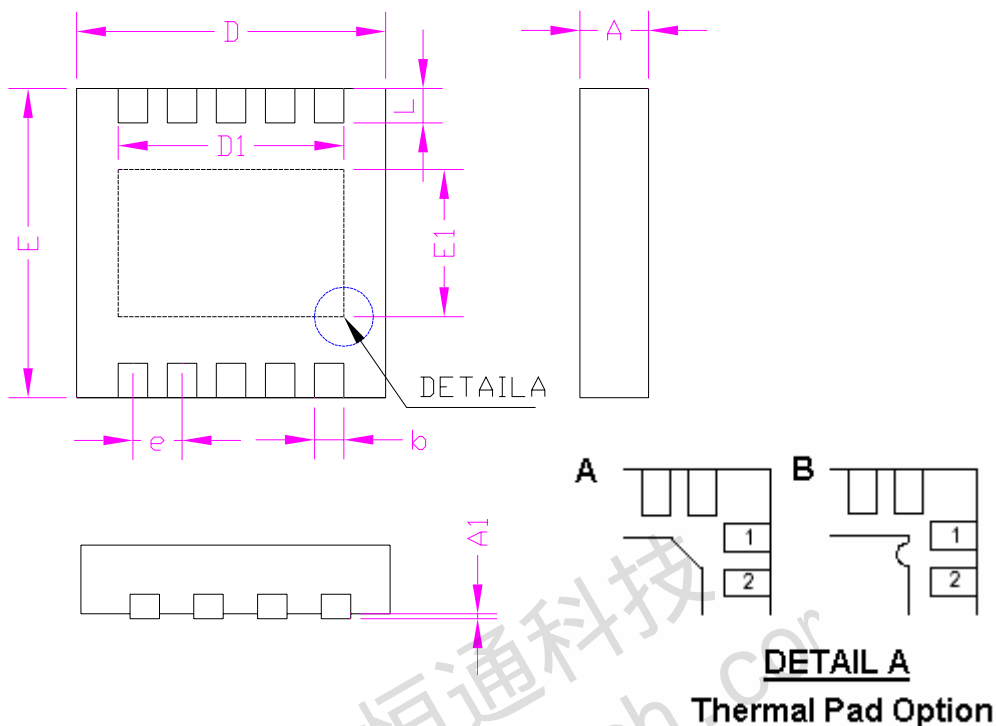
SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
D	2.90	3.10	0.114	0.122
E1	1.70		0.067	
E	2.90	3.10	0.114	0.122
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012
e	0.50		0.020	
D1	2.40		0.094	