100mA Current Sink VCM Driver with I²C Interface

DESCRIPTION

The EUM6820 is a single 10-bit DAC with 100mA output current sink capability. It features an internal reference, I²C interface, 10 bits DAC and current sense resistor. The DAC is controlled via a 2-wire (I²C compatible) serial interface that operates at clock rates up to 400kHz. The EUM6820 can operates from 2.3V to 5.5V.

The EUM6820 incorporates a power-on reset circuit, which ensures that DAC output powers up to 0V and remains there until a valid write takes place. It has a power-down feature that reduces the current consumption of the device to 1μA maximum.

The EUM6820 principally designed for linear control of voice coil motors, targeting at autofocus, image stabilization, and optical zoom applications in camera phones , digital still cameras, and camcorders. While it may also used in many industrial applications, such as controlling temperature, light, and movement.

The I²C address for the EUM6820 is 0×18.

FEATURES

- 100mA current sink
- 2-wire (I²C-compatible) 1.8V serial interface
- 10-bit resolution DAC
- 2.3V to 5.5V power supply
- Guaranteed monotonic over all codes
- Power-down to 0.5μA typical
- Internal reference
- Current sense resistor integrated
- Power-down function
- Power-on reset
- Available in 1.0mm×1.5mm WCSP-6 package
- RoHS compliant and 100% lead (Pb)-free

APPLICATIONS

- Camera phones
- Digital still cameras
- Web/PC cameras
- Digital video cameras/camcorders
- Lens autofocus
- Lens covers
- Optical zoom
- Image stabilization
- Shutters
- Neutral density filters

Application Circuit

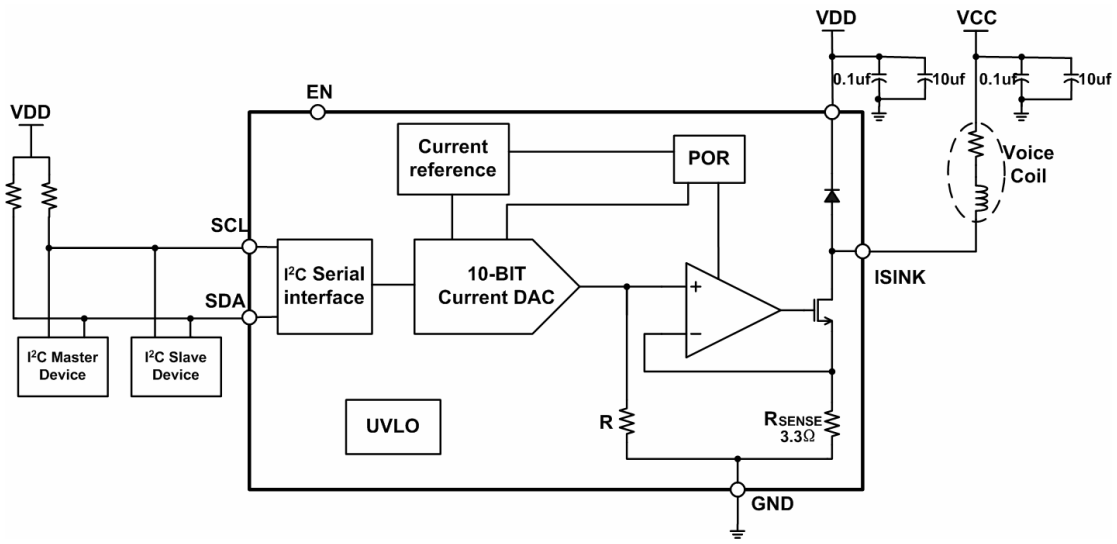
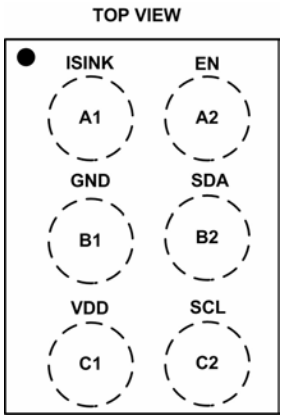


Figure 1. Application Circuit

Pin Configurations

Package Type	Pin Configurations
WCSP-6	

Pin Description

PIN	WCSP-6	DESCRIPTION
ISINK	A1	Output Current Sink
EN	A2	Enable Pin. Logic Hi enable the device, and logic low disable the device.
GND	B1	Ground
SDA	B2	I^2C Interface Signal (data)
VDD	C1	Power Supply
SCL	C2	I^2C Interface Signal (clock)

Block Diagram

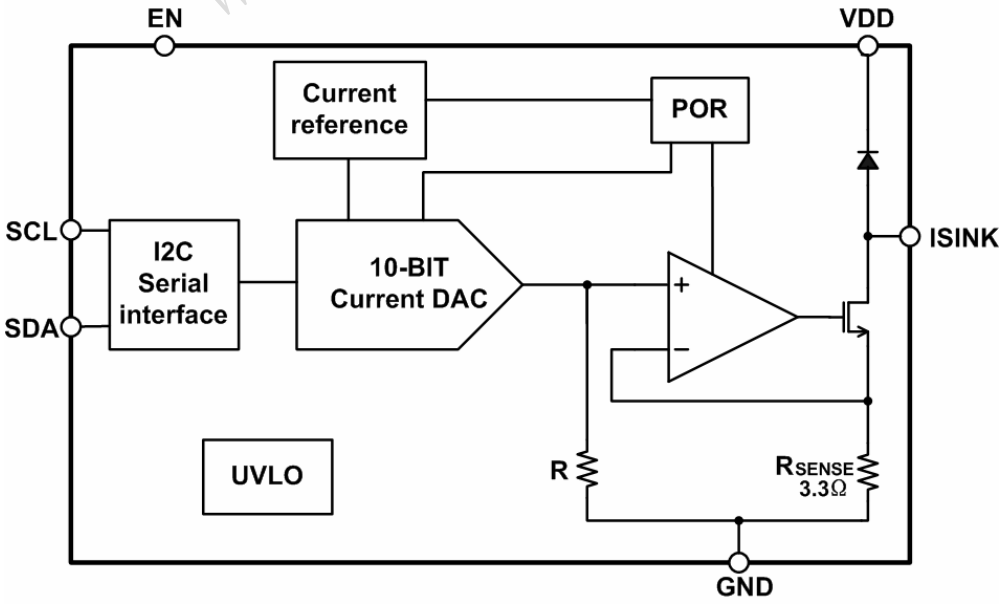
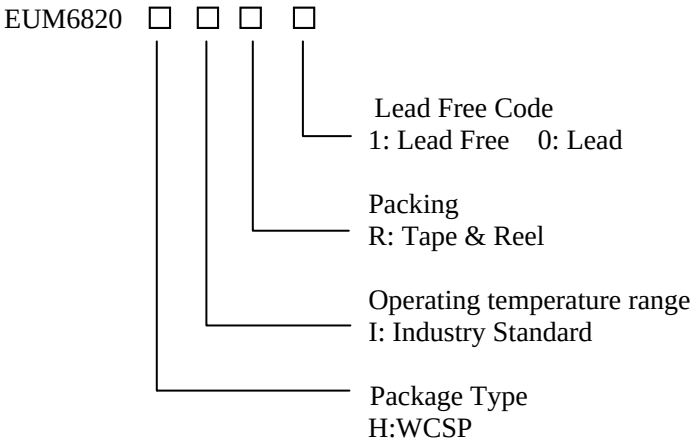


Figure 2. Block Diagram

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUM6820HIR1	WCSP-6	xxx D00	-40°C to +85°C



Absolute Maximum Ratings

- VDD ---------- –0.3V to +5.5V
- SCL, SDA ---------- –0.3V to VDD + 0.3V
- EN ---------- –0.3V to VDD + 0.3V
- ISINK Voltage ---------- –0.3V to VDD + 0.3V
- Operating Temperature Range ---------- −40°C to +85°C
- Storage Temperature Range ---------- −65°C to +150°C
- Junction Temperature ($T_{J\,MAX}$) ---------- 150°C

Electrical Characteristics

V_{DD} from 2.3V to 5.5V, load resistance R_L=25Ω connected to V_{DD}
Full operating temperature range (Ta from -40℃ to +85℃) unless otherwise noted.

Parameter	Symbol	Conditions	EUM6820			Unit
			Min.	Typ.	Max.	
Power Supply						
Power Supply Voltage	V_{DD}	V_{DD}=2.8V to 3.6V ; device operates over 2.3V to 5.5V with reduced performance	2.3		5.5	V
Operating Current	I_{DD}	V_{DD}=3.6V		0.16		mA
Power Down Current	ISD	@ Power Down Mode		0.5		μA
DC Characteristics						
Resolution		97.65μA/LSB		10		Bits
Relative Accuracy	INL			±1.5	±4	LSB
Differential Nonlinearity (1)	DNL	Guaranteed monotonic over all codes			±1	LSB
Zero Code Error		All 0s loaded to DAC	0	1	5	mA
Offset Error		@ Code 16		0.5		mA
Offset Error Drift (2)				10		μA/℃
Gain Error Drift (2)				±0.2	±0.5	LSB/℃
Output Characteristics						
Isink Min	Iomin			3		mA
Isink Max	Iomax			100		mA
Isink Xshutdown	Ioxd	Isink @ EN		80		nA
Output Compliance	OCMR	Output voltage range (Isink form 0mA to 100mA)	0.65		VDD	V
Power Up Time		VDD=5V To 10% of FS, coming out of power down mode		35		μS
Logic input of I^2C (2)						
Low Voltage	V_{INL}	VDD from 2.3V to 5.5V	-0.3		+0.54	V
High Voltage	V_{INH}	VDD from 2.3V to 5.5V	1.26		V_{DD}+0.3	V
Input Current	I_{IN}	VIN from 0V to VDD			±1	μA
Input Hysteresis	V_{HYST}		0.05V_{DD}			V
Input Capacitance	C_{IN}			6		pF
Glitch Rejection		Pulse Width of spike suppressed			50	nS
Logic Inputs of EN						
Low voltage	V_{INL}				0.54	V
High voltage	V_{INH}		1.3			V
Input Current	I_{IN}				±1	μA
Pin Capacitance				3		pF

Electrical Characteristics (continued)

V_{DD} from 2.3V to 5.5V, load resistance R_L=25Ω connected to V_{DD}
Full operating temperature range (Ta from -40℃ to +85℃) unless otherwise noted.

Parameter	Symbol	Conditions	EUM6820			Unit
			Min.	Typ.	Max.	
AC Characteristics						
Output Current Settling Time		V_{DD}=3.6V,R_L=25Ω,L_L=680μH, 30mA to 75mA change		250		μS
Slew Rate				1.8		mA/μS
Major Code Change Glitch Impulse		1 LSB change around major carry		0.15		nA-S
Digital Feedthrough				0.06		nA-S

Note: (1) Linearity is tested using a reduced code range: code 32 to code 1023.
(2) Guaranteed by design and characterization; not production tested. EN is active low.
SDA and SCL pull-up resistors are tied to 1.8V.

TYPICAL PERFORMANCE CHARACTERISTICS

Typical INL vs. Code Plot

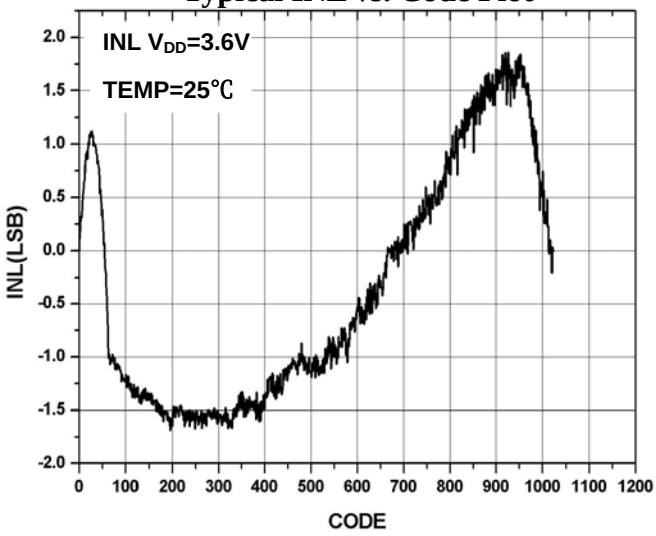


Figure 3.

Typical DNL vs. Code

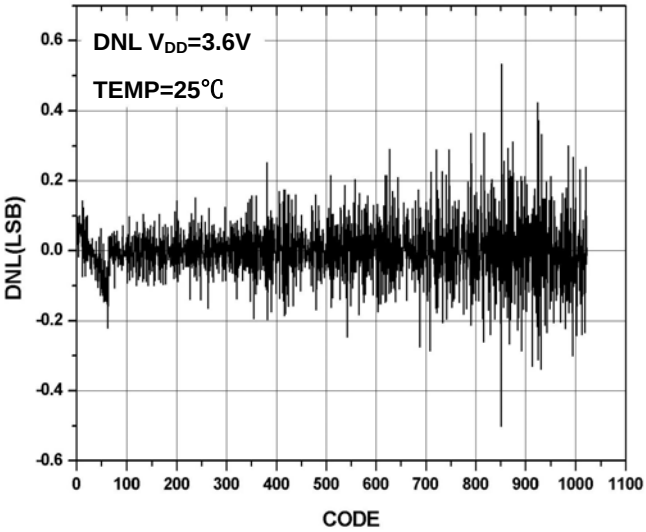


Figure 4.

1/4 to 3/4 Scale Settling Time

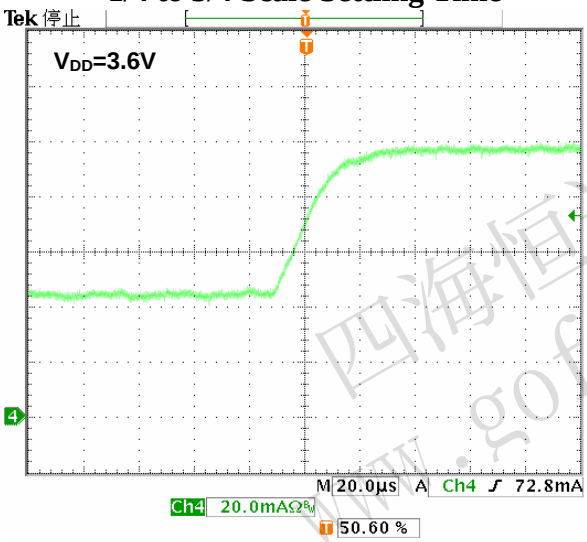


Figure 5.

Settling Time for a 100-LSB Step

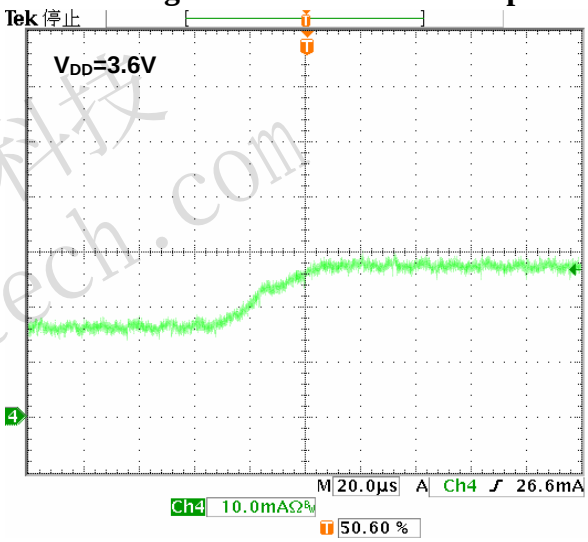


Figure 6.

Sink Current vs. Code vs. Temperature

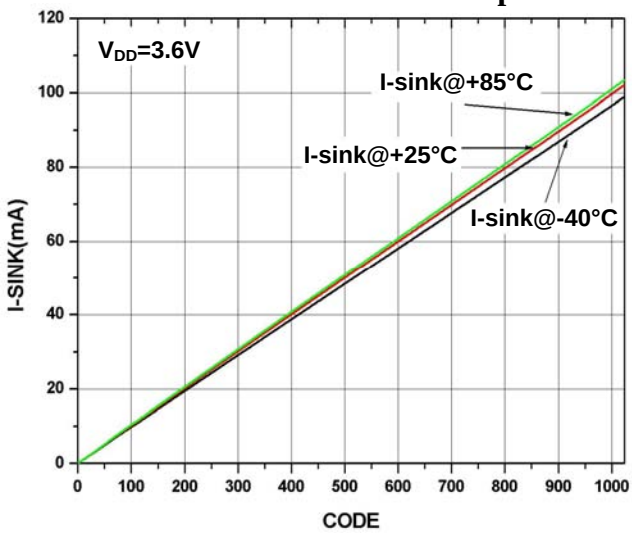


Figure 7.

INL vs. Temperature vs. Supply Voltage

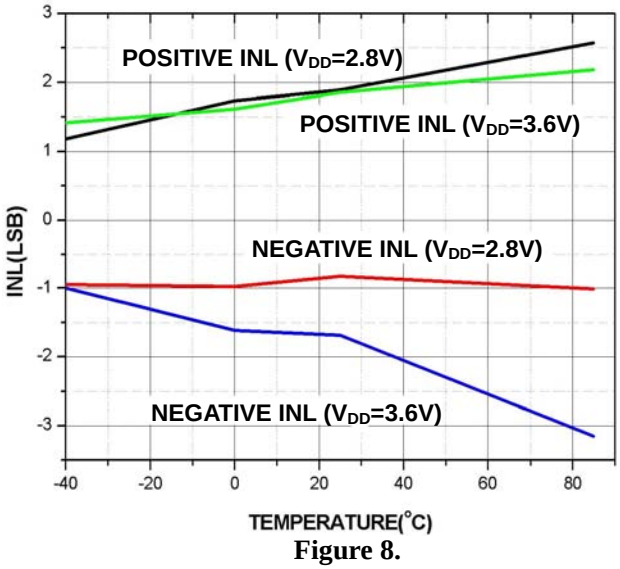


Figure 8.

DNL vs. Temperature vs. Supply Voltage

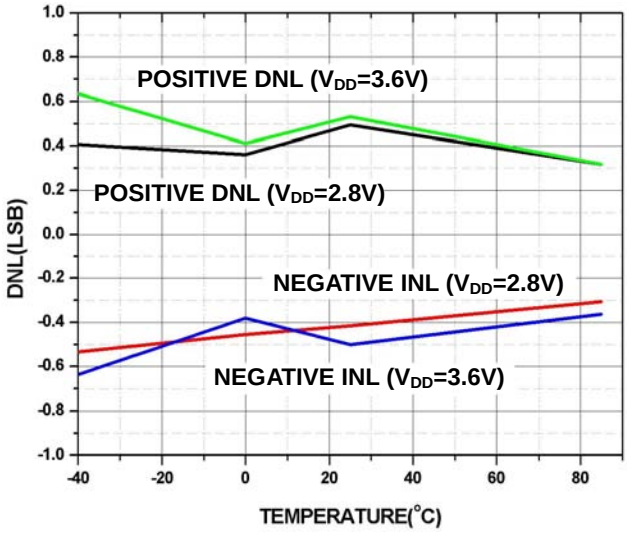


Figure 9.

Zero-Code Error vs. Supply Voltage vs. Temperature

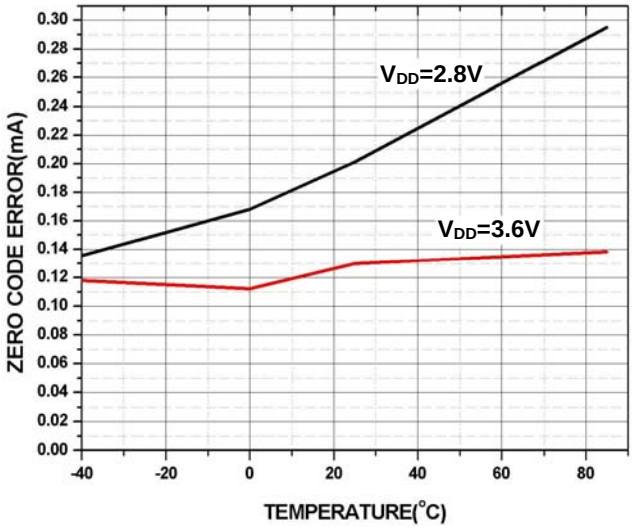


Figure 10.

Full-Scale Error vs. Temperature vs. Supply Voltage

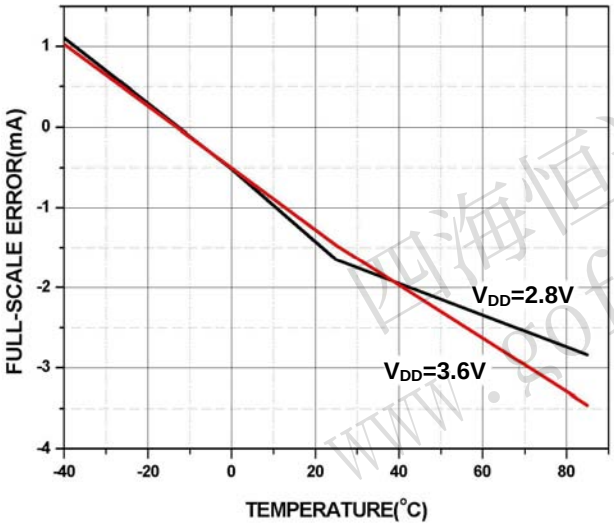


Figure 11.

TERMINOLOGY of EC Table

1. Relative Accuracy (INL)

   Relative accuracy (INL) is calculated by measuring the worse case deviation from a straight line which is defined from end points. The straight line end points are the actual measured values at 0 code and 1023 code.

$$INL_n = \frac{I_n - \left(\frac{I_{1023} - I_0}{1023} \times n + I_0\right)}{97.65\mu A}$$

$$INL = Max(INL_n) \qquad n = 0,.....,1023$$

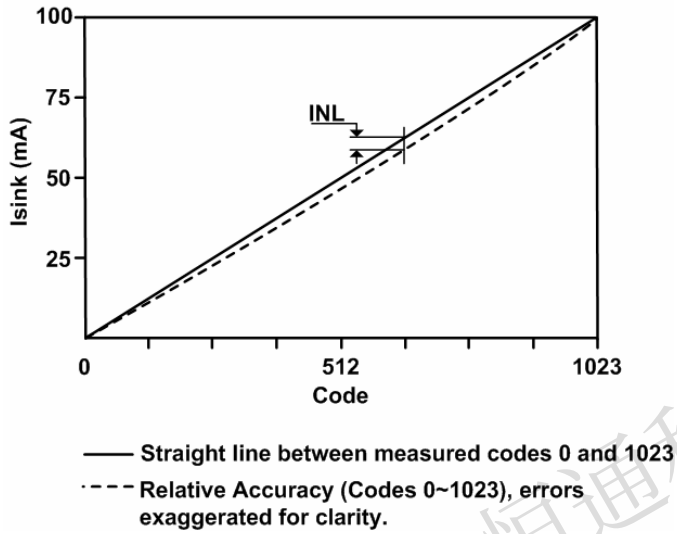


Figure 12. Relative Accuracy

2. Differential Nonlinearity (DNL)

   Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change of any two adjacent codes. The slope of the output line must be positive for each incremental step to guarante monotonic.

$$DNL_n = \frac{I_n - I_{n-1} - 97.65\mu A}{97.65\mu A}$$

$$DNL = Max(DNL_n) \qquad n = 33,.....,1023$$

3. Zero-Code Error

   Zero-code error is a measurement of Isink @ 0 code. Ideally, it is 0 mA.

4. Gain Error

   Gain error is the difference in the slopes of the ideal transfer function and the actual transfer function. It is expressed as a percent of the full-scale range

$$Gain\_Error = \frac{\frac{(I_{1023} - I_{16})}{1007} - \frac{0.1}{1023}}{\frac{0.1}{1023}} \times 1000‰$$

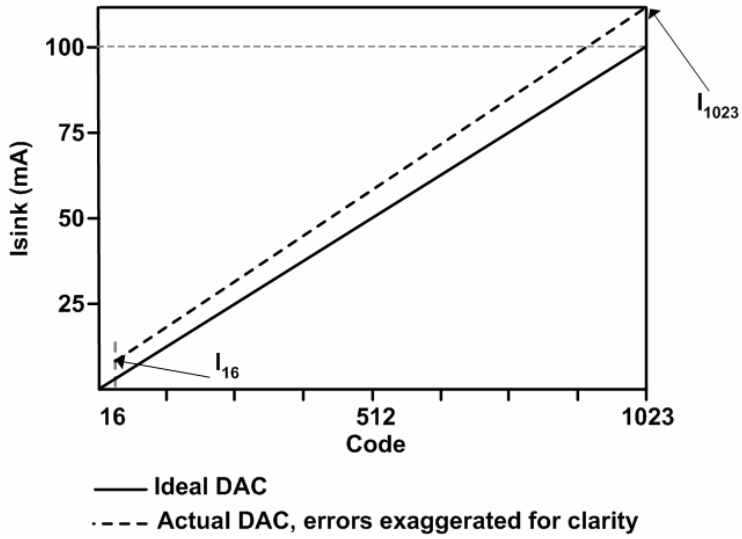


Figure 13. Gain Error

5. Gain Error Drift

The change in slope of the transfer function due to temperature, expressed as LSB/°C.

6. Offset Error

Offset error of EUM6820 is the difference between the actual I_{SINK} @ 16 code the ideal I_{SINK} @ 16 code.

7. Offset Error Drift

The change of offset error due to temperature, expressed as μV/°C.

Timing Specifications

V_{DD}=2.3V to 5.5V.

Full operating temperature range (Ta from -40℃ to 85℃) unless otherwise noted.

f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	μs min	SCL cycle time
t_2	0.6	μs min	t_{HIGH}, SCL high time
t_3	1.3	μs min	t_{LOW}, SCL low time
t_4	0.6	μs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6	0.9	μs max	$t_{HD, DAT}$, data hold time
	0	μs min	
t_7	0.6	μs min	$t_{SU, STA}$, setup time for repeated start
t_8	0.6	μs min	$t_{SU, STO}$, stop condition setup time
t_9	1.3	μs min	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}	300	ns max	$t_{R,}$ rise time of both SCL and SDA when receiving
	0	ns min	May be CMOS driven
t_{11}	250	ns max	t_F, fall time of SDA when receiving
	300	ns max	t_F, fall time of both SCL and SDA when transmitting
	20 + 0.1 C_{B3}	ns min	
C_B	400	pF max	Capacitive load for each bus line

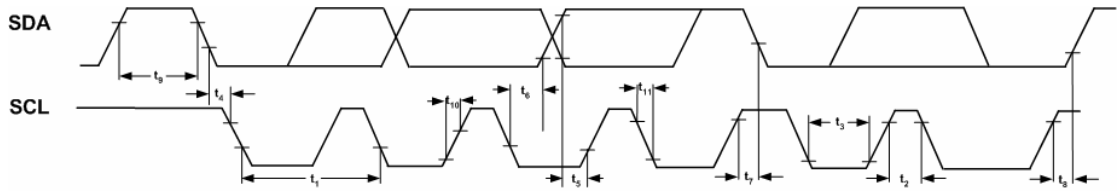


Figure 14. I²C Interface timing Diagram

SERIAL INTERFACE

EUM6820 uses I²C interface. System can write or read from data to DAC at the rates of up to 400 kHz.

I²C BUS OPERATION

This is a serial interface that uses two bus lines, SCL and SDA, to access the internal control registers. The master generates the serial clock (SCL) and reads/write data on the serial data line (SDA) from/to slave devices such as the EUM6820. All devices on an I²C bus have their SDA pin connected to the SDA line and their SCL pin connected to the SCL line of the master device. I²C devices can pull the bus lines low; but pulling high is only achieved by pull-up resistors, Rp. The value of Rp The value of Rp depends on the data rate, bus capacitance, and the maximum load current that the I²C device can sink (3 mA for a standard device).

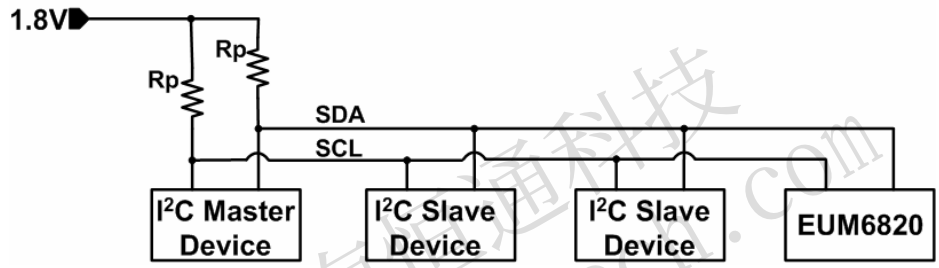


Figure 15. Typical I²C Bus

Rp will pull the bus lines (SCL and SDA) high when the bus is idle. The control sequence of the communication through the I²C interface is composed of several steps in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address: 7 bits of address, plus 1 bit to indicate write (0) or read (1), and an acknowledge bit.
   The write address of EUM6820 is 00011000 (0X18).
   The read address of EUM6820 is 00011001(0X19).
3. Data: Two blocks of eight bits will be written to EUM6820 when a write operation occurs, or read from it when a read operation occurs. At the end of a read or write operation, the EUM6820 acknowledges the second data bytes.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

SDA can only be changed while SCL is low but to indicate a Start or Stop condition. It is possible for the Start or Stop condition to occur at any time during a data transfer.

DATA FORMAT

High byte of the data is written to EUM6820 first, then the lower byte. After all data is shifted into the 16 bit input register, it will be transferred to the DAC register.

The MSB is reserved for an active-high, power-down function.

Bit 14 is unused.

Bit 13 to Bit 4 correspond to the 10-bit DAC data which controls the output current.

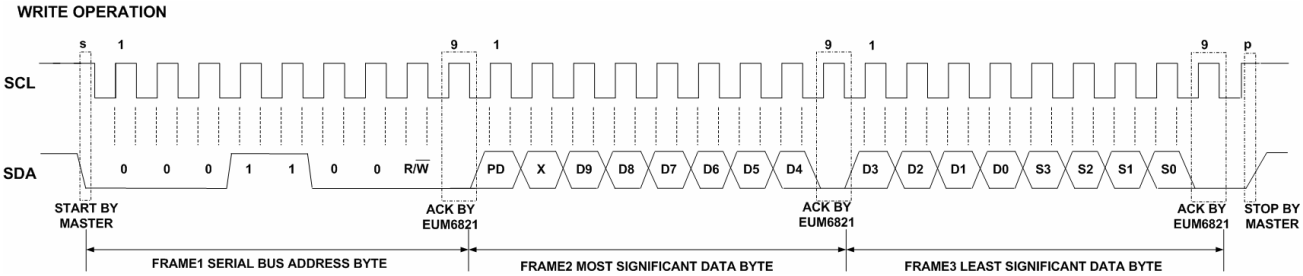


Figure 16. Write Operation

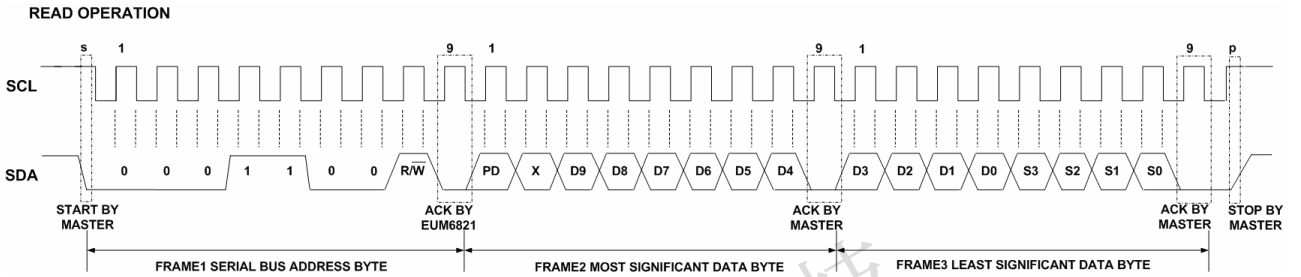


Figure 17. Read Operation

Table 1: Data Format

Bits	MSB								LSB							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Input Register	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
FUNC	PD	FL	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	S3	S2	S1	S0

Data is written to the EUM6820 high byte first, MSB first, and is shifted into the 16-bit input register. Until all data is shifted in, data from the input register is transferred to the DAC register.

Bit 15, the PD bit is a software power down enable. EUM6820 output is disabled and the chip goes into shut-down mode, when PD is set to high.

Bit 14 is unused;

Bit 13 to Bit 4 correspond to the 10 bits DAC data, B9 to B0.

Power Supply Bypassing And Grounding

Decouple the power supply of EUM6820. A tantalum bead type capacitor of 10μF between VDD and GND to decouple the power supply is recommended. A 0.1μF(or more) ceramic capacitor is needed to provide a low impedance path to ground for high transient currents. This ceramic capacitor should be put as close as possible to the VDD pin and should has a low effective series resistance and effective series inductance.

The power supply line should be large enough to provide a low impedance path and reduce glitch effects on the supply line.

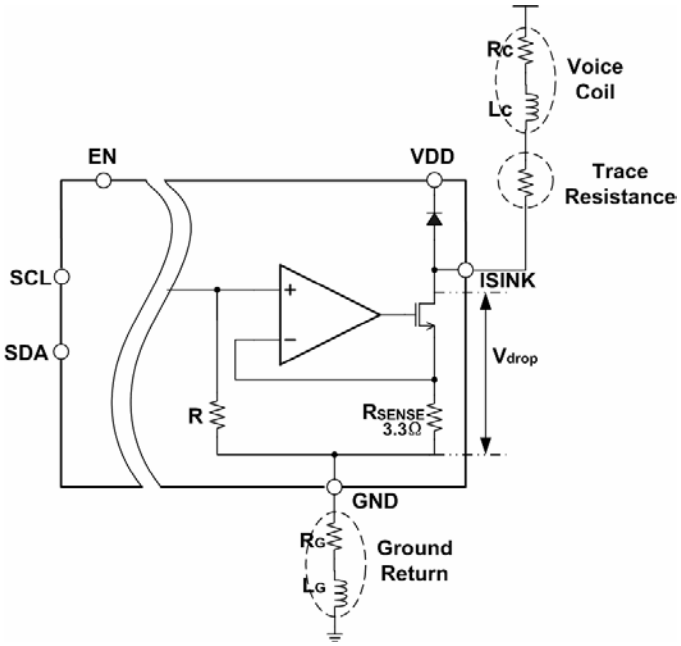


Figure 18. Effect of PCB Trace Resistance and Inductance.

Output Compliance Voltage

The output NMOS of EUM6820 need work in the propriety operation region to make I_{SINK} accurate. A incorrect voltage of I_{SINK} Pin will cause I_{SINK} operate impropriety and I_{SINK} may not be maintained as a constant.
If I_{SINK} is 100mA, the minimum VDS of output NMOS should be 200mV and the voltage drop across R_{SENSE} is 330mV. So, the output compliance voltage of EUM6820 is 530mV @ 100mA. If I_{SINK} Pin voltage is below 550mV, I_{SINK} will become smaller and no longer be 100mA.
If I_{SINK} is 90mA, the minimum VDS of output NMOS should be 180mV and the voltage drop across R_{SENSE} is 297mV. So, the output compliance voltage of EUM6820 is 480mV @ 90mA. If I_{SINK} Pin voltage is below 480mV, I_{SINK} will become smaller and no longer be 90mA.
Because the parasitic resistor of PCB will effect the output compliance voltage drop, special attention should be paid to the layout of the GND and the layout of the path between voice coil motor and I_{SINK} Pin to minimize series resistance. Also, the parasitic resistor of voice coil motor should be choosed exactly to make I_{SINK} correct and constant.
If I_{SINK} is 100mA, the RC of VCM should be smaller than the value calculated as below,

$$R_C \le \frac{V_{BAT} - [V_{DROP} + (I_{SINK} \times R_T) + (I_{SINK} \times R_G)]}{I_{SINK}} = \frac{V_{BAT} - [550mV + 100mA \times (R_T + R_G)]}{100mA}$$

If ISINK is 90mA, The RC of VCM should be smaller than the value calculated as below,

$$R_C \le \frac{V_{BAT} - [V_{DROP} + (I_{SINK} \times R_T) + (I_{SINK} \times R_G)]}{I_{SINK}} = \frac{V_{BAT} - [480mV + 90mA \times (R_T + R_G)]}{90mA}$$

Applications Information

EUM6820 can drive spring-preloaded motor or nonspring linear motors. These motors are applied in applications such as lens auto-focus, optical zoom and so on. Spring-preloaded motor is controlled by the balancing of a voice coil and spring.If voice coil current increases, the strength of voice coil increases and the motor moves to a certain direction. During the motor moving, the strength of spring increases and finally be equated with the coil strength. When balance of these to strength are achieved, motor stop moving.On the contrary, If voice coil current decreases, the strength of voice coil decreases and the motor moves to a opposite direction. During the motor moving, the strength of spring decreases and finally be equated with the coil strength. Then motor stop moving. Figure 10 is transfer curve of a certain spring preloaded motor for autofocus. A start (or threshold) current of TPY 20mA is needed to move the moror because the strength of spring is not zero at 0mm. The current sink capability of EUM6820 is up to 100 mA and more than adequate

for available commercial linear motors or voice coils. EUM6820 guarantees monotonicity at all codes. This makes the EUM6820 the ideal solution for applications of auto focus and lens positioning.

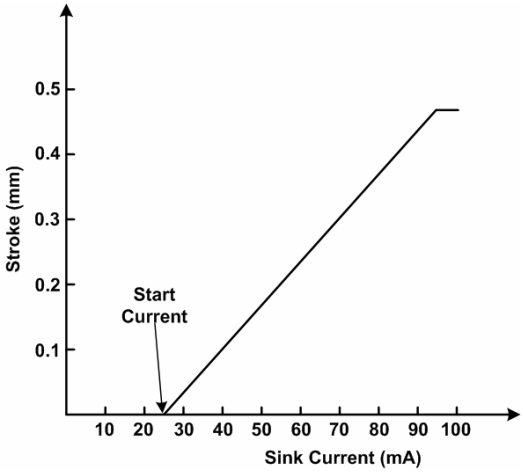
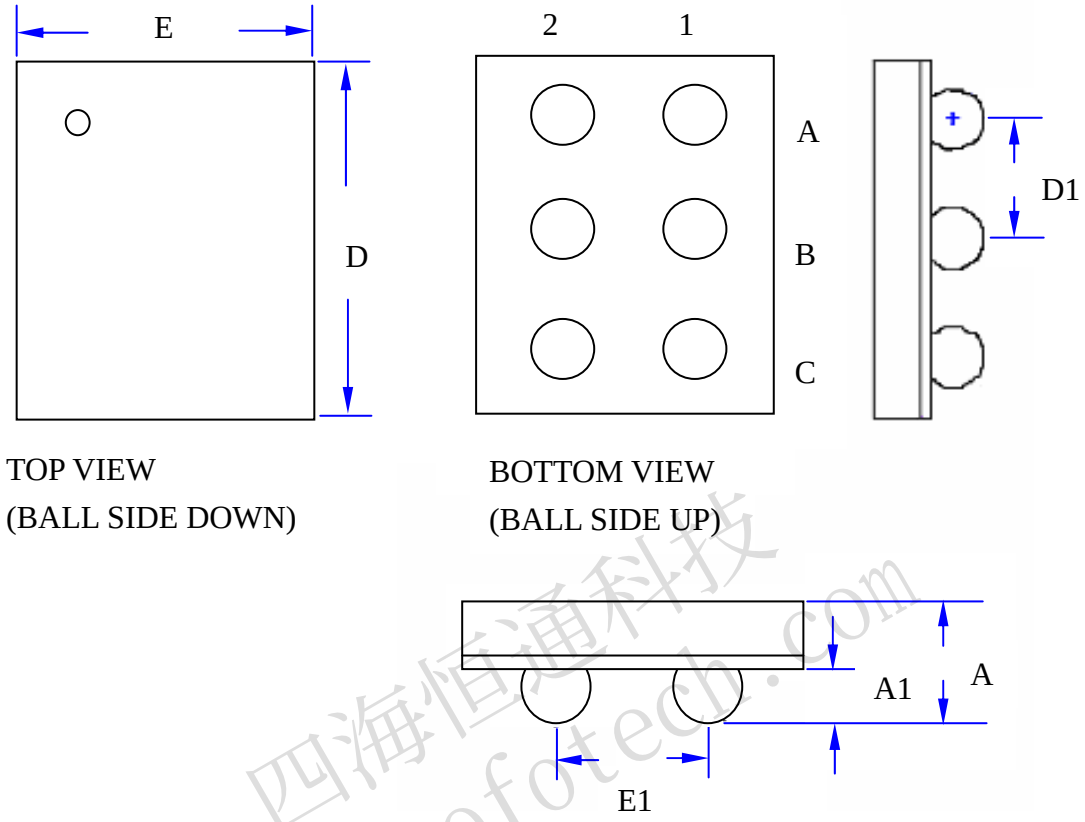


Figure 19.Voice Coil Stroke vs. Isink Current

Packaging Information

WCSP-6



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	0.675	-	0.027
A1	0.15	0.35	0.006	0.014
D	1.45	1.55	0.057	0.061
D1	0.50		0.020	
E	0.95	1.05	0.037	0.041
E1	0.50		0.020	