





## Functional description

The AS7C33256NTD16A/18A family is a high performance CMOS 4-Mbit synchronous Static Random Access Memory (SRAM) organized as 262,144 words × 16 or 18 bits and incorporates a LATE LATE Write.

This variation of the 4Mb synchronous SRAM uses the No Turnaround Delay (NTD) architecture, featuring an enhanced Write operation that improves bandwidth over pipelined burst devices. In a normal pipelined burst device, the write data, command, and address are all applied to the device on the same clock edge. If a Read command follows this Write command, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or Read-Modify-Write operations.

NTD devices use the memory bus more efficiently by introducing a write latency that matches the two-cycle pipelined or one-cycle flow-through read latency. Write data is applied two cycles after the Write command and address, allowing the Read pipeline to clear. With NTD, Write and Read operations can be used in any order without producing dead bus cycles.

Assert  $R/\overline{W}$  low to perform Write cycles. Byte Write enable controls write access to specific bytes, or it can be tied low for full 16/18 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable  $\overline{OE}$  does not need to be toggled for write operations. It can be tied low for normal operations. Outputs go to a high impedance state when the device is deselected by any of the three chip enable inputs. In pipelined mode, a two-cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read, write, and deselect operations. When ADV is high, external addresses, chip select, and  $R/\overline{W}$  pins are ignored, and internal address counters increment in the count sequence specified by the  $\overline{LBO}$  control. Any device operations, including burst, can be stalled using the clock enable input  $\overline{CEN}=1$ .

The AS7C33256NTD18A and AS7C33256NTD16A operate with a  $3.3V \pm 5\%$  power supply for the device core ( $V_{DD}$ ). DQ circuits use a separate power supply ( $V_{DDQ}$ ) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin 14×20 mm TQFP package.

## Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	Address and control pins	$V_{in} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	$V_{in} = V_{out} = 0V$	7	pF

## Burst order

	Interleaved burst order $\overline{LBO} = 1$					Linear burst order $\overline{LBO} = 0$			
<b>Starting address</b>	00	01	10	11	<b>Starting address</b>	00	01	10	11
<b>First increment</b>	01	00	11	10	<b>First increment</b>	01	00	11	10
<b>Second increment</b>	10	11	00	01	<b>Second increment</b>	10	11	00	01
<b>Third increment</b>	11	10	01	10	<b>Third increment</b>	11	10	01	10



## Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ , FT, $\overline{LBO}$ , and ZZ are synchronous to this clock.
$\overline{CEN}$	I	SYNC	Clock enable. When de-asserted high, the clock input signal is masked.
A, A0, A1	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADV}/\overline{LD}$ is asserted.
DQ[a,b]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$ , CE1, CE2	I	SYNC	Synchronous chip enables. Sampled at the rising edge of CLK, when $\overline{ADV}/\overline{LD}$ is asserted. Are ignored when $\overline{ADV}/\overline{LD}$ is high.
$\overline{ADV}/\overline{LD}$	I	SYNC	Advance or Load. When sampled high, the internal burst address counter will increment in the order defined by the $\overline{LBO}$ input value. (refer to table on page 2) When low, a new address is loaded.
R/W	I	SYNC	A high during LOAD initiates a READ operation. A low during LOAD initiates a WRITE operation. Is ignored when $\overline{ADV}/\overline{LD}$ is high.
$\overline{BW}[a,b]$	I	SYNC	Byte write enables. Used to control write on individual bytes. Sampled along with WRITE command and BURST WRITE.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are not driven when $\overline{OE}$ is inactive.
$\overline{LBO}$	I	STATIC	Count mode. When driven high, count sequence follows Intel XOR convention. When driven low, count sequence follows linear convention. This input should be static when the device is in operation.
FT	I	STATIC	Flow-through mode. When low, enables single register flow-through mode. Connect to $V_{DD}$ if unused or for pipelined operation.
ZZ	I	ASYNC	Snooze. Places device in low power mode. Data is retained. Connect to GND if unused.
NC	-	-	No connects. Note that pin 83 and 84 will be used for future address expansion to 8Mb and 16Mb density.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	$V_{DD}$ , $V_{DDQ}$	-0.5	+4.6	V
Input voltage relative to GND (input pins)	$V_{IN}$	-0.5	$V_{DD} + 0.5$	V
Input voltage relative to GND (I/O pins)	$V_{IN}$	-0.5	$V_{DDQ} + 0.5$	V
Power dissipation	$P_D$	-	1.8	W
DC output current	$I_{OUT}$	-	50	mA
Storage temperature (plastic)	$T_{stg}$	-65	+150	°C
Temperature under bias (Junction)	$T_{bias}$	-65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.



### Synchronous truth table

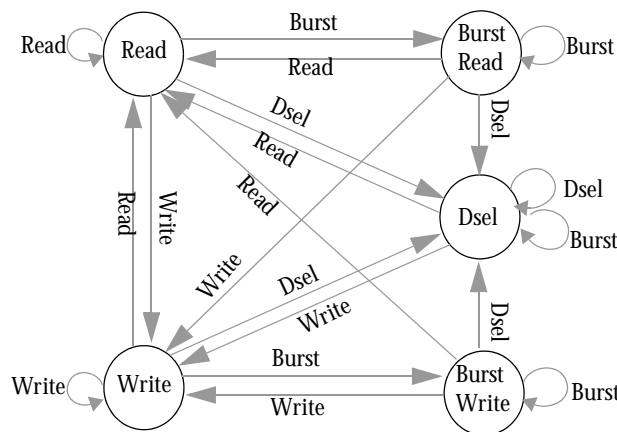
CE0	CE1	CE2	ADV/LD	R/W	BW[a,b]	OE	CEN	Address source	CLK	Operation
H	X	X	L	X	X	X	L	NA	L to H	Deselect, high-Z
X	L	X	L	X	X	X	L	NA	L to H	Deselect, high-Z
X	X	H	L	X	X	X	L	NA	L to H	Deselect, high-Z
L	H	L	L	H	X	X	L	External	L to H	Begin read
L	H	L	L	L	L	X	L	External	L to H	Begin write
X	X	X	H	X	X <sup>1</sup>	X	L	Burst counter	L to H	Burst <sup>2</sup>
X	X	X	X	X	X	X	H	Stall	L to H	Inhibit the CLK

Key: X = don't care. L = low. H = high.

1. Should be low for Burst write, unless a specific byte needs to be inhibited

2. Refer to state diagram below.

### State Diagram for NTD SRAM



### TQFP thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (Junction to Ambient) <sup>1</sup>	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	1-layer	$\theta_{JA}$	40	°C/W
		4-layer	$\theta_{JA}$	22	°C/W
Thermal resistance (Junction to Top of Case) <sup>1</sup>			$\theta_{JC}$	8	°C/W

<sup>1</sup> This parameter is sampled.



### Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		$V_{DD}$	3.135	3.3	3.465	V
		GND	0.0	0.0	0.0	V
3.3V I/O supply voltage		$V_{DDQ}$	3.135	3.3	3.465	V
		$GND_Q$	0.0	0.0	0.0	
2.5V I/O supply voltage		$V_{DDQ}$	2.35	2.5	2.65	V
		$GND_Q$	0.0	0.0	0.0	
Input voltages <sup>1</sup>	Address and control pins	$V_{IH}$	2.0	–	$V_{DD} + 0.3$	V
		$V_{IL}$	$-0.5^2$	–	0.8	V
	I/O pins	$V_{IH}$	2.0	–	$V_{DDQ} + 0.3$	V
		$V_{IL}$	$-0.5^2$	–	0.8	
Ambient operating temperature		$T_A$	0	–	70	°C

1 Input voltage ranges apply to 3.3V I/O operation. For 2.5V operation, contact factory for input specifications.

2  $V_{IL}$  min = -2.0V for pulse width less than  $0.2 \times t_{RC}$ .

### DC electrical characteristics for 3.3V I/O operation

Parameter	Symbol	Test conditions	166		133		100		Unit
			Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} ^1$	$V_{DD} = \text{Max}, V_{in} = \text{GND to } V_{DD}$	–	2	–	2	–	2	μA
Output leakage current	$ I_{LO} $	$\overline{OE} \geq V_{IH}, V_{DD} = \text{Max}, V_{out} = \text{GND to } V_{DD}$	–	2	–	2	–	2	μA
Operating power supply current	$I_{CC}^2$	$\overline{CE} = V_{IL}, CE = V_{IH}, \overline{CE} = V_{IL}, f = f_{max}, I_{out} = 0 \text{ mA}$	–	450	–	425	–	325	mA
Standby power supply current	$I_{SB}$	Deselected, $f = f_{max}$	–	110	–	100	–	90	mA
	$I_{SB1}$	Deselected, $f = 0$ , all $V_{IN} \leq 0.2V$ or $\geq V_{DD} - 0.2V$	–	30	–	30	–	30	mA
	$I_{SB2}$	Deselected, $f=f_{Max}, ZZ \geq V_{DD} - 0.2V$ All $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$	–	30	–	30	–	30	mA
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{DDQ} = 3.6V$	–	0.4	–	0.4	–	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{DDQ} = 3.0V$	2.4	–	2.4	–	2.4	–	V

1 IBO pin has an internal pull-up, and input leakage = ±10 μA.

2  $I_{CC}$  given with no output loading.  $I_{CC}$  increases with faster cycle times and greater output loading

### DC electrical characteristics for 2.5V I/O operation

Parameter	Symbol	Test conditions	166		133		100		Unit
			Min	Max	Min	Max	Min	Max	
Output leakage current	$ I_{LO} $	$\overline{OE} \geq V_{IH}, V_{DD} = \text{Max}, V_{out} = \text{GND to } V_{DD}$	-1	1	-1	1	-1	1	μA
Output voltage	$V_{OL}$	$I_{OL} = 2 \text{ mA}, V_{DDQ} = 2.65V$	–	0.7	–	0.7	–	0.7	V
	$V_{OH}$	$I_{OH} = -2 \text{ mA}, V_{DDQ} = 2.35V$	1.7	–	1.7	–	1.7	–	



### Timing characteristics over operating range

Parameter	Symbol	166		133		100		Unit	Notes <sup>1</sup>
		Min	Max	Min	Max	Min	Max		
Clock frequency	F <sub>MAX</sub>	-	166	-	133	-	100	MHz	
Cycle time (pipelined mode)	t <sub>CYC</sub>	6	-	7.5	-	10	-	ns	
Cycle time (flow-through mode)	t <sub>CYCF</sub>	10	-	12	-	12	-	ns	
Clock access time (pipelined mode)	t <sub>CD</sub>	-	3.5	-	4.0	-	5.0	ns	
Clock access time (flow-through mode)	t <sub>CDF</sub>	-	9	-	10	-	12	ns	
Output enable low to data valid	t <sub>OE</sub>	-	3.5	-	4.0	-	5.0	ns	
Clock high to output low Z	t <sub>LZC</sub>	0	-	0	-	0	-	ns	2,3,4
Data output invalid from clock high	t <sub>OH</sub>	1.5	-	1.5	-	1.5	-	ns	4
Output enable low to output low Z	t <sub>LZOE</sub>	0	-	0	-	0	-	ns	2,3,4
Output enable high to output high Z	t <sub>HZOE</sub>	-	3.5	-	4.0	-	4.5	ns	2,3,4
Clock high to output high Z	t <sub>HZC</sub>	-	3.5	-	4.0	-	4.5	ns	2,3,4
Clock high to output high Z	t <sub>HZCN</sub>	-	1.5	-	2.0	-	2.5	ns	5
Clock high pulse width	t <sub>CH</sub>	2.4	-	2.5	-	3.0	-	ns	6,7
Clock low pulse width	t <sub>CL</sub>	2.2	-	2.5	-	3.0	-	ns	6
Address setup to clock high	t <sub>AS</sub>	1.5	-	1.5	-	1.5	-	ns	7
Data setup to clock high	t <sub>DS</sub>	1.5	-	1.5	-	1.5	-	ns	7
Write setup to clock high	t <sub>WS</sub>	1.5	-	1.5	-	1.5	-	ns	7
Chip select setup to clock high	t <sub>CSS</sub>	1.5	-	1.5	-	1.5	-	ns	7
Clock enable setup to clock high	t <sub>CENS</sub>	1.5	-	1.5	-	1.5	-	ns	7
ADV setup to clock high	t <sub>ADVS</sub>	1.5	-	1.5	-	1.5	-	ns	7
Address hold from clock high	t <sub>AH</sub>	0.5	-	0.5	-	0.5	-	ns	7
Data hold from clock high	t <sub>DH</sub>	0.5	-	0.5	-	0.5	-	ns	7
Write hold from clock high	t <sub>WH</sub>	0.5	-	0.5	-	0.5	-	ns	7
Chip select hold from clock high	t <sub>CSH</sub>	0.5	-	0.5	-	0.5	-	ns	7
Clock enable hold from clock high	t <sub>CENH</sub>	0.5	-	0.5	-	0.5	-	ns	7
ADV hold from clock high	t <sub>ADVH</sub>	0.5	-	0.5	-	0.5	-	ns	7

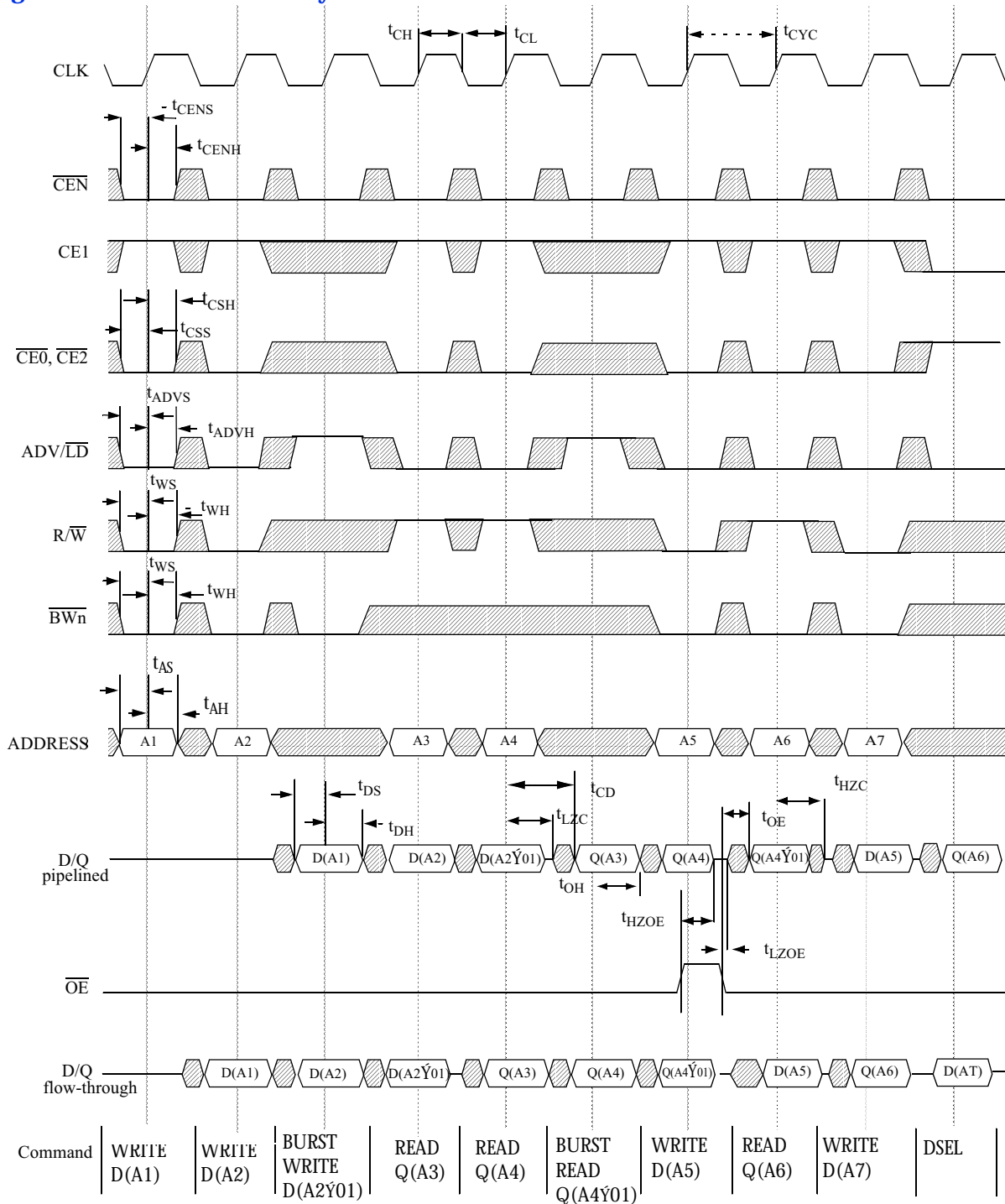
<sup>1</sup> See "Notes" on page 9



Key to waveform

▨ Undefined output/don't care

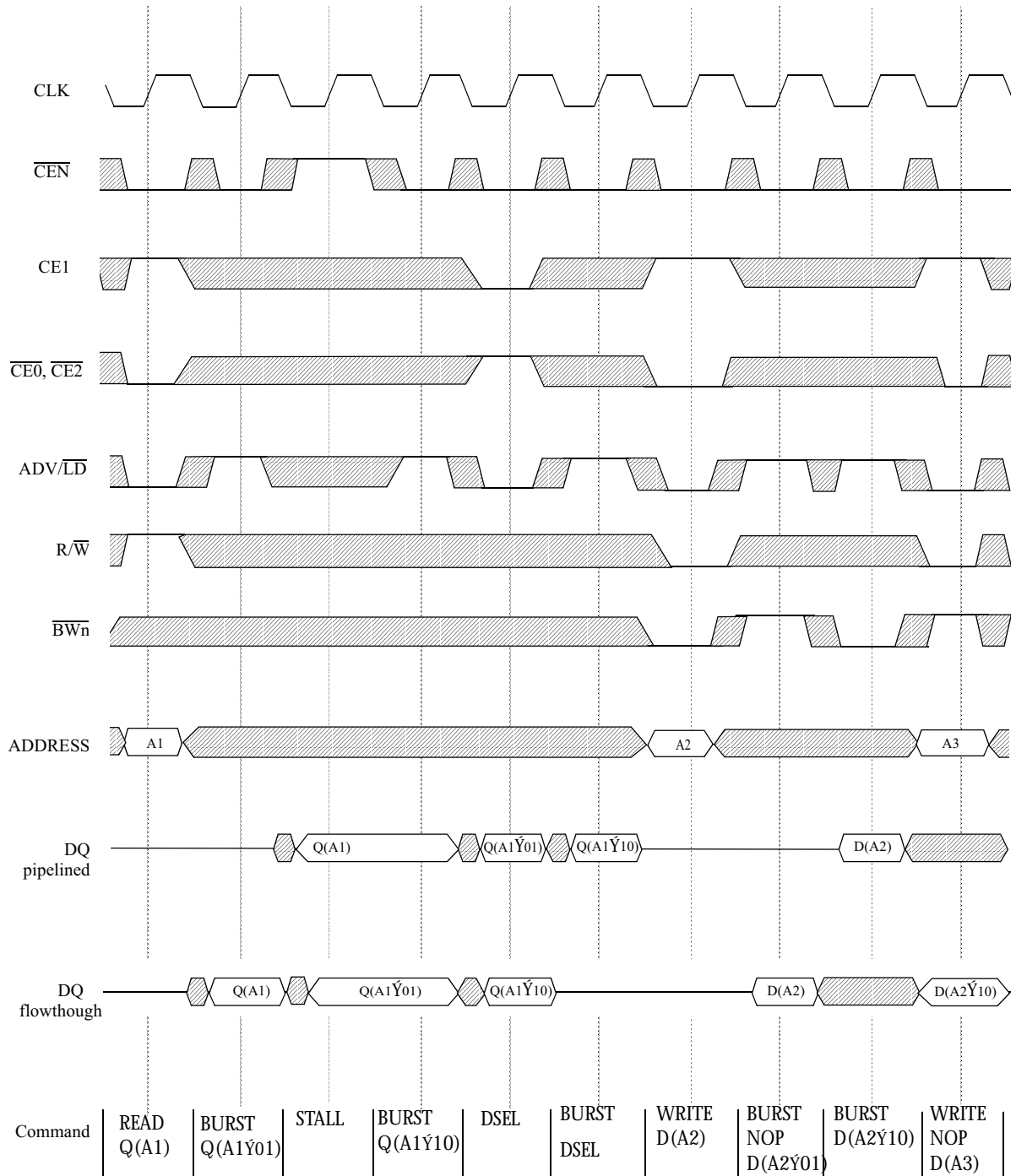
Timing waveform of read/write cycle



Note:  $\dot{Y}$  = XOR when  $\overline{LB0}$  = high/no connect.  $\dot{Y}$  = ADD when  $\overline{LB0}$  = low.  
 $\overline{BW[a:b]}$  is don't care.



**NOP, stall and deselect cycles**



Note:  $\overline{OE}$  is low.





### AC test conditions

- Output Load: For  $t_{LZC}$ ,  $t_{LZO\bar{E}}$ ,  $t_{HZO\bar{E}}$ ,  $t_{HZC}$ , see Figure C. For all others, see Figure B.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

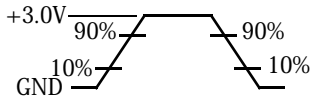


Figure A: Input waveform

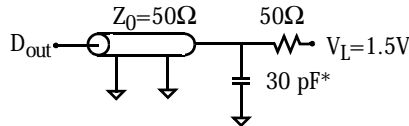


Figure B: Output load (A)

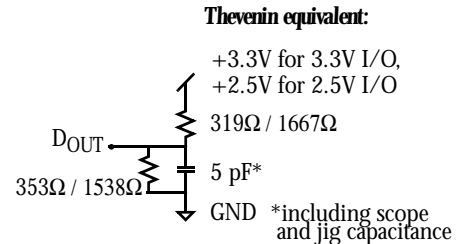


Figure C: Output load (B)

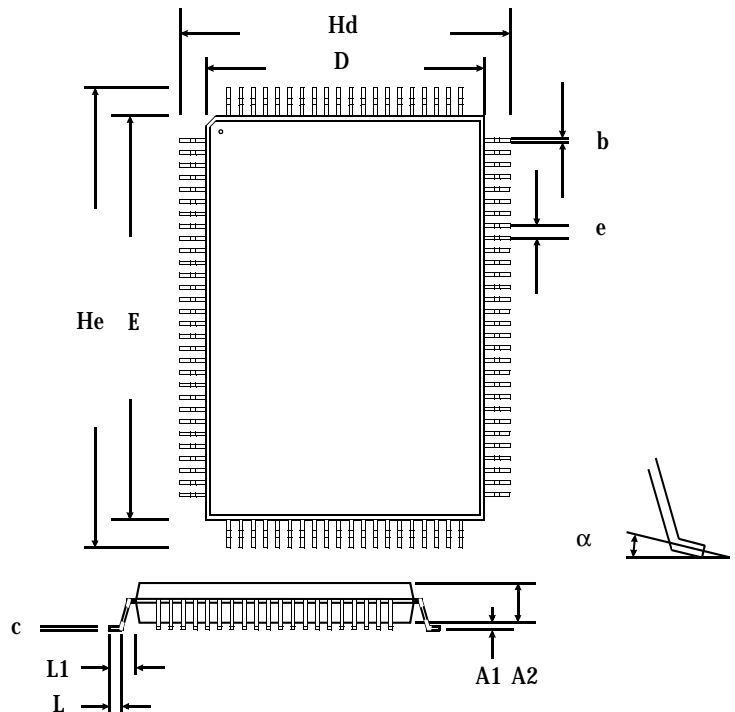
**Notes:**

- 1 For test conditions, see AC Test Conditions, Figures A, B, and C.
- 2 This parameter measured with output load condition in Figure C
- 3 This parameter is sampled and not 100% tested.
- 4  $t_{HZO\bar{E}}$  is less than  $t_{LZO\bar{E}}$  and  $t_{HZC}$  is less than  $t_{LZC}$  at any given temperature and voltage.
- 5  $t_{HZCN}$  is a no-load parameter to indicate exactly when SRAM outputs have stopped driving
- 6  $t_{CH}$  measured as high above  $V_{IH}$ , and  $t_{CL}$  measured as low below  $V_{IL}$
- 7 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.

### Package dimensions: 100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
<b>A1</b>	0.05	0.15
<b>A2</b>	1.35	1.45
<b>b</b>	0.22	0.38
<b>c</b>	0.09	0.20
<b>D</b>	13.90	14.10
<b>E</b>	19.90	20.10
<b>e</b>	0.65 nominal	
<b>Hd</b>	15.90	16.10
<b>He</b>	21.90	22.10
<b>L</b>	0.45	0.75
<b>L1</b>	1.00 nominal	
<b>a</b>	0°	7°

Dimensions in millimeters





## Ordering information

Package	Width	166 MHz	133 MHz	100 MHz
TQFP	×16	AS7C33256NTD16A-166TQC	AS7C33256NTD16A-133TQC	AS7C33256NTD16A-100TQC
TQFP	×16	AS7C33256NTD16A-166TQI	AS7C33256NTD16A-133TQI	AS7C33256NTD16A-100TQI
TQFP	×18	AS7C33256NTD18A-166TQC	AS7C33256NTD18A-133TQC	AS7C33256NTD18A-100TQC
TQFP	×18	AS7C33256NTD18A-166TQI	AS7C33256NTD18A-133TQI	AS7C33256NTD18A-100TQI

## Part numbering guide

AS7C	33	256	NTD	16/18	A	-XXX	TQ	C/I
1	2	3	4	5	6	7	8	9

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 33 = 3.3V
3. Organization: 256 = 256K
4. NTD = No Turnaround Delay
5. Organization: 16 = x16, 18 = x18
6. Production version: A = first production version
7. Clock speed (MHz)
8. Package type: TQ = TQFP
9. Operating temperature: C = commercial (0° C to 70° C). I = industrial (-40° C to 85° C)