INTERNATIONAL RECTIFIER IOR

160PFT & 160PFT-A SERIES

600 and 700A I_{TGQ} Gate Turn-Off Hockey Puk SCRs

Major Ratings and Characteristics

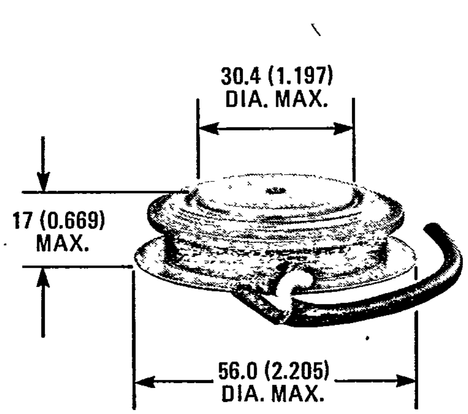
	160PFT100 160PFT120	160PFT100A 160PFT120A	160PFT140 & 160	Units
I_{TGQ}	600	700	600	A
$I_{T(RMS)}$	250		250	A
$I_{T(AV)}$	160		160	A
@ Max. T_C	88		79	°C
I_{TSM} @ 50 Hz	2500		2000	A
@ 60 Hz	2600		2100	
I^2t @ 50 Hz	31,000		20,000	A^2s
@ 60 Hz	28,500		18,000	
I_{GT}	1.0		1.2	A
dv/dt	1000		1000	V/µs
di/dt	600		600	A/µs
t_{gq}	8.0		8.0	µs
T_J	-40 to 125		-40 to 125	°C
V_{RRM}, V_{DRM}	1000 and 1200		1400 and 1600	V

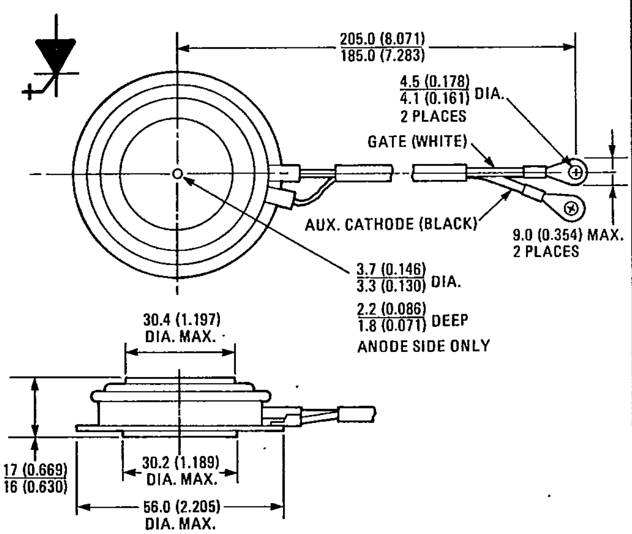
Description/Features

The 160PFT and 160PFT-A Series of GTO (gate turn-off) thyristors is designed for power control applications such as uninterruptible power supplies (UPS), variable speed ac motor drives, etc. Since they can be turned off by a negative current pulse to the gate, devices in the 160PFT and 160PFT-A Series allow reductions in overall size, weight, cost and acoustical noise when compared to conventional thyristors that require bulky commutating circuits.

- 160A average current.
- 600A or 700A controllable on-state current.
- Maximum turn-off time of 8 µsec.
- Critical dv/dt of 1000 V/µsec.
- Available with maximum repetitive peak off-state voltage (V_{DRM}) to 1600V.

CASE STYLE AND DIMENSIONS





IR Case Style A-30
Dimensions in Millimeters and (Inches)

160PFT & 160PFT-A Series

VOLTAGE RATINGS ①

Part Number	V_{RRM}, V_{DRM} – Max. Repetitive Peak Reverse and Off-State Voltage (V) T_J = -40°C to 125°C	V_{RSM}, V_{DSM} – Max. Non-Repetitive Peak Reverse and Off-State Voltage $t_p \leqslant$ 5 ms (V) T_J = 25°C to 125°C
160PFT100,A	1000	1200
160PFT120,A	1200	1400
160PFT140	1400	1600
160PFT160	1600	1750

ELECTRICAL SPECIFICATIONS

		160PFT100 160PFT120	160PFT100A 160PFT120A	160PFT140 160PFT160	Units	Conditions
ON-STATE						
$I_{T(RMS)}$	Nominal RMS on-state current	250	250	250	A	
$I_{T(AV)}$	Max. average on-state current	160	160	160	A	180° half sine wave conduction.
	@ Max. T_C	88	88	79	°C	
I_{TGQ}	Max. controllable peak on-state current	600	700	600	A	T_J = 125°C, V_{DM} = 0.5 V_{DRM}, G_{GQ} = 5, ② C_S = 2 μF. Note: $V_S \leqslant$ 400V @ T_J = 25°C, $V_S \leqslant$ 350V @ T_J = 125°C (160PFT100 & 120,A), $V_S \leqslant$ 450V @ T_J = 25°C, $V_S \leqslant$ 400V @ T_J = 125°C (160PFT140 & 160). (V_S is the voltage spike which appears on the dynamic on-state voltage trace during fall time.)
I_{TSM}	Max. peak one cycle, non-repetitive surge current	2500	2500	2000	A	50 Hz half cycle sine wave or 6 ms rectangular pulse. Following any rated load condition, and with rated V_{RRM} applied following surge. SCR turned fully on.
		2600	2600	2100	A	60 Hz half cycle sine wave or 5 ms rectangular pulse. Following any rated load condition, and with rated V_{RRM} applied following surge. SCR turned fully on.
I^2t	Max. I^2t capability for fusing	31,000	31,000	20,000	A^2s	t = 10 ms. Rated V_{RRM} applied following surge, initial T_J = 125°C.
		28,500	28,500	18,000	A^2s	t = 8.3 ms. Rated V_{RRM} applied following surge, initial T_J = 125°C.
V_{TM}	Max. peak on-state voltage	2.70	2.70	3.15	V	T_J = 25°C, $I_{T(AV)}$ = 160A (503A peak), I_G = 2A (160PFT100 & 120,A), I_G = 2.4A (160PFT140 & 160)
I_L	Typical latching current	20	20	20	A	T_J = 25°C
I_H	Typical holding current	20	20	20	A	T_J = 25°C
BLOCKING						
dv/dt	Min. critical rate-of-rise of off-state voltage	1000	1000	1000	V/μs	Gate voltage = -2V; T_J = 125°C, V_D = 0.5 V_{DRM}
		200	200	200	V/μs	Gate-to-cathode resistance = 2Ω; T_J = 125°C, V_D = 0.5 V_{DRM}
I_{DM} & I_{RM}	Max. peak off-state and reverse current	50	50	50	mA	T_J = 125°C, V_{DM} = rated V_{DRM}. Peak off-state current applies for -2V or more negative gate voltage or for gate-to-cathode resistance = 2Ω.
SWITCHING						
di/dt	Max. repetitive rate-of-rise of turned-on current	600	600	600	A/μs	$di_G/dt \geqslant$ 5 A/μs, $+I_{GM} \geqslant$ 5A (160PFT100 & 120,A), $+I_{GM} \geqslant$ 6A (160PFT140 & 160), $I_{TM} \leqslant$ 600A, $V_D \leqslant$ 0.5 V_{DRM}.

① Peak off-state voltages apply for -2V or more negative gate voltage, or for gate-to-cathode resistance = 2 ohms. Peak reverse voltages apply for zero or negative gate voltage.

② $G_{GQ} = \frac{I_T}{\text{applied } I_{GQ}}$ = forced turn-off gain. I_T = on-state current. Applied I_{GQ} = maximum negative gate current during turn-off interval.

③ I^2t for time $t_x = I^2\sqrt{t} \bullet \sqrt{t_x}$.

ELECTRICAL SPECIFICATIONS (Continued)

		160PFT100 160PFT120	160PFT100A 160PFT120A	160PFT140 160PFT160	Units	Conditions
	SWITCHING (Continued)					
t_{gt}	Max. turn-on time	5.0	5.0	6.0	µs	t_{gt} is measured from the instant at which $i_G = 0.1 I_{GM}$ to the instant at which $V_D = 0.1 V_D$ with resistive load. $T_J = 125^oC$, $I_T = 600A$, $+I_{GM} = 5A$ (160PFT100&120,A), $+I_{GM} = 6A$ (160PFT140 & 160), $di_G/dt = 5$ A/µs, $V_D = 0.5\ V_{DRM}$.
t_{on}	Min. permissible on-time	10	10	12	µs	t_{on} is the time necessary to ensure that all cathode islands are in conduction. $T_J = 125^oC$, $I_T = 600A$, $V_D = 0.5\ V_{DRM}$, $I_{GM} = 5A$ (160PFT100 & 120,A), = 6A, (160PFT140 & 160), $di_G/dt = 5$ A/µs.
t_{gq}	Max. gate-controlled turn-off time	8.0	8.0	8.0	µs	t_{gq} is measured from instant at which $I_G = -12A$ to instant at which $I_T = 60A$ with resistive load. $T_J = 125^oC$, $I_T = 600A$, $V_D = 0.5\ V_{DRM}$, $di_G/dt = 50$ A/µs, $G_{GQ} = 5$. (1)
t_f	Max. fall time	0.8	0.8	0.8	µs	t_f is measured from instant at which $i_T = 540A$ to instant at which $i_T = 60A$ with resistive load. $T_J = 125^oC$, $I_T = 600A$, $V_D = 0.5\ V_{DRM}$, $di_G/dt = 50$ A/µs, $G_{GQ} = 5$. (1)
t_{off}	Min. permissible off-time	38	38	38	µs	t_{off} is measured from the instant at which the turn-off pulse is applied to the gate to the earliest instant at which the GTO may be retriggered. $T_J = 125^oC$, $I_T = 600A$, $di_G/dt = 50$ A/µs, $G_{GQ} = 5$. (1)
	TRIGGERING					
$P_{GF(AV)}$	Max. average forward gate power	10	10	10	W	Forward gate power is produced by positive gate current, reverse gate power is produced by negative gate current.
P_{GRM}	Max. peak reverse gate power	8000	8000	8000	W	$t_p \leqslant 5$ µs.
$P_{GR(AV)}$	Max. average reverse gate power	20	20	20	W	
$+I_{GM}$	Max. peak positive gate current	100	100	100	A	$t_p \leqslant 100$ µs. Positive gate current may not be applied during reverse recovery interval.
$-I_{GM}$	Max. peak negative gate current	50	50	50	mA	$T_J = 125^oC$, $-V_{GM}$ = rated $-V_{GRM}$, SCR blocking.
$-V_{GRM}$	Max. repetitive peak negative gate voltage	18	18	18	V	SCR blocking.
I_{GT}	Max. required DC gate current to trigger	2.5	2.5	3.0	A	$T_C = -40^oC$ Max. required gate trigger current is the lowest value which will trigger all units with +12 volts anode-to-cathode and $I_T = 50A$ after triggering.
		1.0	1.0	1.2		$T_C = 25^oC$
		0.35	0.35	0.5		$T_C = 125^oC$
V_{GT}	Max. required DC gate voltage to trigger	1.4	1.4	1.5	V	$T_C = -40^oC$ Max. required gate trigger voltage is the lowest value which will trigger all units with +12 volts anode-to-cathode and $I_T = 50A$ after triggering.
		1.0	1.0	1.0		$T_C = 25^oC$

THERMAL-MECHANICAL SPECIFICATIONS

T_J	Junction operating temperature range	-40 to 125	^oC	
T_{stg}	Storage temperature range	-40 to 125	^oC	
R_{thJC}	Max. internal thermal resistance, junction-to-case	0.075	deg. C/W	DC operation; double side cooled, mounting force = 4900N (1100 lbf)
R_{thCS}	Thermal resistance, case-to-sink	0.035	deg. C/W	Mounting surface smooth, flat and greased. One pole piece to one heat sink.
F	Mounting force	4900 to 5900 (1100 to 1325)	N (lbf)	
wt	Approximate weight	140 (5)	g (oz.)	
	Case Style	IR: A-30		

(1) $G_{GQ} = \frac{I_T}{\text{applied } I_{GQ}}$ = forced turn-off gain. I_T = on-state current. Applied I_{GQ} = maximum negative gate current during turn-off interval.

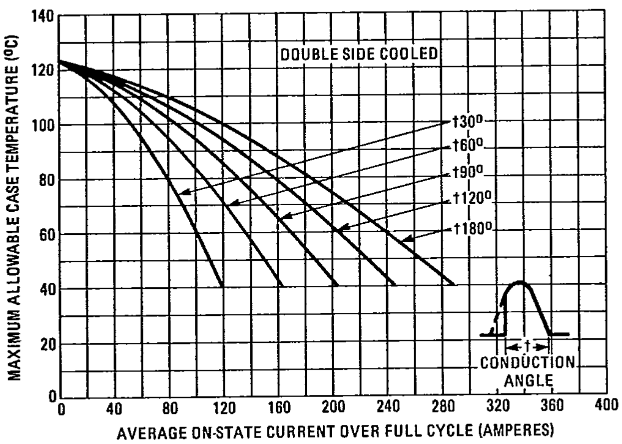


Fig. 1 – Maximum Allowable Case Temperature Vs. Average On-State Current (Sinusoidal Current Waveform), 160PFT100,A & 160PFT120,A

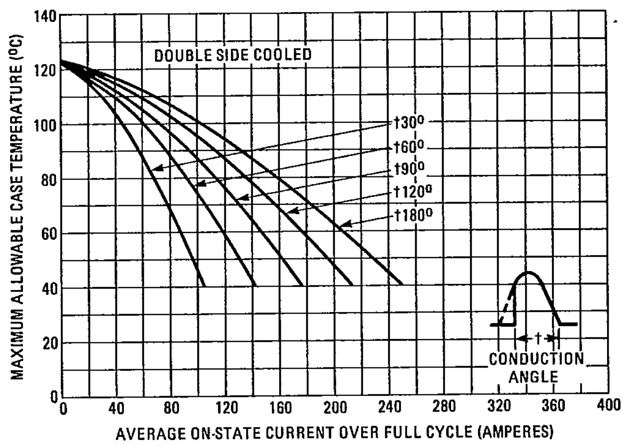


Fig. 2 – Maximum Allowable Case Temperature Vs. Average On-State Current (Sinusoidal Current Waveform), 160PFT140 & 160PFT160

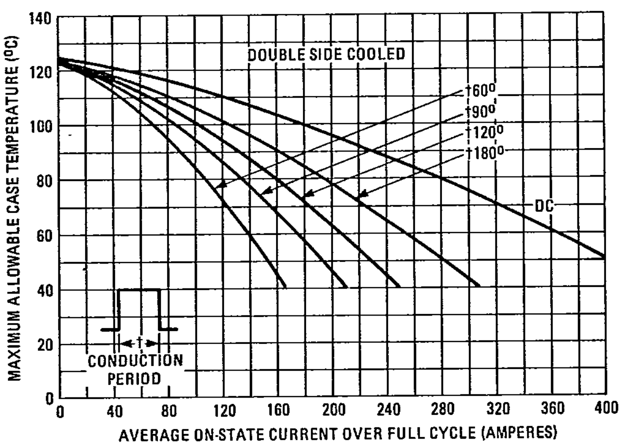


Fig. 3 – Maximum Allowable Case Temperature Vs. Average On-State Current (Rectangular Current Waveform), 160PFT100,A & 160PFT120,A

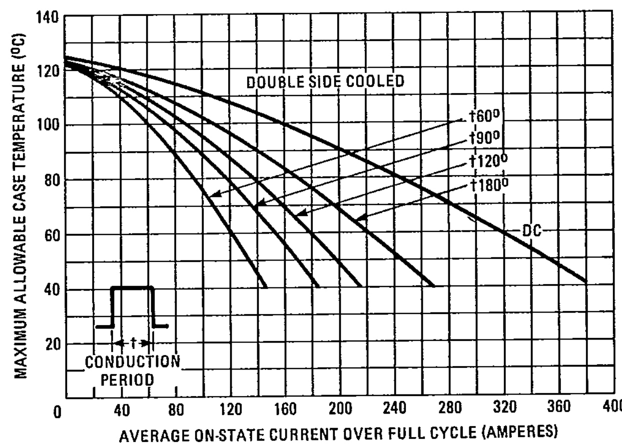


Fig. 4 – Maximum Allowable Case Temperature Vs. Average On-State Current (Rectangular Current Waveform), 160PFT140 & 160PFT160

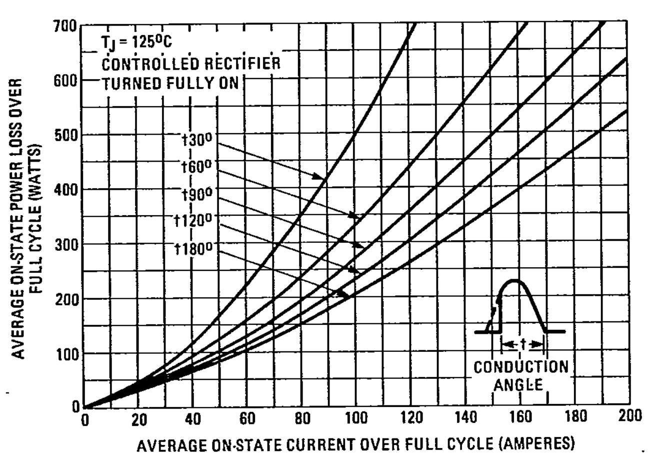


Fig. 5 – Maximum Low Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 160PFT100,A & 160PFT120,A

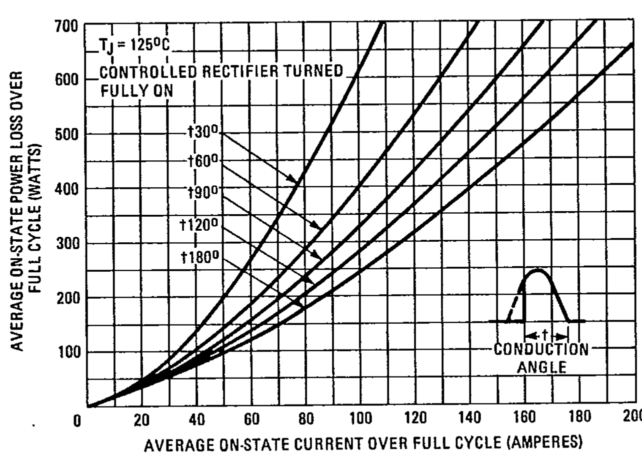


Fig. 6 – Maximum Low Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 160PFT140 & 160PFT160

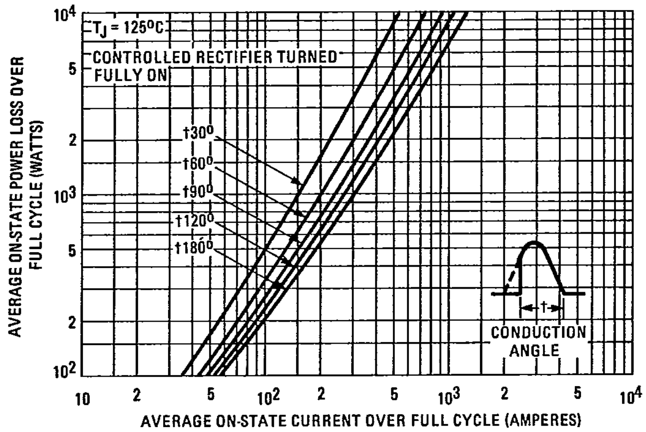


Fig. 7 — Maximum High Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 160PFT100,A & 160PFT120,A

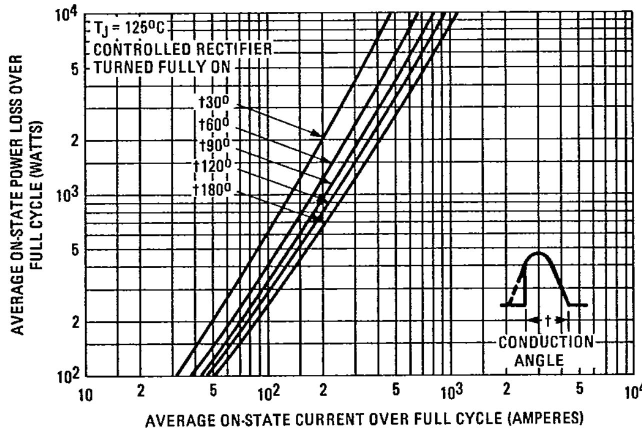


Fig. 8 — Maximum High Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 160PFT140 & 160PFT160

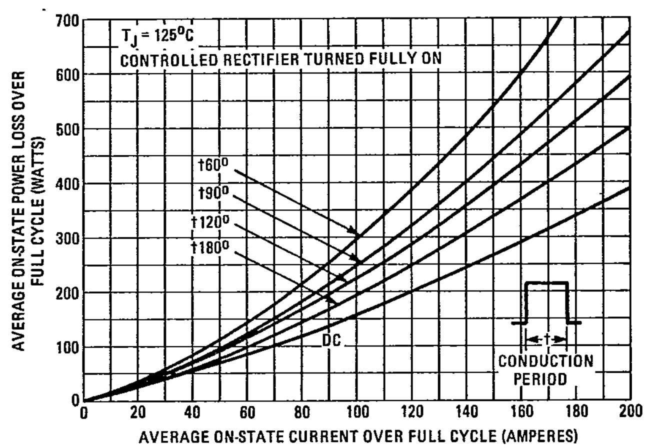


Fig. 9 — Maximum Low Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 160PFT100,A & 160PFT120,A

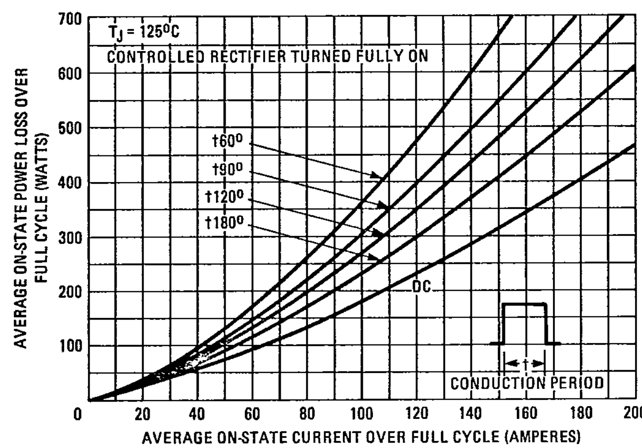


Fig. 10 — Maximum Low Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 160PFT140 & 160PFT160

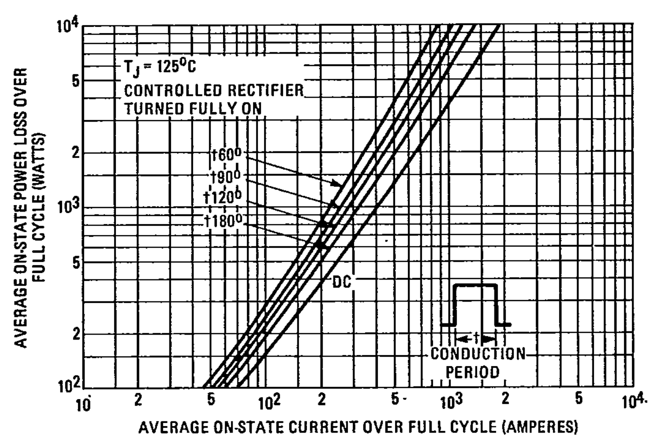


Fig. 11 — Maximum High Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 160PFT100,A & 160PFT120,A

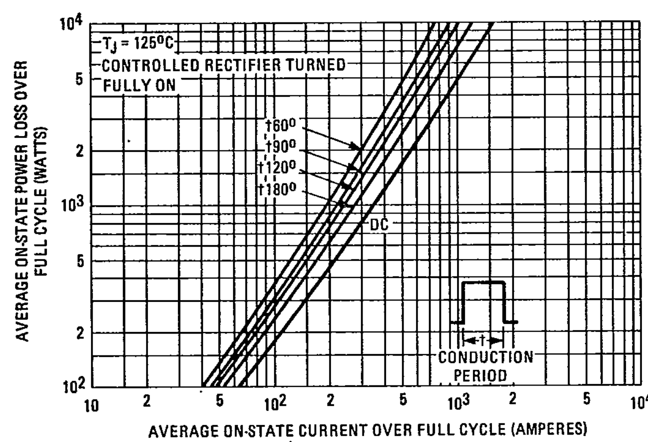


Fig. 12 — Maximum High Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 160PFT140 & 160PFT160

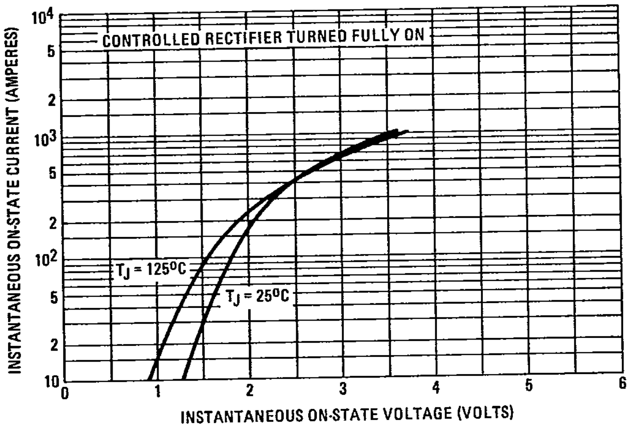


Fig. 13 – Maximum Instantaneous On-State Voltage Vs. Instantaneous On-State Current, 160PFT100,A & 160PFT120,A

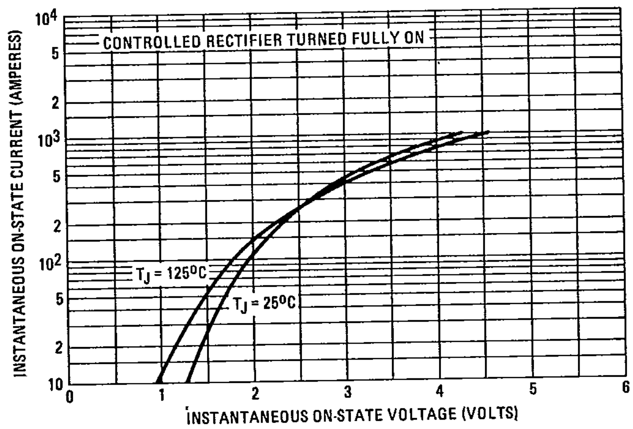


Fig. 14 – Maximum Instantaneous On-State Voltage Vs. Instantaneous On-State Current, 160PFT140 & 160PFT160

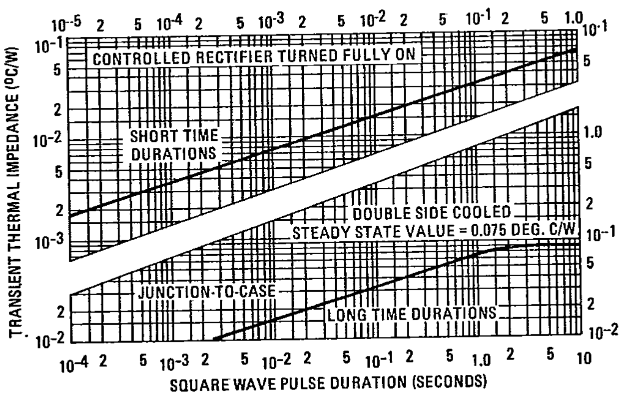


Fig. 15 – Maximum Transient Thermal Impedance Vs. Square Wave Pulse Duration, All Devices

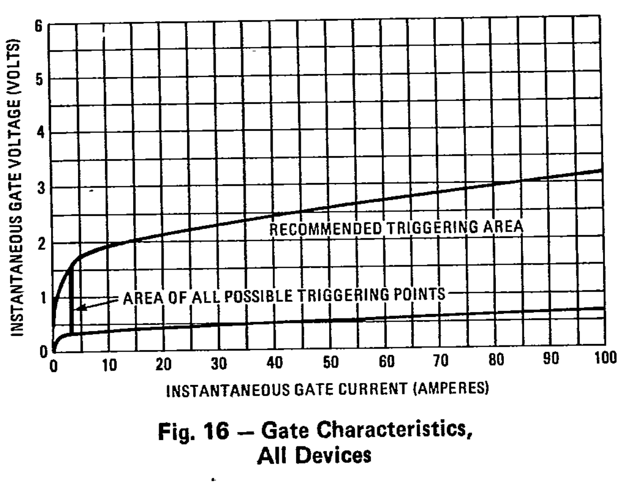


Fig. 16 – Gate Characteristics, All Devices

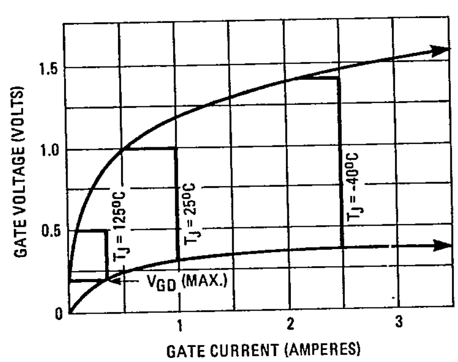


Fig. 16a – Areas of All Possible Triggering Points, 160PFT100,A & 160PFT120,A

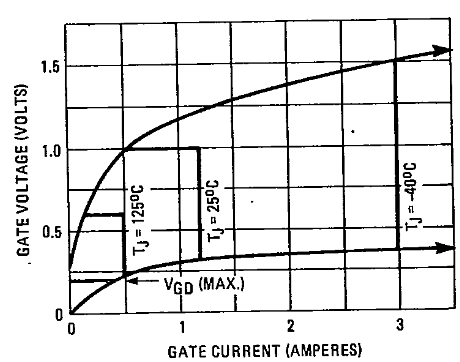


Fig. 16b – Areas of All Possible Triggering Points, 160PFT140 & 160PFT160

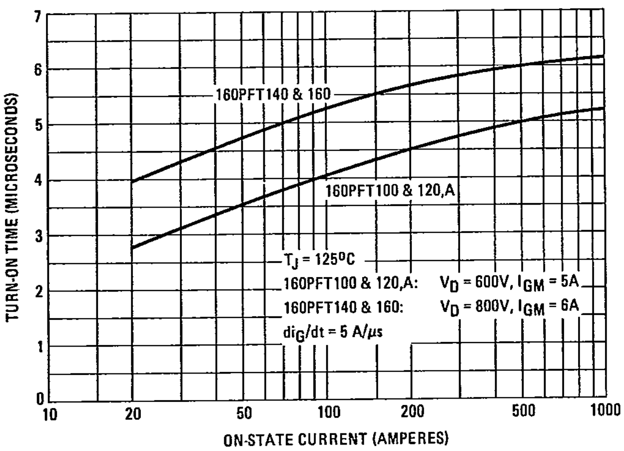


Fig. 17 – Turn-On Time Vs. On-State Current, All Devices

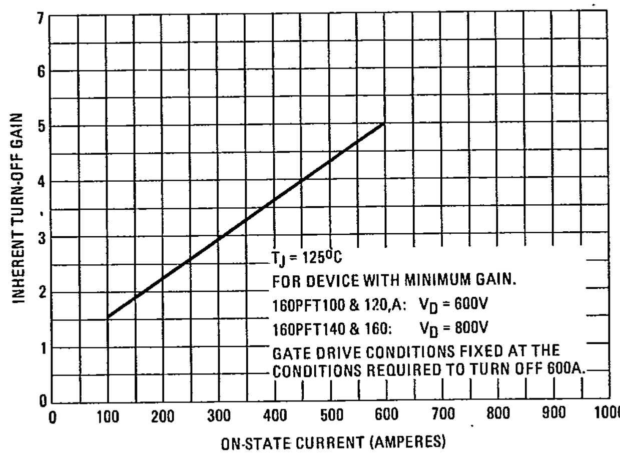


Fig. 18 – Inherent Turn-Off Gain Vs. Instantaneous On-State Current, All Devices

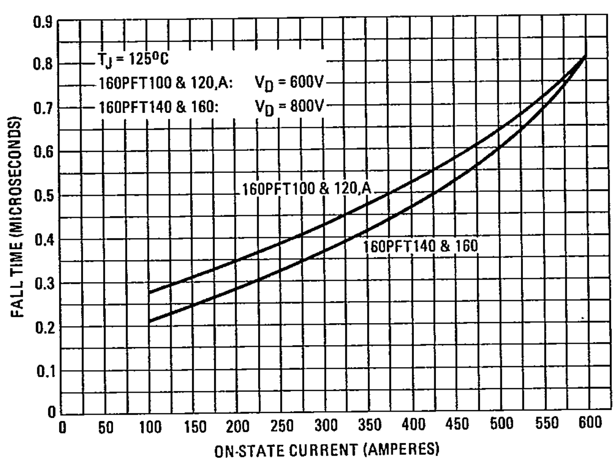


Fig. 19 – Maximum Fall Time Vs. On-State Current, All Devices

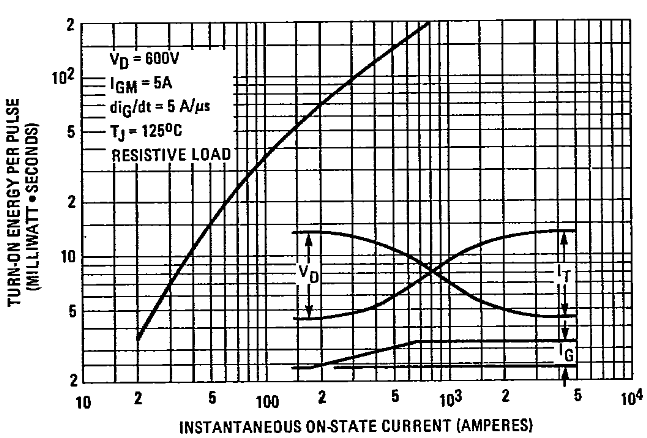


Fig. 20 – Maximum Turn-On Energy Per Pulse Vs. On-State Current, 160PFT100,A & 160PFT120,A

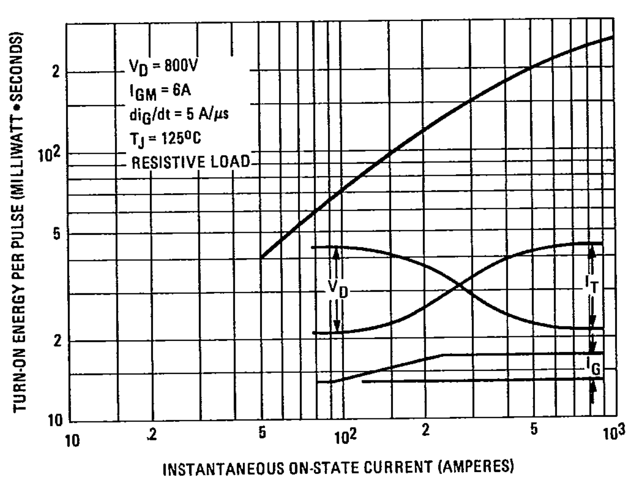


Fig. 21 – Maximum Turn-On Energy Per Pulse Vs. On-State Current, 160PFT140 & 160PFT160

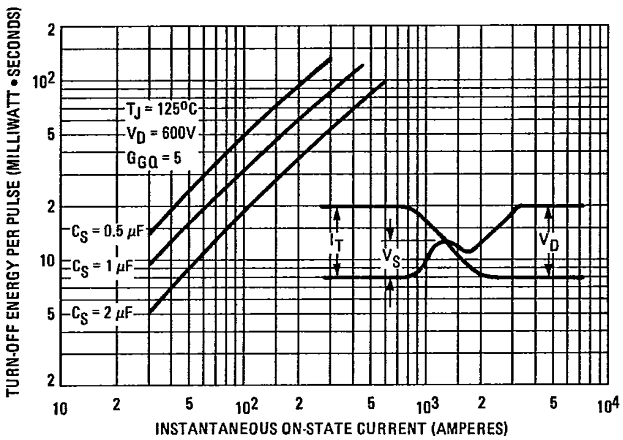


Fig. 22 — Maximum Turn-Off Energy Per Pulse Vs. On-State Current, 160PFT100,A & 160PFT120,A

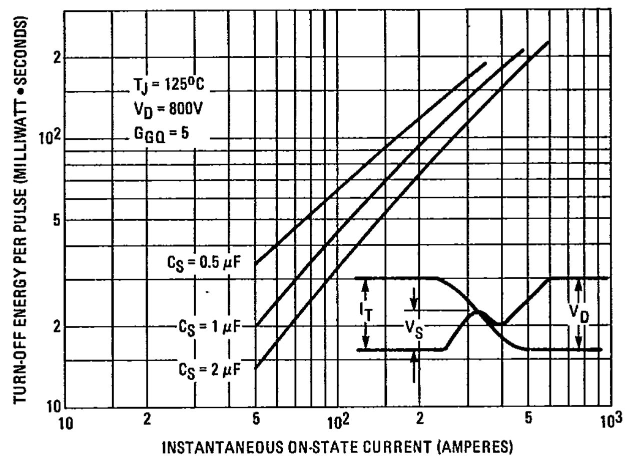


Fig. 23 — Maximum Turn-Off Energy Per Pulse Vs. On-State Current, 160PFT140 & 160PFT160

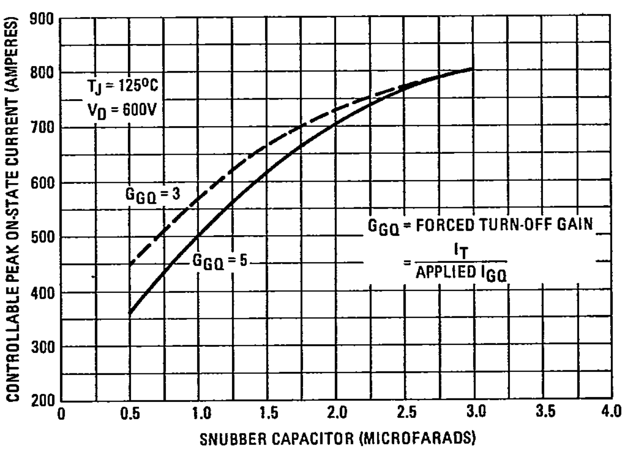


Fig. 24 — Maximum Controllable Peak On-State Current Vs. Snubber Capacitor Value, 160PFT100A & 160PFT120A

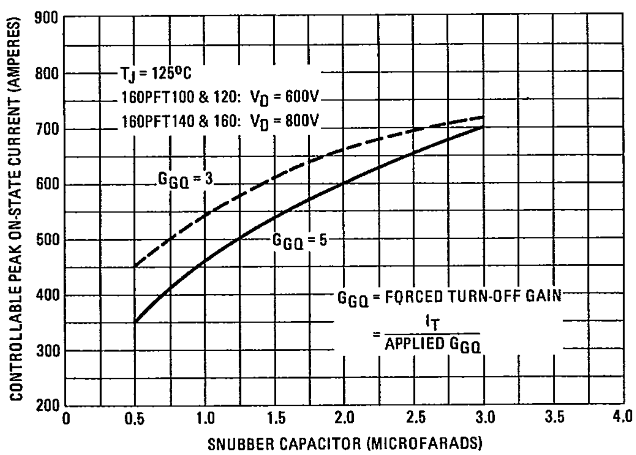


Fig. 25 — Maximum Controllable Peak On-State Current Vs. Snubber Capacitor Value, 160PFT100 through 160PFT160

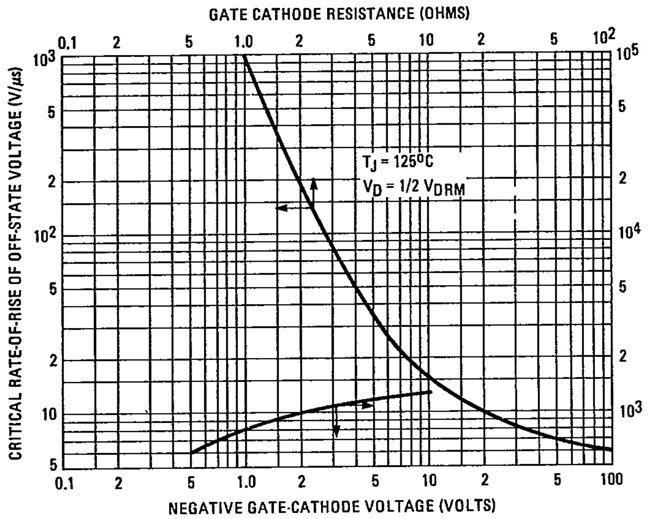


Fig. 26 — Minimum Critical Rate-of-Rise of Off-State Voltage Vs. Negative Gate-Cathode Voltage and Vs. Gate-Cathode Resistance, All Devices

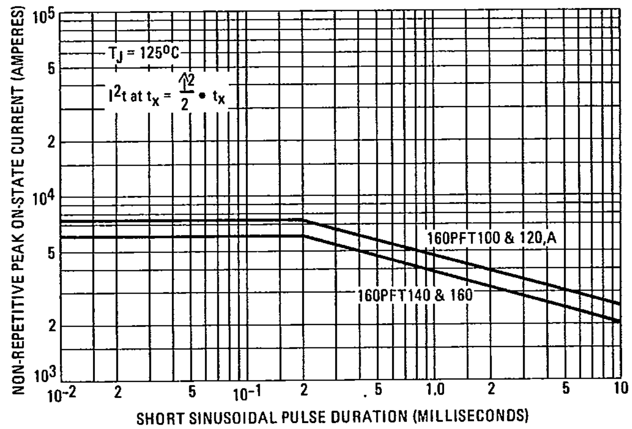
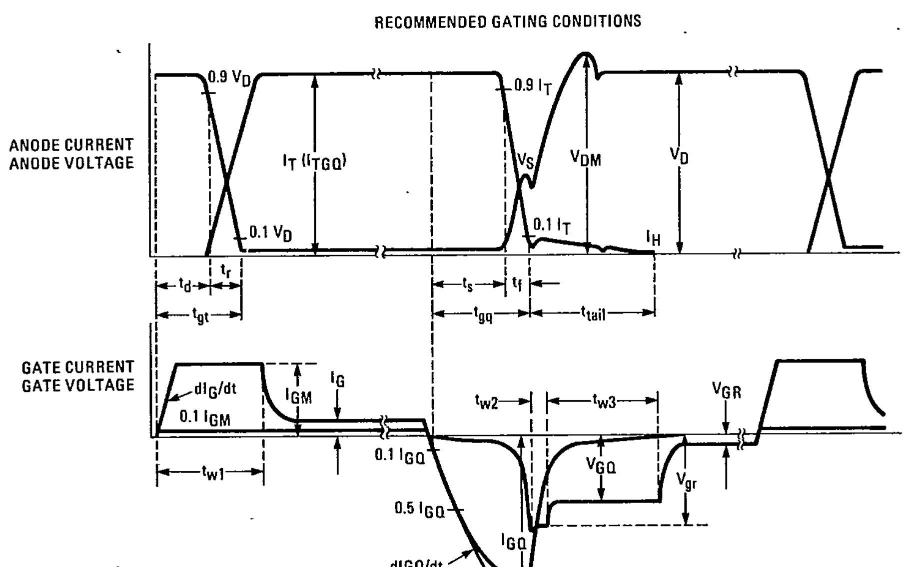


Fig. 27 — Non-Repetitive Peak On-State Current Vs. Sinusoidal Pulse Duration, All Devices



$I_{GM} \geq 8.5A$*
$dI_G/dt \geq 5$ A/μs
$I_G \geq 1.7A$*
$t_{w1} \geq 10$ μs

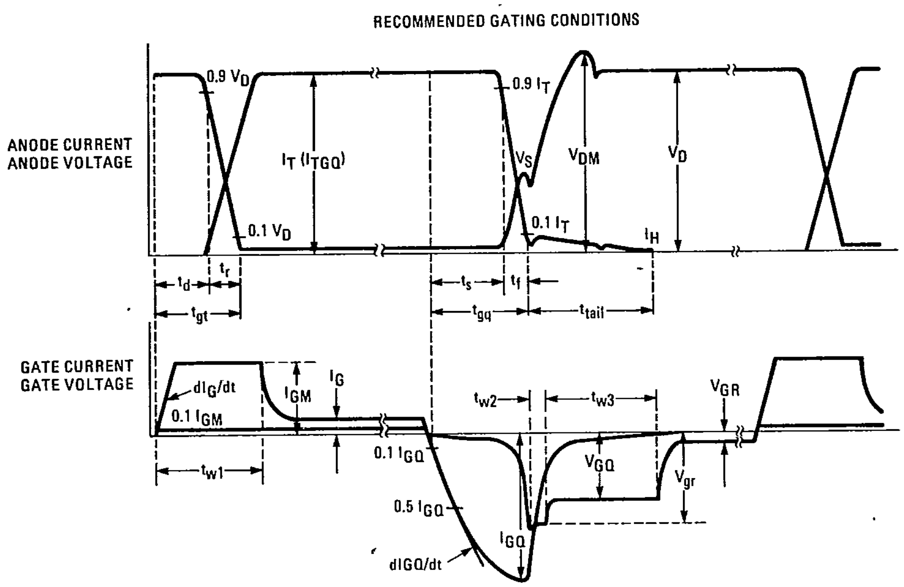
$I_{GQ} \geq I_{TGQ}/5$
$dI_{GQ}/dt \geq 20$ A/μs
V_{GQ} = 12 ~ 18V
V_{GR} = 2 ~ 18V

V_{gr}: AVALANCHE VOLTAGE OF G-K JUNCTION
$t_{w2} \leq 5$ μs
$t_{w3} \leq 25$ μs
$t_{w2} + t_{w3} \geq 30$ μs

*ASSUMED DEVICE OPERATED DOWN TO -10°C.

Fig. 28 — Recommended Gating Conditions, 160PFT100,A & 160PFT120,A

SNUBBER CAPACITOR Cs (μF)	SNUBBER RESISTOR Rs (Ω)	MINIMUM ON-TIME (μs)
3	10	75
	5	45
2	10	50
	5	24
1	10	24
	5	14



$I_{GM} \geq 10A$*
$dI_G/dt \geq 5\ A/\mu s$
$I_G \geq 2.0A$*
$t_{w1} \geq 12\ \mu s$

$I_{GQ} \geq I_{TGQ}/5$
$dI_{GQ}/dt \geq 20\ A/\mu s$
$V_{GQ} = 12 \sim 18V$
$V_{GR} = 2 \sim 18V$

V_{gr}: AVALANCHE VOLTAGE OF G-K JUNCTION
$t_{w2} \leq 5\ \mu s$
$t_{w3} \leq 25\ \mu s$
$t_{w2} + t_{w3} \geq 30\ \mu s$

*ASSUMED DEVICE OPERATED DOWN TO -10°C.

Fig. 29 – Recommended Gating Conditions, 160PFT140 & 160PFT160

SNUBBER CAPACITOR Cs (μF)	SNUBBER RESISTOR Rs (Ω)	MINIMUM ON-TIME (μs)
3	10	75
	5	45
2	10	50
	5	24
1	10	24
	5	14